Machine Learning for 3D IC Floorplanning

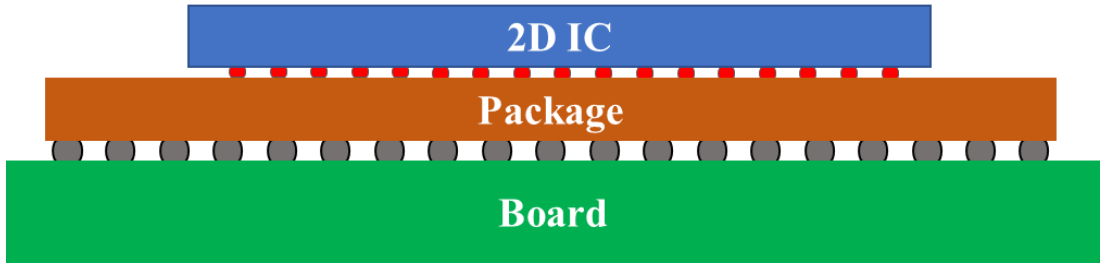
Dima Al Saleh

ECSE 689

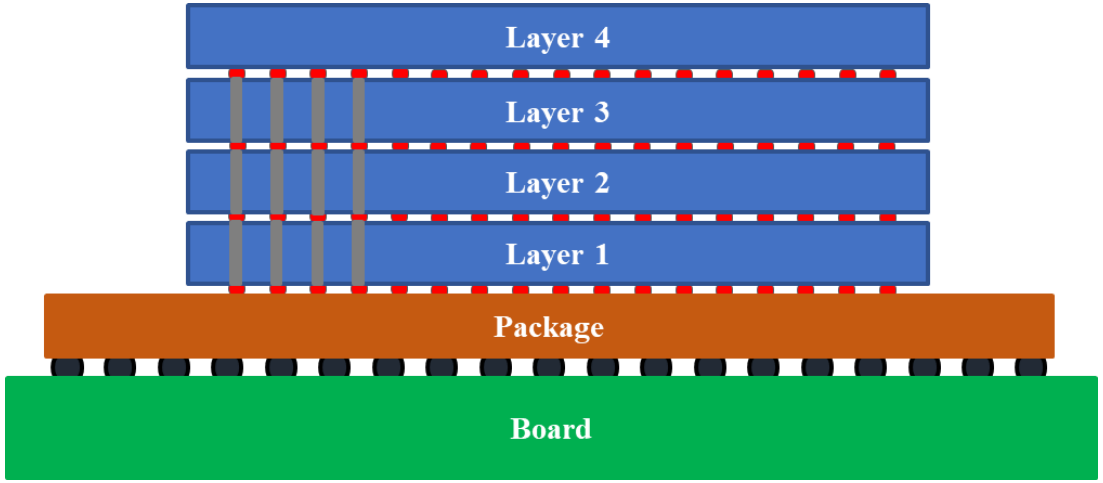
November 27, 2024

3D ICs – Overview

- Three dimensional Integrated Circuits
  - Exploit vertical dimension
  - Connected using Through Silicon Vias TSVs
- Thickness increases but not impactfully (each layer 150 μm)



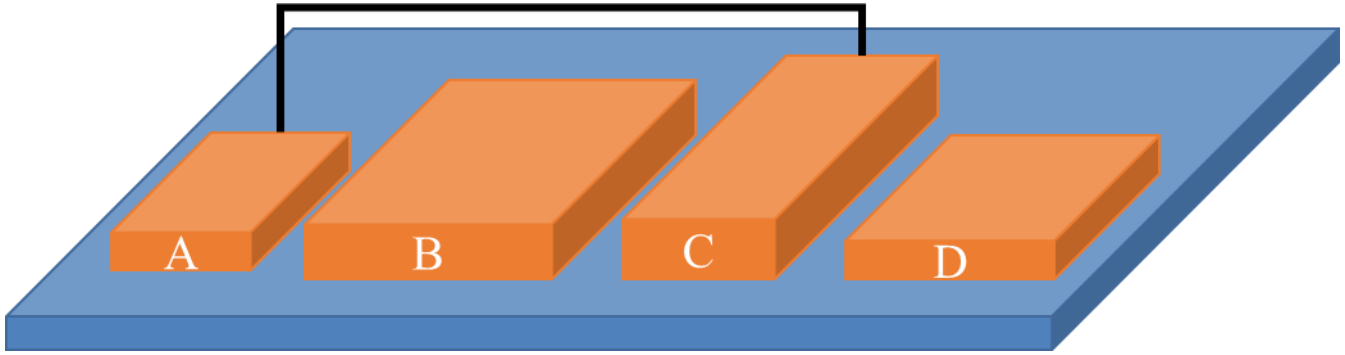
2D IC



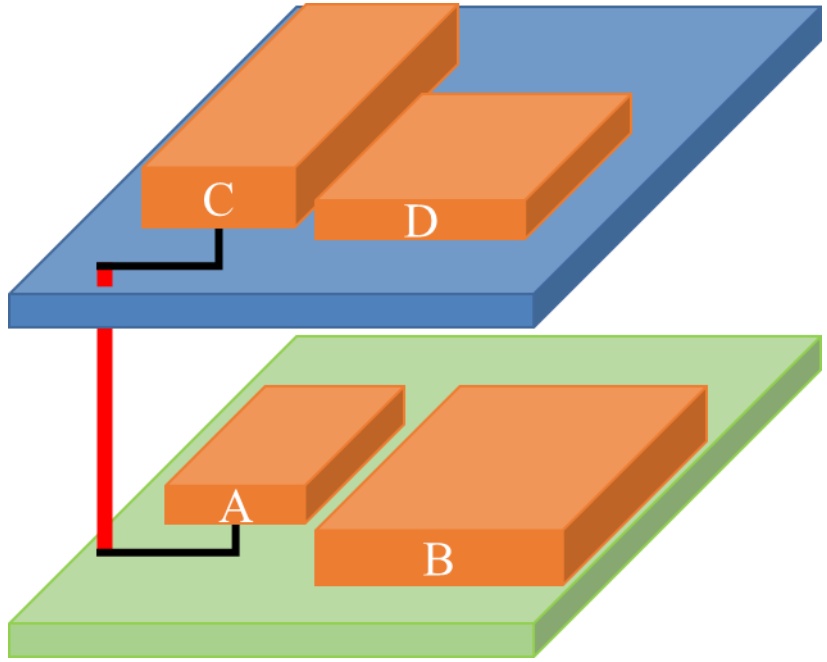
3D IC

3D ICs – Advantages

- Advantages
  - More heterogeneity
  - Less area
  - Less wirelength
  - Less communication power
  - Ideal for complex applications



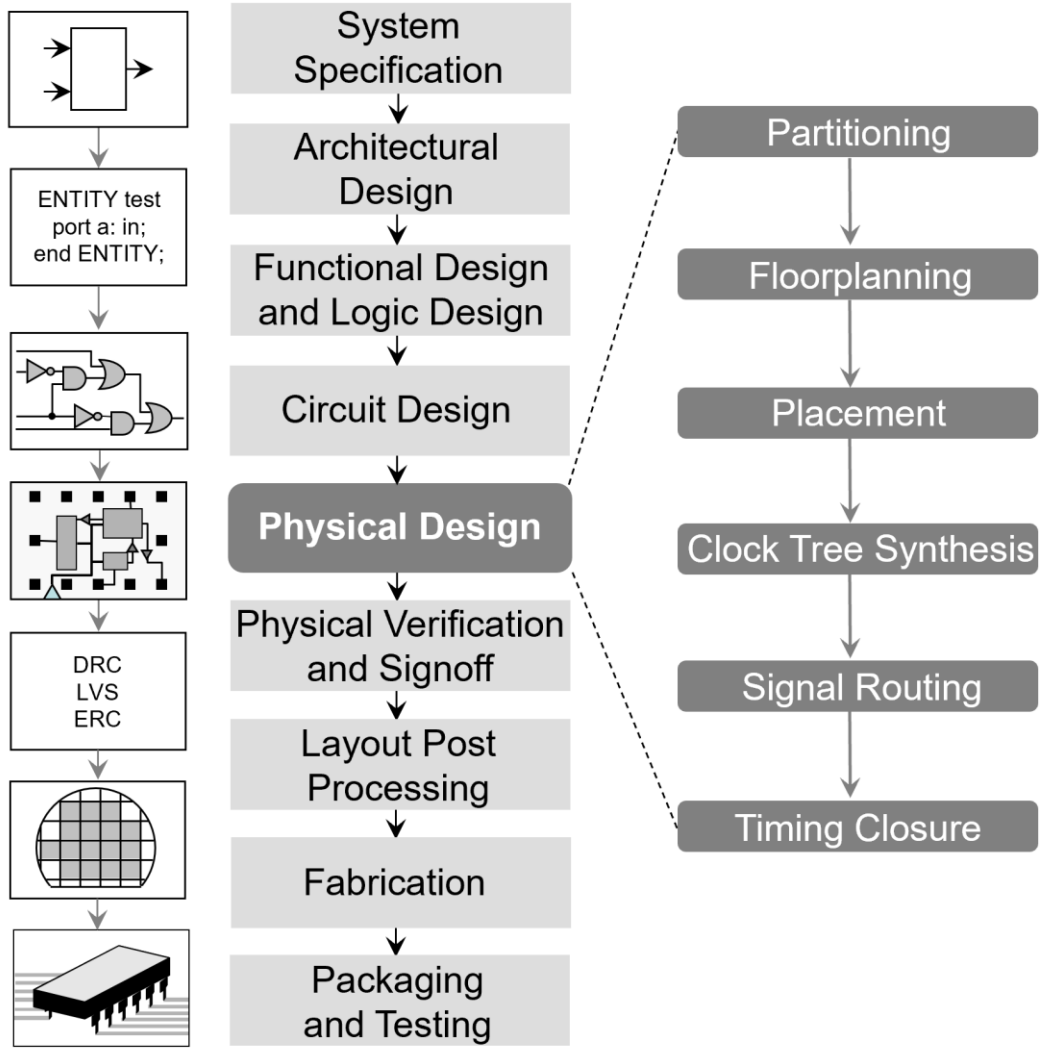
2D IC



3D IC

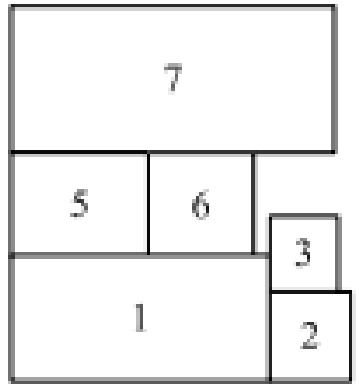
3D ICs – Design Challenge

- Design of circuit is crucial
  - Impacts performance & lifetime
- Floorplanning
  - Main step in IC design
  - Outputs coordinates (*x*, *y*, and *z*) of circuit components

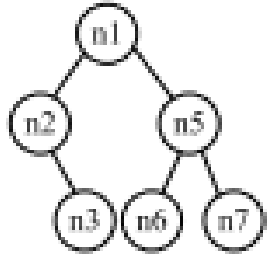


3D ICs – Floorplanning

- Circuit components
  - CPU, Memory, Caches, Branch predictors, …
  - Referred to as blocks
- Input of floorplanner: the netlist
  - List of blocks & dimensions
  - Power (for thermal)
  - Connections (for wirelength and TSVs)



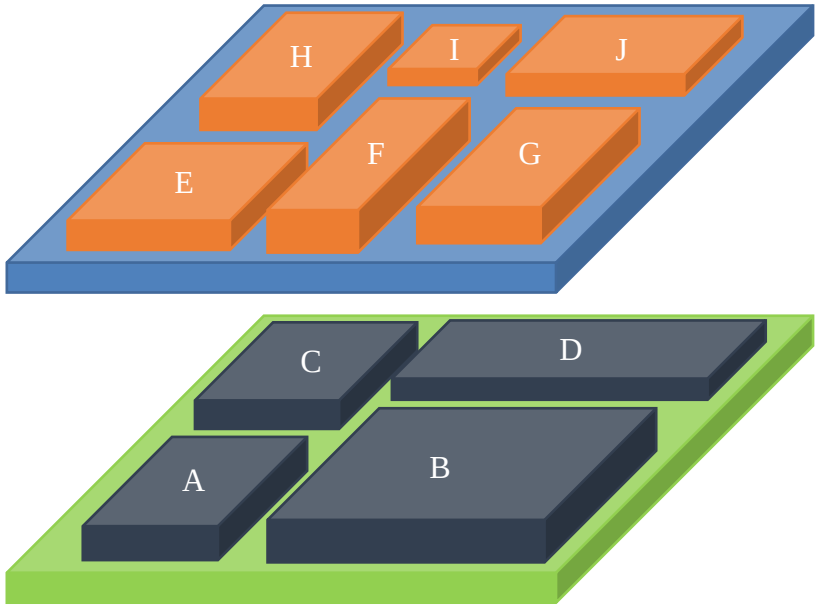
Layer 1



Layer 1

3D IC Floorplanners – Gap and Research Question

- Exponentially increase of runtime
  - With each added layer
  - More blocks to floorplan
  - Failure to converge of search-based algorithms
- No ML based 3D IC floorplanner
  - Even though exists in 2D



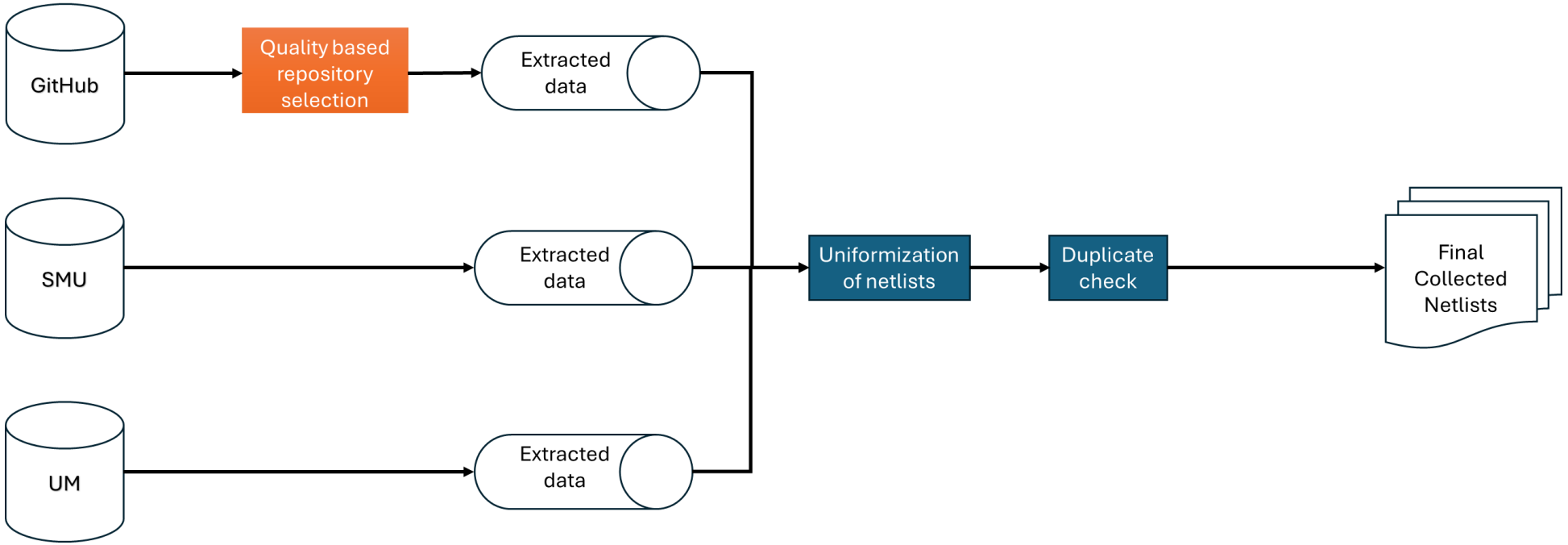
What is the performance of the best-known ML optimization models for 3D IC floorplanning?

ML-Based 3D Floorplanner

- Need for dataset
  - ML models require datasets
- Train models on different circuits
  - Circuits properties (number of blocks, average width, aspect ratio (width/height)…)
- Purpose of dataset
  - **Width & height**: Area optimization
  - **Power**: Thermal optimization
  - **Connections**: Wirelength and number of TSV optimization

Dataset Sources

- Lack of reputable repositories
  - Circuits are proprietary (not available)
  - Need for netlists with industry significance
    - Practical characteristics
- Snowballing technique



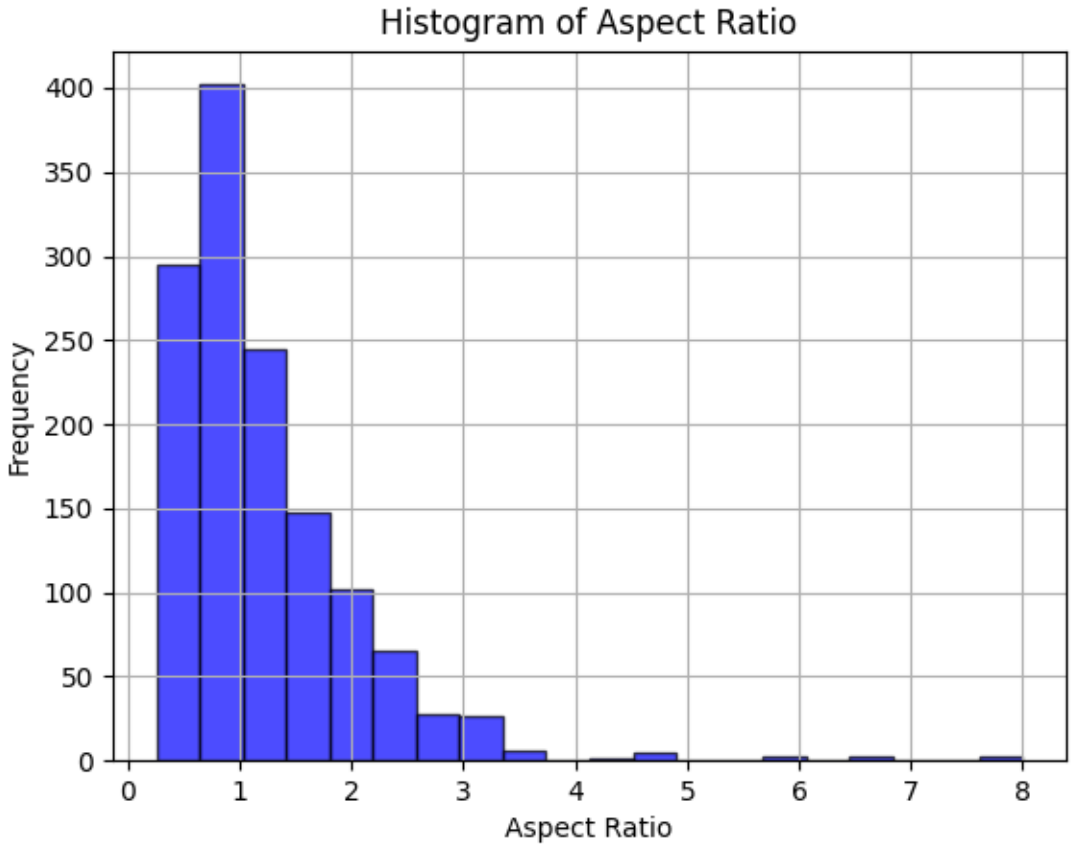
Data Extraction

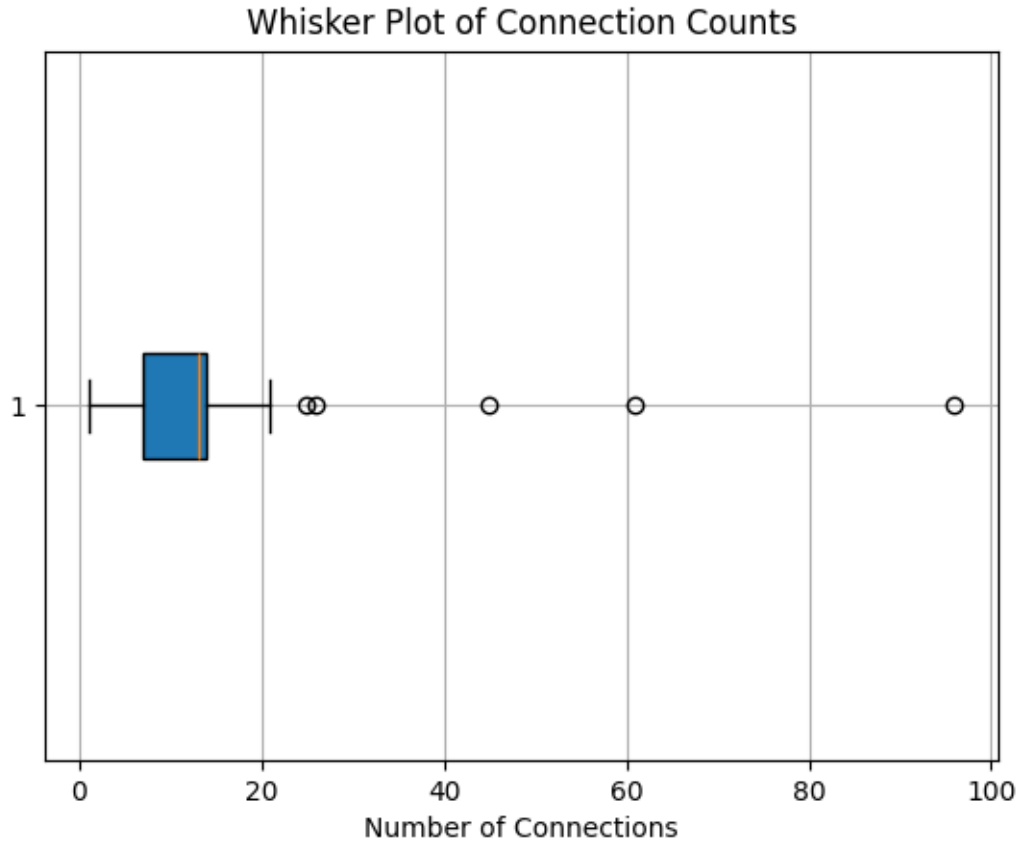
- Manual for UM and SMU
- Scripts for GitHub repositories
- Uniformization process
  - Raw netlist written differently

```
MODULE bk1;
 TYPE GENERAL;
 DIMENSIONS 336 0 336 133 0 133 0 0;
 IOLIST;
  P_0 PWR 175 0 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
  P_1 PWR 105 0 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
  P_2 B 336 14 1 METAL2;
  P_3 B 0 14 1 METAL2;
  P_4 B 336 7 1 METAL2;
  P_5 B 0 7 1 METAL2;
  P_6 B 336 105 1 METAL2;
  P_7 B 0 105 1 METAL2;
  P_8 B 336 112 1 METAL2;
  P_9 B 0 112 1 METAL2;
  P_10 B 112 133 1 METAL2;
  P_11 B 0 42 1 METAL2;
  P_12 B 273 133 1 METAL2;
 ENDIOLIST;
ENDMODULE;
```

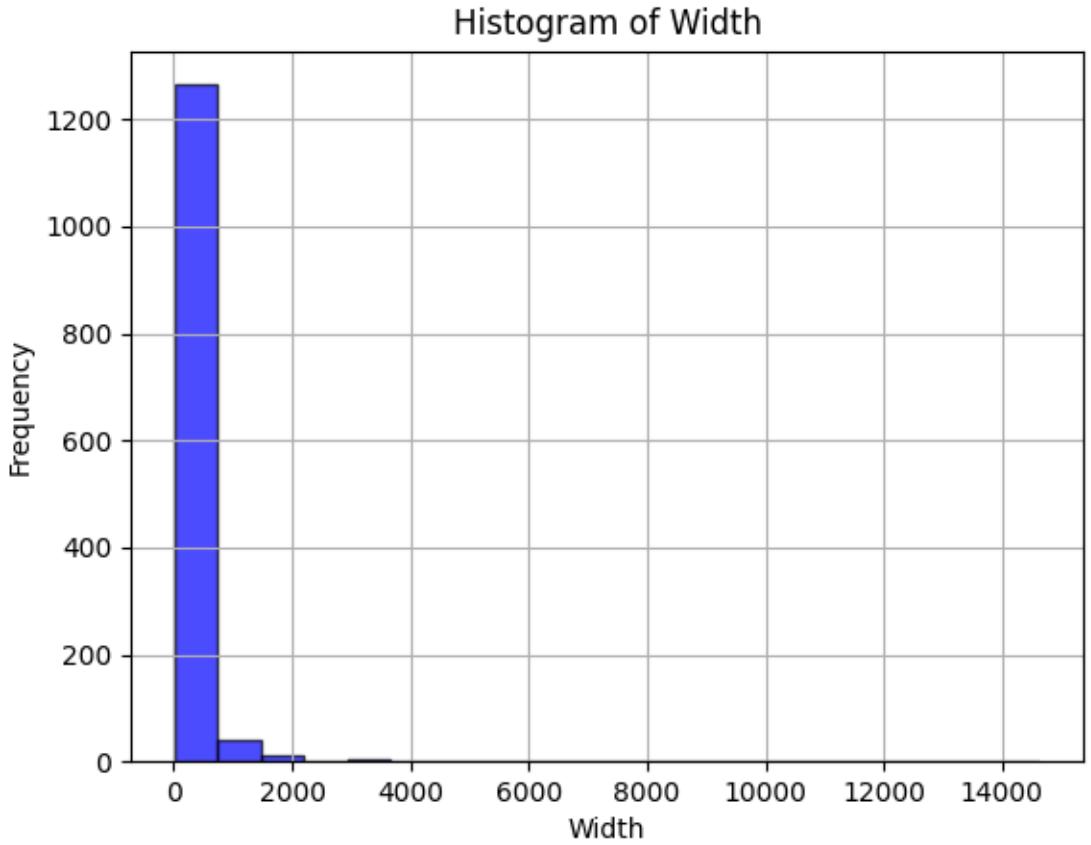
```
# Line Format: <unit-name>\t<area-in-m2>\t<min-aspect-ratio>\t<max-aspect-ratio>\t<rotable>

Icache  8.3459e-6       1       3       1
Dcache  7.8240e-6       1       3       1
Bpred   2.2690e-6       1       5       1
```

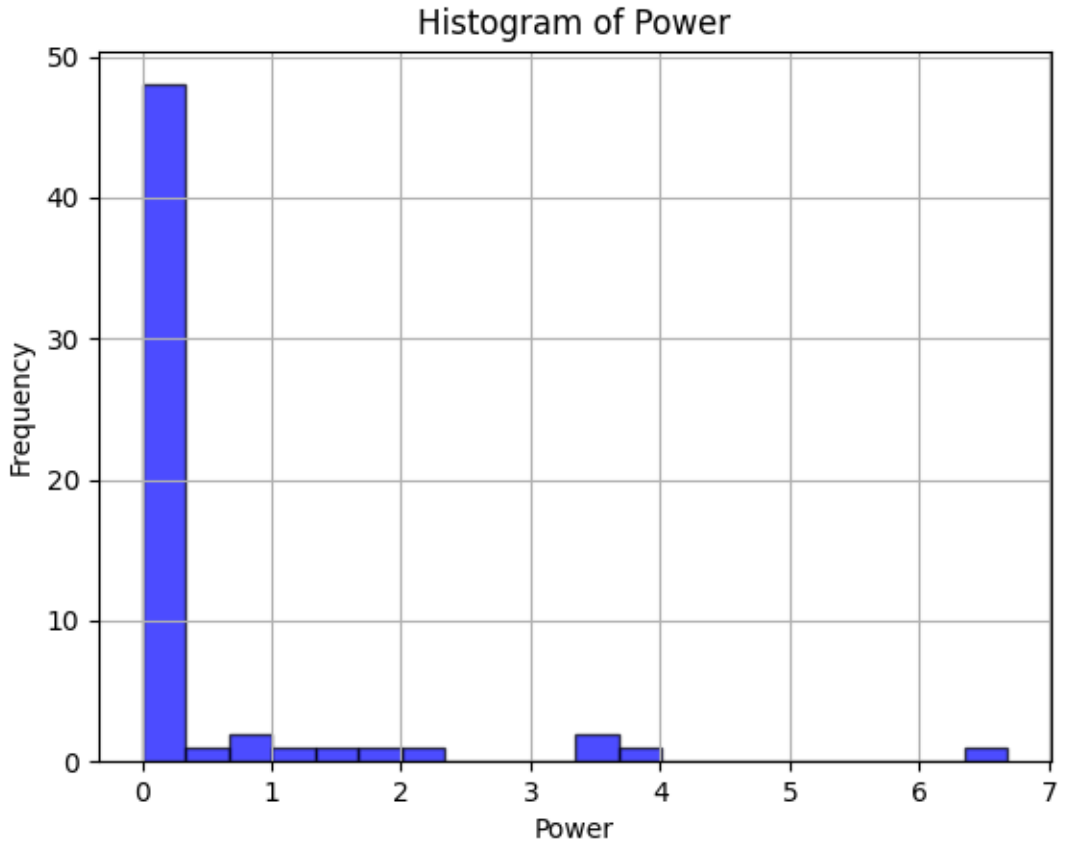
Statistics – Collected Data





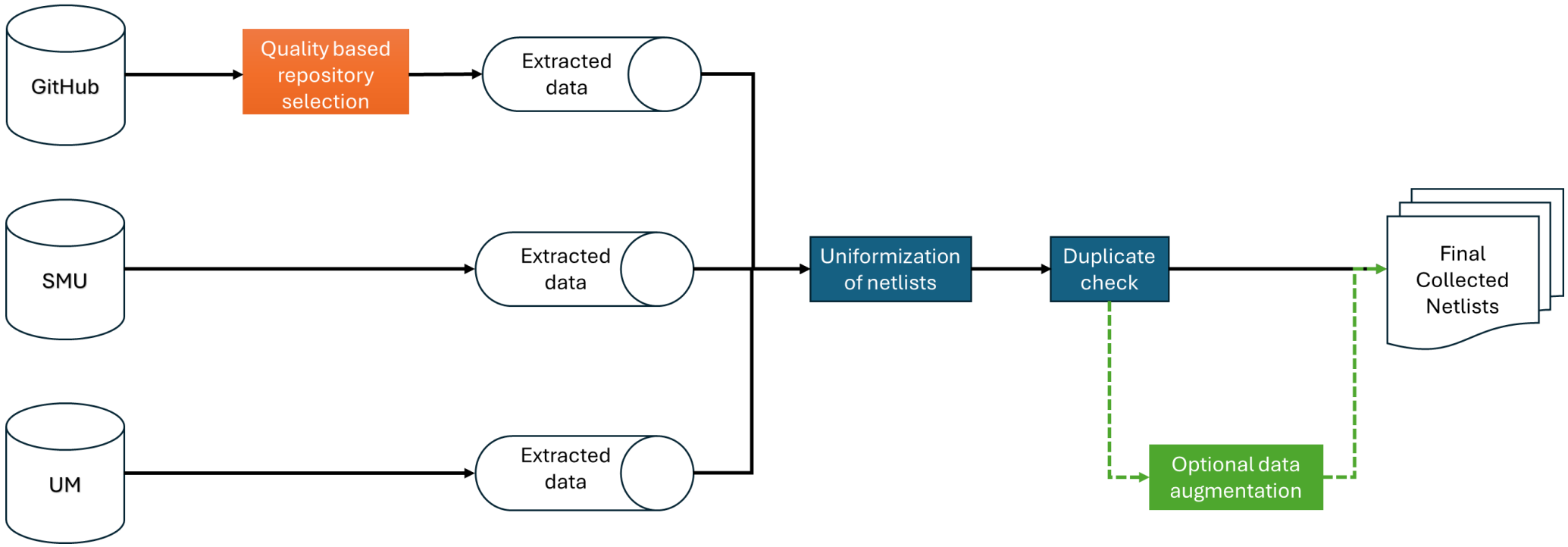
Statistics – Collected Data





Collected Data – Challenge

- Small dataset
  - Only 11 netlists were found
- Data augmentation
  - Based on circuit properties



Conclusions & Next Steps

- 3D ICs are powerful
  - Floorplanning is essential
- What is the performance of the best-known ML optimization models for 3D IC floorplanning?

- Dataset is needed
  - Reputable sources
  - Small dataset available

- Adapt popular 2D floorplanners to floorplan in 3D
  - Determine performance on area, WL, TSVs, thermal

Thank you for Listening!
Any Questions?