Machine Learning for 3D IC Floorplanning

Three-dimensional (3D) integrated circuits (ICs) are gaining popularity as they allow a smaller footprint, shorter interconnects, and more heterogeneity in the system [1]. The shorter interconnects in 3D ICs reduce transmission delay, power consumption, noise, and improve scalability [2]. 3D ICs are therefore crucial for applications like large-scale neural networks, brain modeling, genome sequencing and weather prediction. 3D ICs are formed by integrating multiple heterogeneous circuits on top of one another and connecting these layers of circuitry using through-silicon vias (TSVs). Designing the circuit layers of a 3D IC is a complex yet important step. The quality of the design process impacts greatly the performance and lifetime of the 3D IC [2].

Floorplanning is a main step in the design process of ICs. During this step, the input to the floorplanner is a list of blocks (*macros* or *subchips*) and their properties such as their width, height, connectivity, and power requirements. This input is commonly referred to as "netlist". Once the floorplanning process is completed, coordinates (x, y, and z) for each block are outputted. Floorplanning is essential in the design of 3D ICs since the location of blocks in the circuit greatly impacts on-chip temperature, a key limitation of 3D ICs [3]. As circuits are vertically stacked the temperature on-chip increases significantly, which can cause degradation of the IC [4].

Although there are many computer-aided-design (CAD) tools to facilitate the floorplanning of ICs, few of them have been specifically made to address the unique challenges of 3D ICs and the increasing number of blocks in the circuit. As the number of blocks in 3D ICs increases, traditional floorplanning algorithms based on popular search techniques such as simulated annealing (SA) [5], ant colony (AC) [6], and particle warm optimization (PSO) [7], struggle to keep up. The runtime complexity increases exponentially with each new added layer, and the algorithm fails to converge [8].

Moreover, in 3D IC floorplanning, unlike in 2D ICs, additional factors such as temperature and the number of TSVs must be considered in the design evaluation. In 2D floorplanning, the focus is on optimizing area and wirelength. However, in 3D ICs, co-optimizing all four of these parameters introduces conflicting optimization objectives. Furthermore, accurately estimating the circuit's temperature is a time-consuming process [5].

[9] achieves floorplanning of 2D ICs using a machine learning model, specifically reinforcement learning. However, there has been no effort to develop a machine learning model to floorplan in 3D, with the greater number of blocks in 3D vs 2D, the exponentially larger design space, and the addition of TSVs and temperature in the design requirements.

Therefore, to fill this gap, we propose to study the validity of machine learning optimization algorithms in the floorplanning of 3D ICs. The main research question tackled is: *What is the performance of the best known ML optimization models for 3D IC floorplanning*? To tackle this question and enable training of the various models, a large dataset of both netlists and optimized (good) floorplans are needed. Once the dataset is created, and pre-processed, popular ML models can be trained, tested, and compared based on the quality of their outputted floorplans.

References

[1] "Samsung Announces Availability of its Silicon-Proven 3D IC Technology for High-Performance Applications." Samsung Semiconductor Global, 2023.

[2] V. F. Pavlidis *et al.*, *Three-Dimensional Integrated Circuit Design, Second Edition*, Morgan Kaufmann, 2017.

[3] T. Ni *et al.*, "Temperature-Aware Floorplanning for Fixed-Outline 3D ICs," *IEEE Access*, vol. 7, pp. 139787‑139794, 2019.

[4] B. Vaisband, I. Savidis, and E. G. Friedman, "Thermal Conduction Path Analysis in 3-D ICs," Proceedings of the I*EEE International Symposium on Circuits and Systems (ISCAS)*, pp. 594-597, 2014.

[5] H. Y. Zhu *et al.*, "Floorplanning for 3D-IC with Through-Silicon Via Co-Design Using Simulated Annealing," in *Proceedings of the IEEE Asia-Pacific Symposium on Electromagnetic Compatibility*, pp. 550‑553, 2018.

[6] Q. Xu, S. Chen, and B. Li, "Combining the Ant System Algorithm and Simulated Annealing for 3D/2D Fixed-Outline Floorplanning," *Applied Soft Computing*, vol. 40, pp. 150‑160, 2016.

[7] G. Chen, W. Guo, H. Cheng, X. Fen, and X. Fang, "VLSI Floorplanning Based on Particle Swarm Optimization," in *Proceedings of the 3rd International Conference on Intelligent System and Knowledge Engineering (ISKE)*, vol. 1, pp. 1020‑1025, 2008.

[8] P. Zhou et al., “3D-STAF: Scalable Temperature and Leakage Aware Floorplanning for Three-Dimensional Integrated Circuits,” Proceedings of the IEEE/ACM International Conference on Computer-Aided Design, November 2007.

[9] A. Mirhoseini *et al.*, “A Graph Placement Methodology for Fast Chip Design,” *Nature*, vol. 594, no. 7862, pp. 207‑212, 2021.