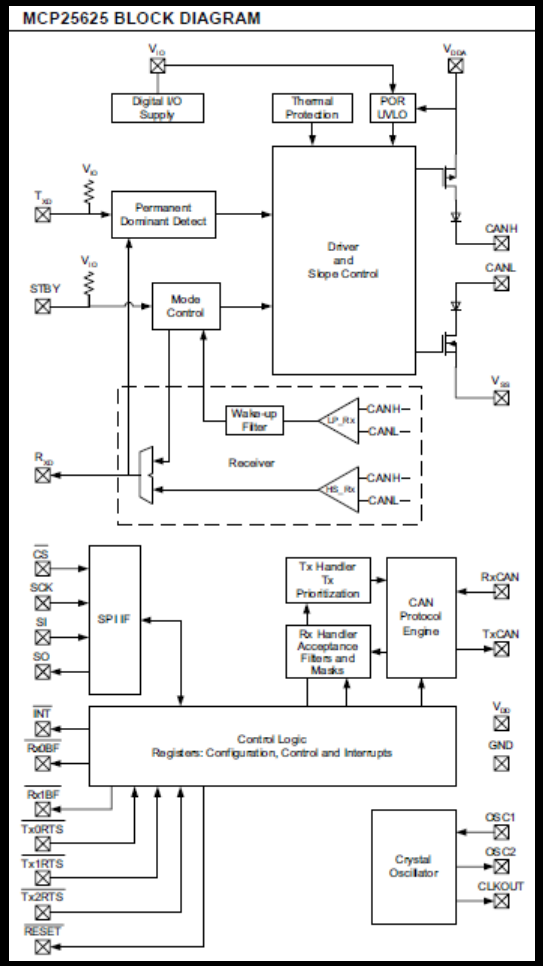
# MCP25625

# CAN Controller + Transceiver

# Introducción

El MCP25625 es un circuito integrado para manejo de CAN con las siguientes características:

- Controlador + *transceiver*.
- Alimentación digital y CAN independiente.
- Comunicación SPI.
- 3 *buffers* de transmisión.
- 2 *buffers* de recepción.
- Filtrado de recepción de mensajes.



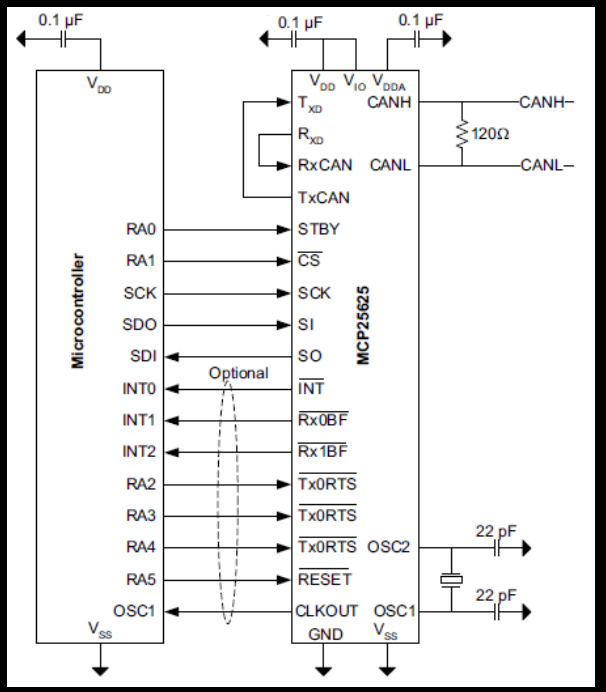
# Conexión

Microcontrolador – MCP25625:

- Alimentación (2): GND y VIO (3,3V)
- Comunicación SPI (4): /CS, CLK, MOSI y MISO
- Opcional: STBY, INT, RXnBF, TXmRTS, RESET y CLKOUT

MCP25625 – CAN bus:

- Alimentación (2): GND y VDDA (5V)
- CAN signal (2): CANH y CANL



# Driver: Mapa de Registros

El MCP25625 se controla mediante una serie de registros internos (similar a un periférico).

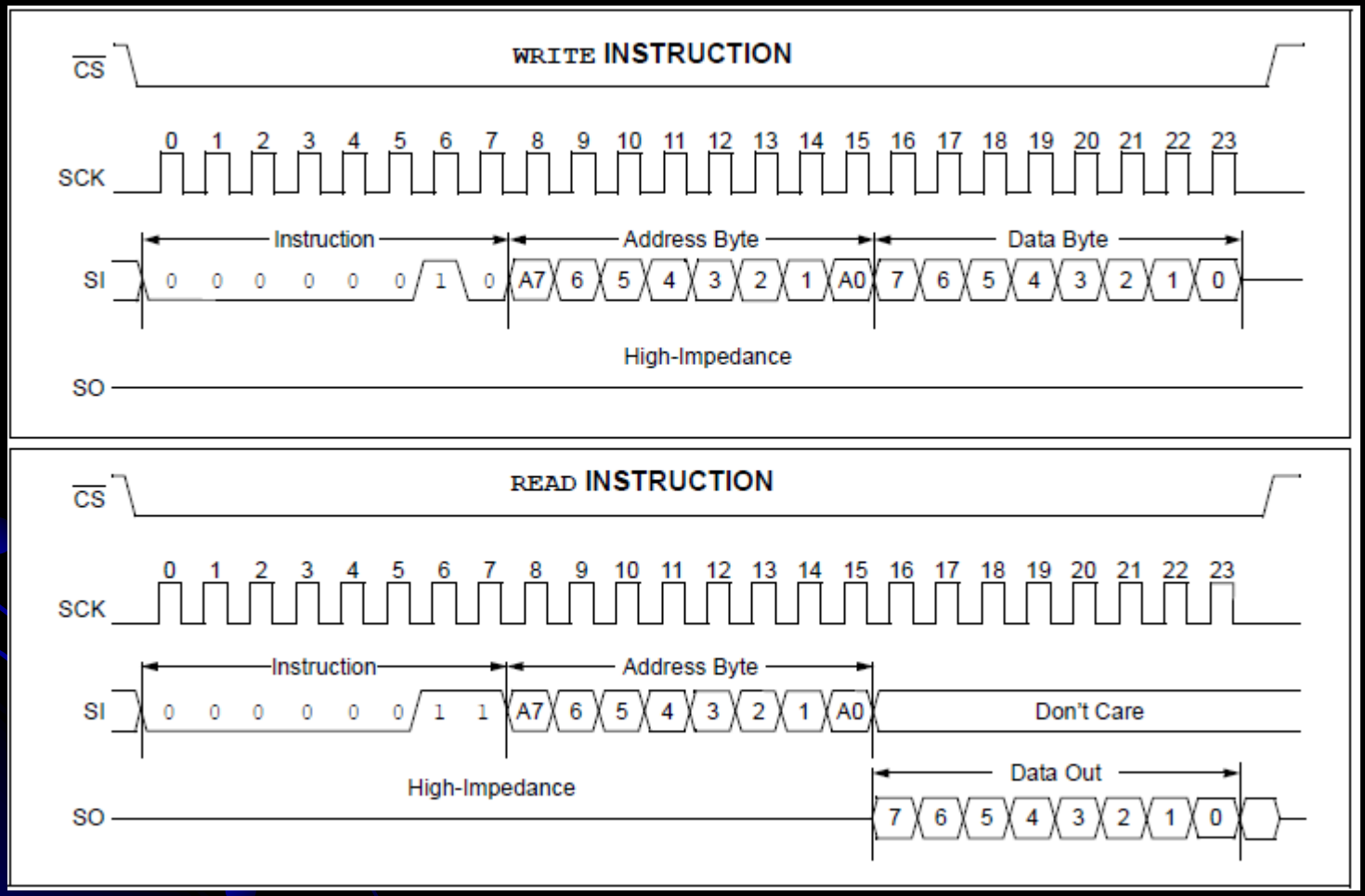
**TABLE 4-1: CAN CONTROLLER REGISTER MAP(1)**

| Lower Address Bits | Higher Order Address Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0000 xxxx | 0001 xxxx | 0010 xxxx | 0011 xxxx | 0100 xxxx | 0101 xxxx | 0110 xxxx | 0111 xxxx |
| 0000 | RXF0SIDH | RXF3SIDH | RXM0SIDH | TXB0CTRL | TXB1CTRL | TXB2CTRL | RXB0CTRL | RXB1CTRL |
| 0001 | RXF0SIDL | RXF3SIDL | RXM0SIDL | TXB0SIDH | TXB1SIDH | TXB2SIDH | RXB0SIDH | RXB1SIDH |
| 0010 | RXF0EID8 | RXF3EID8 | RXM0EID8 | TXB0SIDL | TXB1SIDL | TXB2SIDL | RXB0SIDL | RXB1SIDL |
| 0011 | RXF0EID0 | RXF3EID0 | RXM0EID0 | TXB0EID8 | TXB1EID8 | TXB2EID8 | RXB0EID8 | RXB1EID8 |
| 0100 | RXF1SIDH | RXF4SIDH | RXM1SIDH | TXB0EID0 | TXB1EID0 | TXB2EID0 | RXB0EID0 | RXB1EID0 |
| 0101 | RXF1SIDL | RXF4SIDL | RXM1SIDL | TXB0DLC | TXB1DLC | TXB2DLC | RXB0DLC | RXB1DLC |
| 0110 | RXF1EID8 | RXF4EID8 | RXM1EID8 | TXB0D0 | TXB1D0 | TXB2D0 | RXB0D0 | RXB1D0 |
| 0111 | RXF1EID0 | RXF4EID0 | RXM1EID0 | TXB0D1 | TXB1D1 | TXB2D1 | RXB0D1 | RXB1D1 |
| 1000 | RXF2SIDH | RXF5SIDH | CNF3 | TXB0D2 | TXB1D2 | TXB2D2 | RXB0D2 | RXB1D2 |
| 1001 | RXF2SIDL | RXF5SIDL | CNF2 | TXB0D3 | TXB1D3 | TXB2D3 | RXB0D3 | RXB1D3 |
| 1010 | RXF2EID8 | RXF5EID8 | CNF1 | TXB0D4 | TXB1D4 | TXB2D4 | RXB0D4 | RXB1D4 |
| 1011 | RXF2EID0 | RXF5EID0 | CANINTE | TXB0D5 | TXB1D5 | TXB2D5 | RXB0D5 | RXB1D5 |
| 1100 | BFPCTRL | TEC | CANINTF | TXB0D6 | TXB1D6 | TXB2D6 | RXB0D6 | RXB1D6 |
| 1101 | TXRTSCTRL | REC | EFLG | TXB0D7 | TXB1D7 | TXB2D7 | RXB0D7 | RXB1D7 |
| 1110 | CANSTAT | CANSTAT | CANSTAT | CANSTAT | CANSTAT | CANSTAT | CANSTAT | CANSTAT |
| 1111 | CANCTRL | CANCTRL | CANCTRL | CANCTRL | CANCTRL | CANCTRL | CANCTRL | CANCTRL |

**Note 1:** Shaded register locations indicate that these allow the user to manipulate individual bits using the BIT MODIFY command.

# Driver: Registros R/W

Los registros pueden ser escritos o leidos mediante SPI:



# Driver: Configuración inicial

1. Inicializar SPI (modo 0,0)
2. Resetear el MCP25625 (ponerlo en Configuration Mode) (RESET pin, o RESET instruction, o registro CANCTRL)
3. Configurar el tiempo de bit (CNF1, CNF2 y CNF3, *chapter 4.4*)
4. Configurar el los filtros de recepción (*chapter 4.3*)
5. Configurar modo de recepción (RXB0CTRL y RXB1CTRL, *chapter 4.2*)
6. Borrar flags y habilitar interrupciones (CANINTF y CANINTE, *chapter 4.7*)
7. Ponerlo en Normal Mode (CANCTRL, *chapter 4.7*)

# Driver: baudrate y $t_Q$

Del *chapter 3.8*:

**EQUATION 3-2: TIME QUANTA**

$$T_Q = 2 \times (BRP<5:0> + 1) \times T_{OSC} = \frac{2 \times (BRP<5:0> + 1)}{F_{OSC}}$$

**EQUATION 3-3: $T_Q$ PER NBT**

$$\frac{NBT}{T_Q} = SYNC + PRSEG + PHSEG1 + PHSEG2$$

Del *chapter 4.4*:

| Register Name | Address (Hex) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR/RST Value |
|---|---|---|---|---|---|---|---|---|---|---|
| CNF3 | 28 | SOF | WAKFIL | — | — | — | PHSEG2<2:0> | | | 00-- -000 |
| CNF2 | 29 | BTLMODE | SAM | PHSEG1<2:0> | | | PRSEG2 | PRSEG1 | PRSEG0 | 0000 0000 |
| CNF1 | 2A | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 | 0000 0000 |

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits
$T_Q = 2 \times (BRP<5:0> + 1)/F_{OSC}$

bit 7-6 **SJW<1:0>**: Synchronization Jump Width Length bits
11 = Length = 4 x $T_Q$
10 = Length = 3 x $T_Q$
01 = Length = 2 x $T_Q$
00 = Length = 1 x $T_Q$

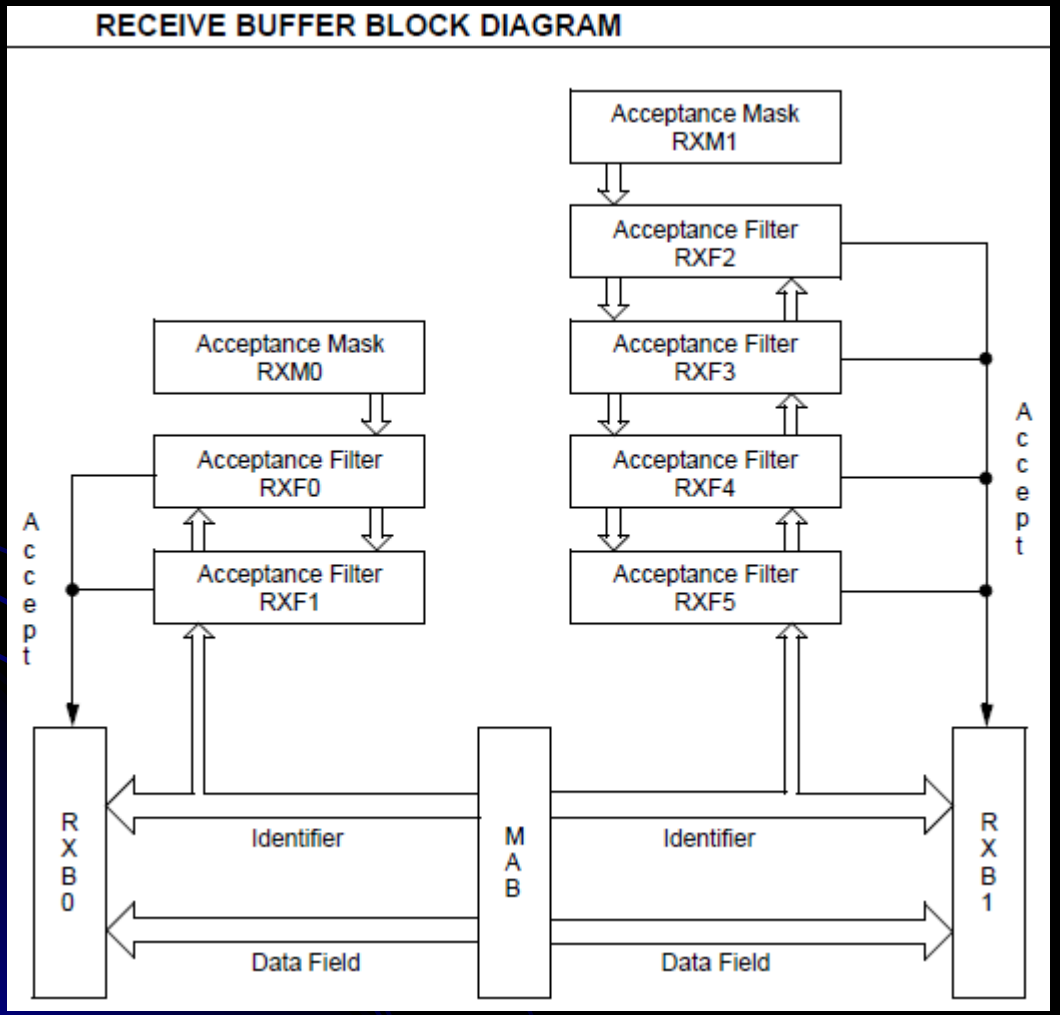
bit 5-3 **PHSEG1<2:0>**: PS1 Length bits
(PHSEG1<2:0> + 1) x $T_Q$

bit 2-0 **PRSEG<2:0>**: Propagation Segment Length bits
(PRSEG<2:0> + 1) x $T_Q$

bit 2-0 **PHSEG2<2:0>**: PS2 Length bits
(PHSEG2<2:0> + 1) x $T_Q$
Minimum valid setting for PS2 is 2 $T_Q$.

# Driver: Filtros de RX

Del *chapter 3.7*:

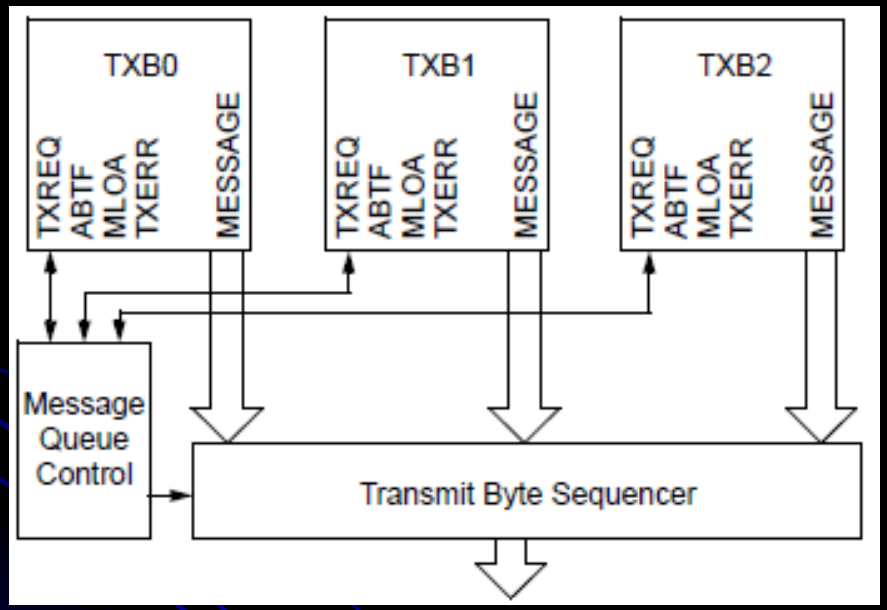



| Mask Bit n | Filter Bit n | Message Identifier Bit | Accept or Reject Bit n |
|---|---|---|---|
| 0 | x | x | Accept |
| 1 | 0 | 0 | Accept |
| 1 | 0 | 1 | Reject |
| 1 | 1 | 0 | Reject |
| 1 | 1 | 1 | Accept |

**Note:** x = Don't care.

# Driver: frame TX

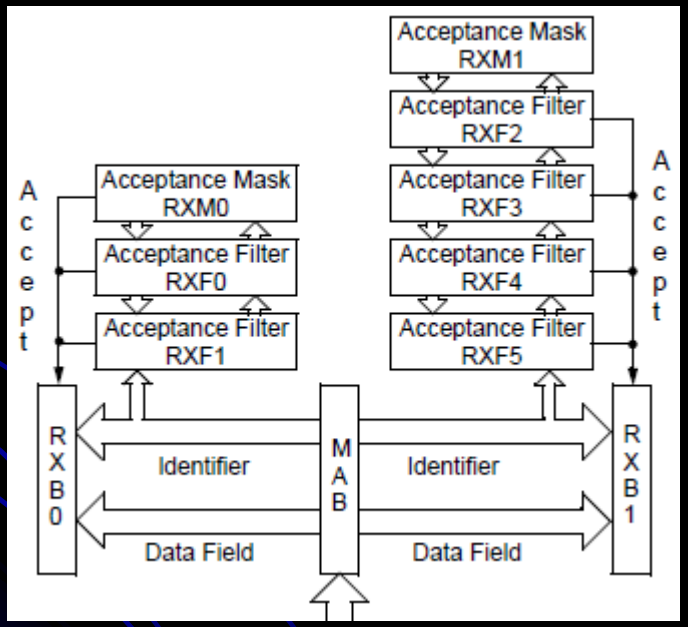
1. Buscar un TX buffer libre (TXBxCTRL.TXREQ)
2. Llenar el buffer (ID, DLC, DATA, etc.)
3. Solicitar envío del TX buffer (TXBxCTRL.TXREQ)




| TXB0CTRL | TXB1CTRL | TXB2CTRL |
|---|---|---|
| TXB0SIDH | TXB1SIDH | TXB2SIDH |
| TXB0SIDL | TXB1SIDL | TXB2SIDL |
| TXB0EID8 | TXB1EID8 | TXB2EID8 |
| TXB0EID0 | TXB1EID0 | TXB2EID0 |
| TXB0DLC | TXB1DLC | TXB2DLC |
| TXB0D0 | TXB1D0 | TXB2D0 |
| TXB0D1 | TXB1D1 | TXB2D1 |
| TXB0D2 | TXB1D2 | TXB2D2 |
| TXB0D3 | TXB1D3 | TXB2D3 |
| TXB0D4 | TXB1D4 | TXB2D4 |
| TXB0D5 | TXB1D5 | TXB2D5 |
| TXB0D6 | TXB1D6 | TXB2D6 |
| TXB0D7 | TXB1D7 | TXB2D7 |

# Driver: frame RX

1. Comprobar que ocurrió un hit (llegó un mensaje que pasó los filtros) (CANINTF.RXnIF)
2. Leer información del RX buffer (ID, DLC, DATA, etc.)
3. Borrar flag de RX buffer lleno (CANINTF.RXnIF)




| RXB0CTRL | RXB1CTRL |
|---|---|
| RXB0SIDH | RXB1SIDH |
| RXB0SIDL | RXB1SIDL |
| RXB0EID8 | RXB1EID8 |
| RXB0EID0 | RXB1EID0 |
| RXB0DLC | RXB1DLC |
| RXB0D0 | RXB1D0 |
| RXB0D1 | RXB1D1 |
| RXB0D2 | RXB1D2 |
| RXB0D3 | RXB1D3 |
| RXB0D4 | RXB1D4 |
| RXB0D5 | RXB1D5 |
| RXB0D6 | RXB1D6 |
| RXB0D7 | RXB1D7 |

# Referencias

- MCP25625 Official Website: www.microchip.com/wwwproducts/en/MCP25625
- MCP25625 CAN Controller with Integrated Transceiver Datasheet: ww1.microchip.com/downloads/en/DeviceDoc/20005282B.pdf
- MCP25625 PICtail Plus Daughter Board User Guide: ww1.microchip.com/downloads/en/DeviceDoc/50002414A.pdf