Signals-From-Noise
Single-Bit DACs in a Nutshell - Part I: DAC Basics
by Dave Van Ess, Principal Application Engineer, Cypress Semiconductor

Many embedded applications require generating analog outputs under digital control. It may be a dc reference voltage or an ac signal to stimulate transducers. It may be a reconstructed voice signal for some wireless application. The applications are endless. This function requires a Digital-to-Analog Converter (DAC).

DACs are cool! They allow analog signals to be generated under CPU control. The name even sounds cool. DAC, the name brings up images of a Clive Cussler adventure. DAC Bit, man of finite resolution!

The number of DACs that can be squeezed on to single chip systems is always limited, making them a dear resource. One solution is to use onboard digital resources and firmware, along with simple filters to build single-bit DACs. This article will explain the concept of single-bit DACs; different techniques to construct them; and the benefits and consequences of each type.

A DAC, in its simplest form, is circuitry to generate an output that is a percentage of a reference. A simple four bit implementation is shown in Fig. 1.

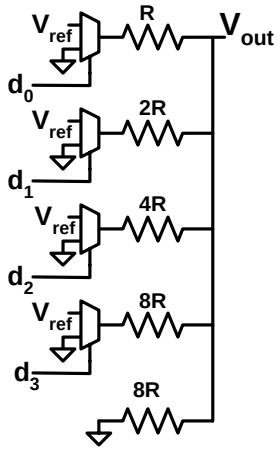

Fig. 1: Four-Bit DAC

The following defines the output voltage:

$$V_{out} = \frac{d_0 V_{ref}}{2} + \frac{d_1 V_{ref}}{4} + \frac{d_2 V_{ref}}{8} + \frac{d_3 V_{ref}}{16} \qquad (1)$$

If it is acceptable to use the supply voltage as the reference, then the input multiplexers can be replaced with digital outputs from the CPU. This simplifies the design to four digital output pins and five resistors as shown in Fig.2.

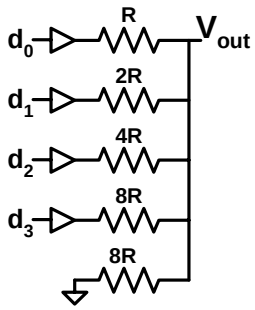

Fig. 2: Ratiometric Four-Bit DAC

When the supply voltage is used as the reference it is known as *ratiometric*. This may sound cool but it is just really just clever marketing! It makes not having a real reference sound like a feature. Who would want buy a *10-bit serial-input, no-real-reference DAC*?

Within reason, each extra bit of resolution requires only one extra resistor and a port pin to drive it. Resistor tolerance is going to become a problem. If implemented with 1% resistors, resolution is limited to about 6 bits. Each added resistor is double the value of the previous resistor. The tenth bit is 1024R. At some point the ratio of the resistors becomes impracticality large. This can be solved using the topology shown in Fig. 3.

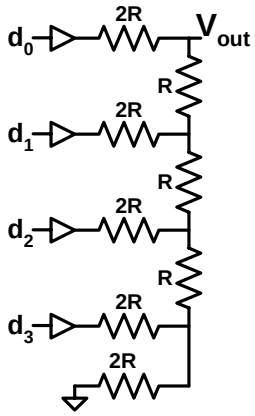

Fig. 3: R - 2R Ladder Four-Bit DAC

This is called an R - 2R ladder. It has the advantage that the resistor ratio never gets larger than two. If the R value is constructed with two parallel 2R resistors, then only a single value of resistor is needed. Generally 1% resistors from the same reel hold a relative tolerance better than ½%. This increases the resolution limit to 7 bits but requires three resistors per bit. To be accurate this topology really should be called a ½R - R ladder DAC. However this was rejected as some digital engineers could not fathom the idea of a number between zero and one.

So far the DACs discussed generate a particular ratio of the reference, 100% of the time. For example when an 8-bit DAC with a 5-V reference is set to 37 the output is 0.72 V -- 5 V * (37 ÷ 256).

Suppose instead of supplying 14.5% of the reference 100% of the time, one could supply 100% of the reference 14.5% of the time. Just such a topology is shown in Fig.4

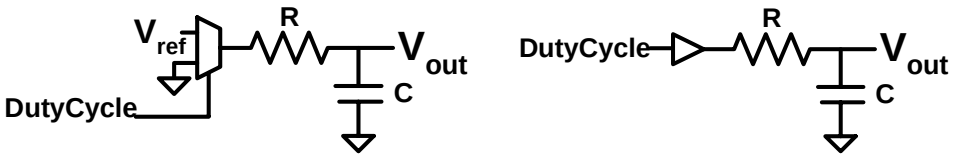

Fig. 4: Single-Bit And Ratiometric Single-Bit DAC

The output voltage is V_{ref} * DutyCycle. Again, if it is acceptable to use the supply voltage as the reference, then the input multiplexer can be replaced by a single digital output from the CPU. This simplifies the design to a single digital output pin and a filter. These examples represent the filter as single-pole RC but the filtering could be the flywheel effect of a motor or the current integrating effect of an inductor. Any system component that has a slower response than the generated output frequency acts as the filter.

What waveform is ideal for generating a duty cycle? Well this is the stuff theses are made of. There are many ways to generate a duty cycle. Each has particular advantages. We'll close off this first section with the simplest method and leave the more advanced techniques for the next time.

Pulse-Width Modulator (PWM)

One of the simplest ways to generate a duty cycle is to use a PWM. Many microcontrollers already are equipped with as least one and many in cases, several of them. A block diagram of a PWM is shown in Fig. 5.

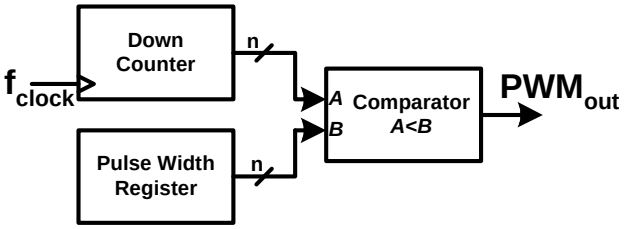

Fig. 5: PWM Block Diagram

The hardware consisted of a down counter with some period and a register to store a pulse-width value. The comparator will go high whenever the counter's value is less the pulse-width value. For a period of 256, the count will be down from 255 to zero. If the pulse-width value is 128 then the comparator output will be high when the counter output

is down from 127 to zero: 128 counts. The equations for the duty cycle and output frequency are:

$$dc = \frac{PulseWidth}{Period} \qquad f_{out} = \frac{f_{clock}}{Period}$$

For PWMs, the output frequency is independent of the pulse-width. The plots in Fig. 6 are for two PWMs.

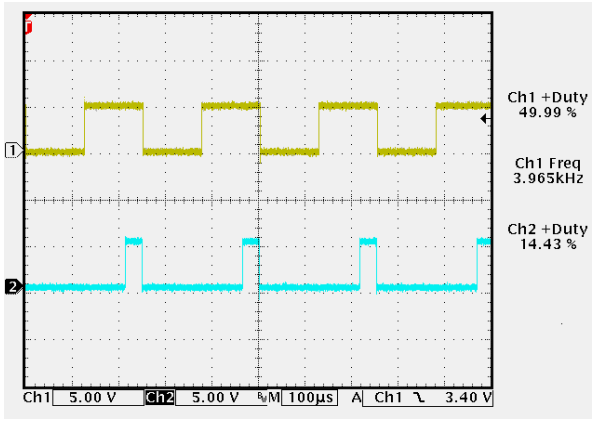

Fig. 6: PWM Waveforms: 50% And 14.5% Duty Cycles

Both have a period of 256 and input clock of 1 MHz, resulting in both having an output frequency of 3.9 kHz. The top trace shows a PWM with its pulse width set to 128. This trace verifies that this is a 50% duty cycle. The bottom trace is for a PWM with a pulse width of 37. It has the same output frequency but has a duty cycle of 14.5% (37/256). Again the trace shows a signal that is high about 1/7th of the time. A spectral plot of the two signals is shown in Fig. 7.

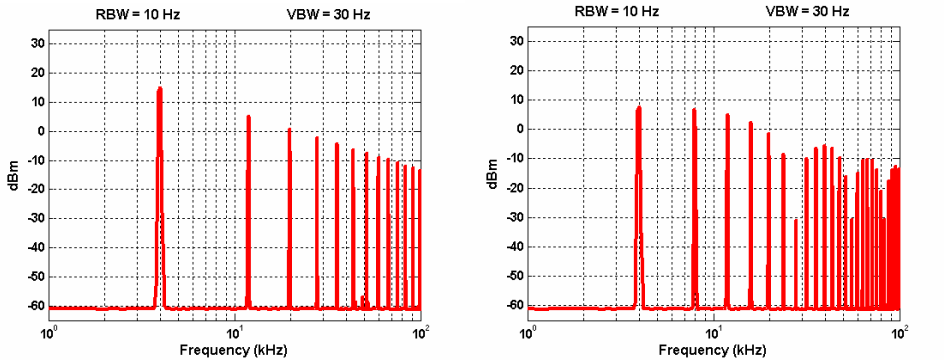

Fig. 7: PWM Spectral Plots: 50% and 14.5% Duty Cycles

It is apparent that there are significant harmonics in these outputs. It will require filtering to remove them. Although relatively easy to build, PWMs suffer from significant harmonic generation that is at a relatively low frequency. Given a constant clock frequency, a PWM with finer resolution (larger period) has a lower output frequency. The

general solution is to increase the clock frequency. The maximum operating frequency for the counter and comparator limits the practical resolution.

We'll discuss several other techniques that get around these limitations in the concluding installment of this article.

About The Author

Dave Van Ess is a Principal Applications Engineer at Cypress Semiconductor. He is an electrical engineer with experience in hardware, software, and analog design. Dave joined Cypress in 2000. He has nine patents for medical systems, signal processing design, and PSoC digital block enhancements. He has written numerous User Modules, application notes, and articles. He graduated sigma cum barely with his BSEE from the University of California, Berkeley, 1977.

An engineer by training, a poet by temperament, an outlaw in Nebraska, and a heck of a nice guy, Dave has worked in many different industries. His work experience includes test and measurement equipment, measurement and control systems for high-energy physics research, and underwater acoustic transmitters and receivers deployed in open sea and artic ice fields. Electrons fear him! Women revere him!

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