Signals-from-Noise
Single-Bit DACs in a Nutshell - Part II: Advanced DAC Techniques
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In our first installment, "DAC Basics" http://www.analogZONE.com/iot_0904.pdf we explored how traditional resistor ladder networks can be replaced with simpler single-bit and ratiometric single-bit DAC elements and how to drive them with a pulse-width modulated (PWM) waveform. In this concluding installment, we'll look at three other ways to drive these networks. Each will have example oscilloscope waveforms and spectral plots for duty cycles of 50% and 14.5%.

Delta-Sigma (Δ-Σ) Modulation (DSM)

PWMs reduce the number of transitions to the smallest possible value. (One high and one low per counter cycle.) DSM is a technique that increases the number of transitions to the largest possible value. For the same clock frequency, the harmonics are pushed farther out making it easier to filter them. A block diagram of a DSM is shown (Fig. 8).

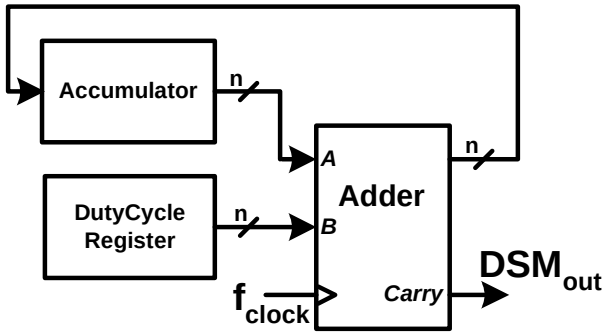

Fig. 8: Delta-Sigma Modulator Block Diagram

The duty cycle value is added to an accumulated value when the adder overflows the output is high. For example, constantly adding 128 to an 8-bit adder causes a carry every other time. Constantly adding 64 results in a carry one in four times. Adding 63 results in a carry one in four times, most of the time, but occasionally a carry one in five times. The equations for the duty cycle and output frequency are:

$$dc = \frac{DutyCycleValue}{AccumWidth} \qquad f_{out} = \begin{cases} dc \cdot f_{clock} & : dc \le 0.5 \\ (1-dc) \cdot f_{clock} & : dc > 0.5 \end{cases}$$

The output frequency is no longer set by the counter period. Independent of the adder width, if the duty cycle is limited to a range of 10% to 90%, the output frequency is guaranteed to be no smaller than 1/10th the clock frequency. The plots (Fig. 9) are for two DSMs.

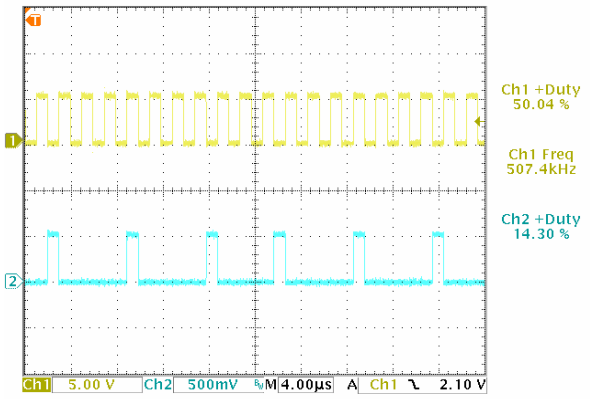

Fig. 9: DSM Waveforms: 50% And 14.5% Duty Cycles

Both have an adder width of 256 and input clock of 1 MHz. The top trace shows a DSM with its duty-cycle value set to 128. This results in an output with a 50% duty cycle and an output frequency of 500 kHz. The bottom trace is for a DSM with its duty-cycle value set to 37. This results in an output high one part in seven most of the time, and occasionally one part in six, for an average output frequency of 145 kHz (1 MHz * 37 ÷ 256). The generated harmonics are pushed well past the 3.9 kHz of the PWM example. A spectral plot of the two signals (Fig. 10) confirms this.

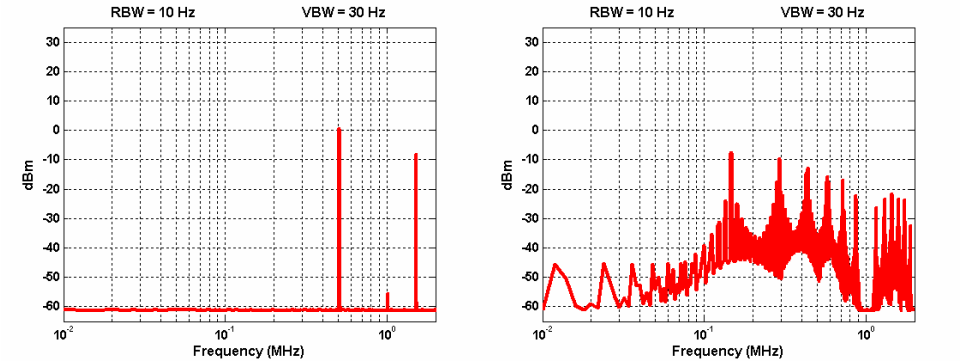

Fig. 10: DSM Spectral Plots: 50% And 14.5% Duty Cycles

Note: The frequency components of the 37/256 duty cycle DMS is a mixture of 1 MHz ÷ 6 and 1 MHz ÷ 7. (256/37 = 6.92)

One chief problem with this solution is that no micro-controller comes with this type of hardware. It could be built with programmable logic or implemented with software. The Cypress Semiconductor CY8C27443 programmable system on a chip has eight PWMs, each capable of running with a clock frequency as high as 48 MHz while using zero CPU overhead. Implementing a software DSM in the same device requires 100% of the CPU for a clock frequency of 1 MHz.

Pseudo-Random Modulation (PRM)

PRM is a variation of pulse-width modulation where the down counter is replaced with a pseudo-random counter (see Fig. 11).

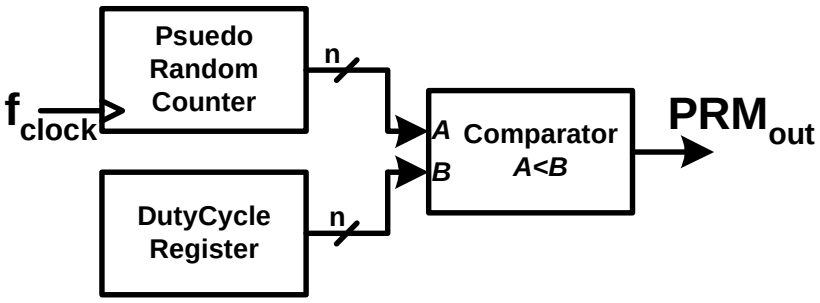

Fig. 11: Pseudo-Random Modulator Block Diagram

The comparator is still high whenever the counter is below the duty cycle value It is just that the counter no longer counts linearly. The output is still high the same number of counts it just that they are now (pseudo) randomly dispersed within the counter period. As with the delta sigma modulator the output frequency is not dependent on the counter period. The output frequency is higher but not as high as the DSM. The random nature of the output keeps it frequency to approximately half of what it would be for DSM. The equations for the duty cycle and output frequency are shown below.

$$dc = \frac{DutyCycleValue}{Period} \qquad f_{out} \approx \begin{cases} \frac{1}{2} dc \cdot f_{clock} & : dc \le 0.5 \\ \frac{1}{2}(1-dc) \cdot f_{clock} & : dc > 0.5 \end{cases}$$

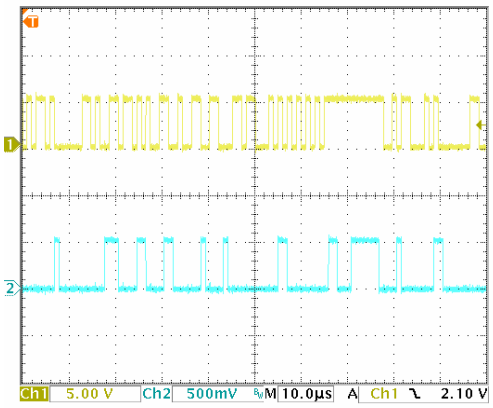

Fig. 12: PRM Waveforms: 50% And 14.5% Duty Cycles

Fig. 12 shows two PRM waveforms where both have a counter width of 256 and input clock of 1 MHz. The top trace shows a PRM with its duty-cycle value set to 128. This results in a very random looking output with a 50% average duty cycle and an output frequency of approximately 250 kHz. The bottom trace is for a DSM with its duty-cycle value set to 37. This results in a signal that is high 14.5% of the time. Its output frequency

is around 172 kHz. Being nearly random there is not much harmonic content at any particular frequency. A spectral plot (Fig. 13) of the two signals confirms this.

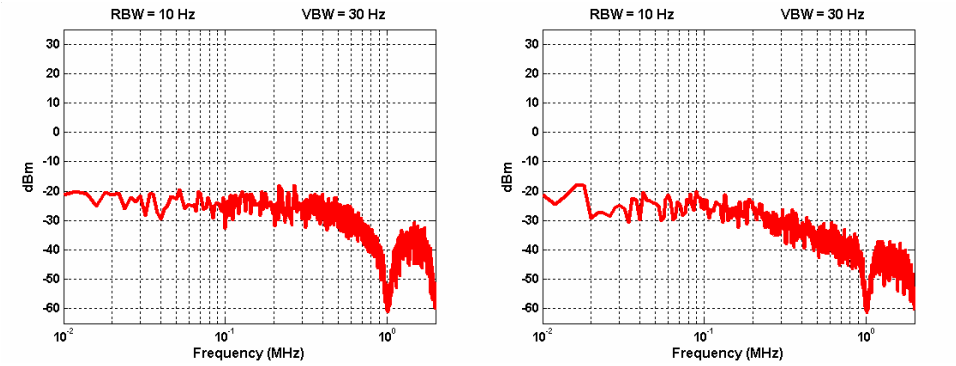

Fig. 13: PRM Spectral Plots: 50% And 14.5% Duty Cycles

Although not pushing the harmonic frequencies as high as DSM there are advantages to the random nature of the output. The PSoC CY8C27443 is capable of implementing up to eight of these modulators.

Dithered-Pulse-Width Modulators (DPWM)

So far three different modulation techniques have been shown. The second and third reduce the effects of harmonics by pushing them up in frequency making them easier to remove. They do this by increasing the output frequency. This can be a problem where there is cost to high-frequency switching and the components cannot switch above a certain frequency, or there is an energy loss associated with switching. (Battery chargers are a good example: there is loss every time the power FET is switched.). A fourth option is randomize the clock feeding a PWM (see Fig. 14).

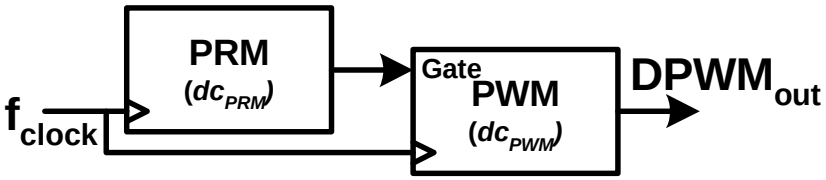

Fig. 14: Dither-Pulse-Width Modulator (DPWM) Block Diagram

Normally the output frequency of a PWM is the clock divided by the period. 1 MHz clocking an 8-bit PWM has an output frequency of 3.9 kHz. Building a dithered-PWM requires using the gate input of the PWM. When the gate is high the PWM clock is enabled and it generates an output frequency of 3.9 kHz. When the gate is low the clock is disabled and the output frequency is zero. If the gate input has some duty cycle then the output is proportional to it.

The equations for the duty cycle and output frequency are:

$$dc_{PRM} = \frac{DutyCycleValue_{PRM}}{Period_{PRM}} \quad dc_{PWM} = \frac{PulseWidth_{PWM}}{Period_{PRM}} \quad f_{out} = dc_{PRM} \frac{f_{clock}}{Period_{PWM}}$$

For a 2 MHz clock and a pseudo-random duty cycle of 50%, the 8-bit PWM has an average output frequency of 3.9 kHz (2 MHz * ½*/256). It is average because the random nature of the PRM output causes a fluctuation frequency. For these particular parameters the change in output frequency is ±10% (see Fig. 15).

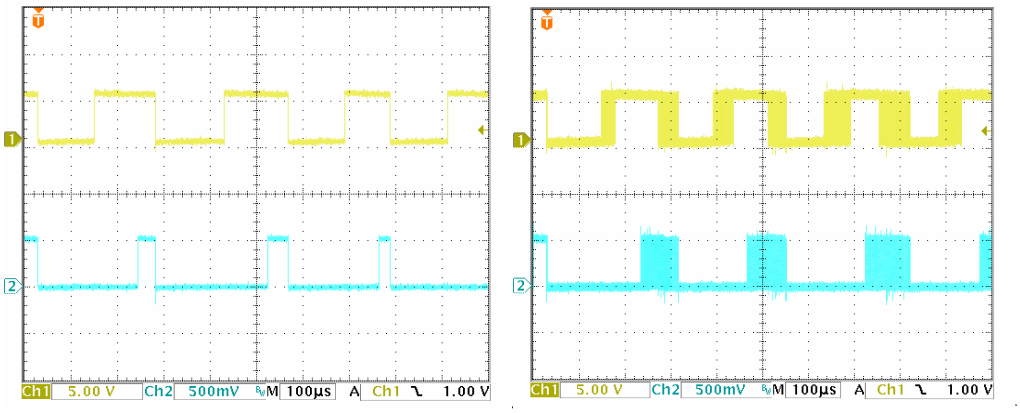

Fig. 15: DPWM Waveforms: 50% And 14.5% Duty Cycles

With this much frequency shift the spectrum will no longer be harmonics at fixed frequency. This dither effect smears them out over a wider area (Fig. 16).

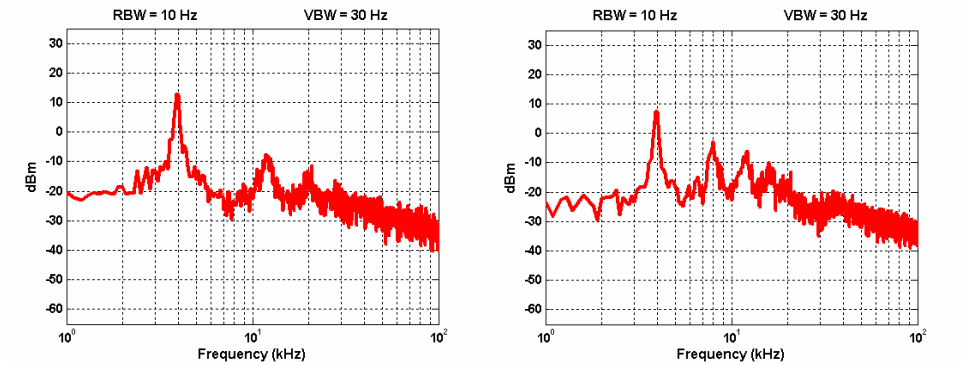

Fig. 16: DPWM Spectral Plots: 50% And 14.5% Duty Cycles

Comparing these plots with those for a regular PWM, the peak harmonic noise is down maybe 3 dB and the other harmonics are significantly reduced -- but it comes at the expense of the overall noise floor. Another feature is that only changing the PRM duty cycle allows for fine tuning of the average output frequency. For example, the average output frequency is 3.9 kHz. Changing the PRM duty cycle to 64% shifts the average output frequency to 5 kHz.

DACs are precious resources that are frequently completely used. It may become necessary to fabricate your own with on-chip digital resources or firmware. Four examples of single-bit DACs have been shown; the decision on which to use is dependent on your unique system requirements and available resources.

About The Author

Dave Van Ess is a Principal Applications Engineer at Cypress Semiconductor. He is an electrical engineer with experience in hardware, software, and analog design. Dave joined Cypress in 2000. He has nine patents for medical systems, signal processing design, and PSoC digital block enhancements. He has written numerous User Modules, application notes, and articles. He graduated sigma cum barely with his BSEE from the University of California, Berkeley, 1977.

An engineer by training, a poet by temperament, an outlaw in Nebraska, and a heck of a nice guy, Dave has worked in many different industries. His work experience includes test and measurement equipment, measurement and control systems for high-energy physics research, and underwater acoustic transmitters and receivers deployed in open sea and artic ice fields. Electrons fear him! Women revere him!

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