Circuits Lab 7

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1 Experiment 1

For this experiment we constructed the pMOS differential pair. We set the bias transistor to be just at or below threshold. We then measured the I1 and I2 for V2 values of 0.5V, 1.5V, and 2.5V. We then constructed a plot showing I1, I2, I1 I2, and I1 + I2, as a function of V1 V2 for all three values of V2 that we used. This plot is shown in figure Figure 1. These current–voltage characteristics do not change significantly at all for different values at V2.

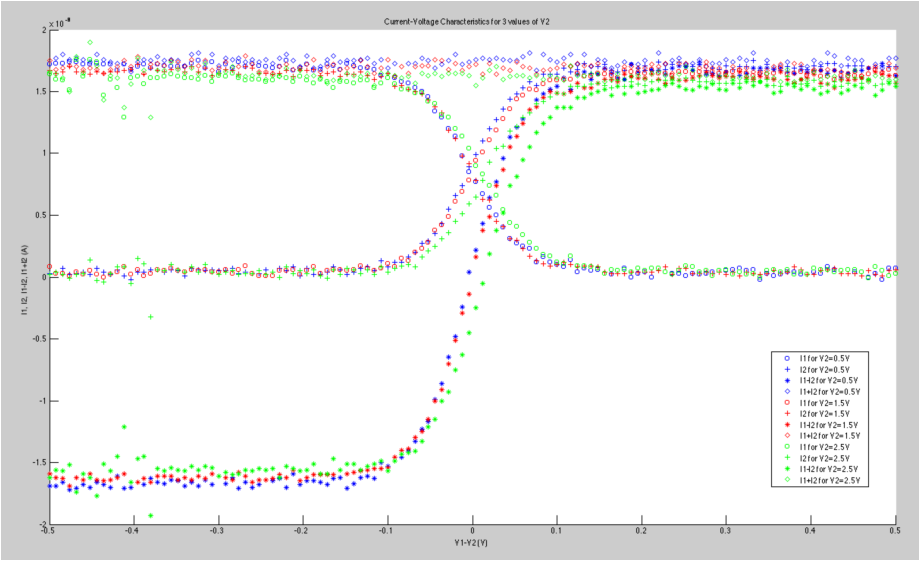

Figure 1: A plot showing, I1, I2, I1-I2, I1+I2 for three different values of V2 for a differential pair

Figure 2 on the next page shows the Common-Source Node voltage for all three configurations as a function of the difference in the input voltages. While V1 is smaller V2, V increases with V1. It plateaus when it passes V2.

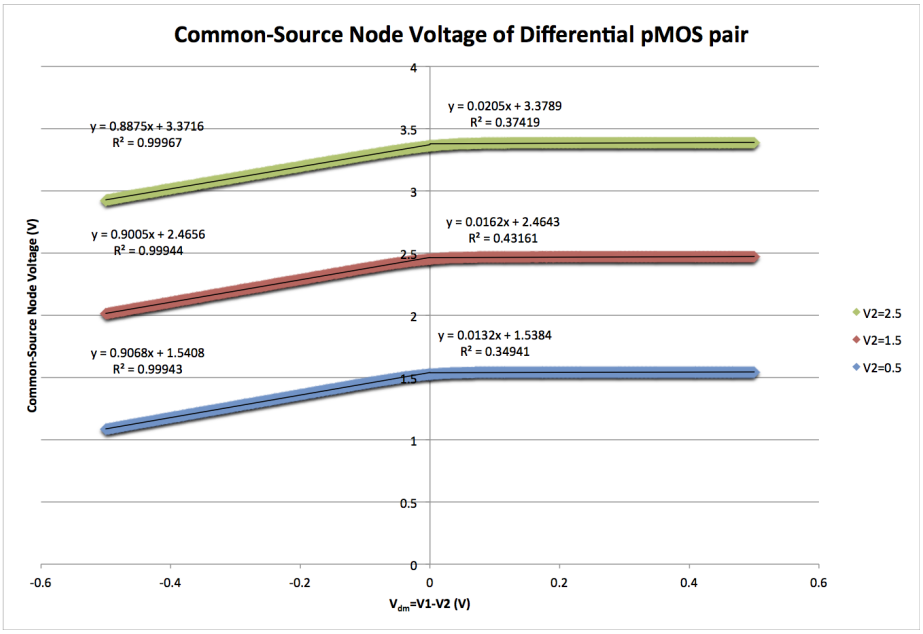

Figure 2: V versus V1-V2 for all three values of V2 tested

We also repeated the experiment for $V_b = 1.5V$, which insured the bias current was well above threshold. The graphs are shown in Figure 3 on the following page and Figure 4 on the next page. The total output current no longer stays constant and the individuals ones are linear.

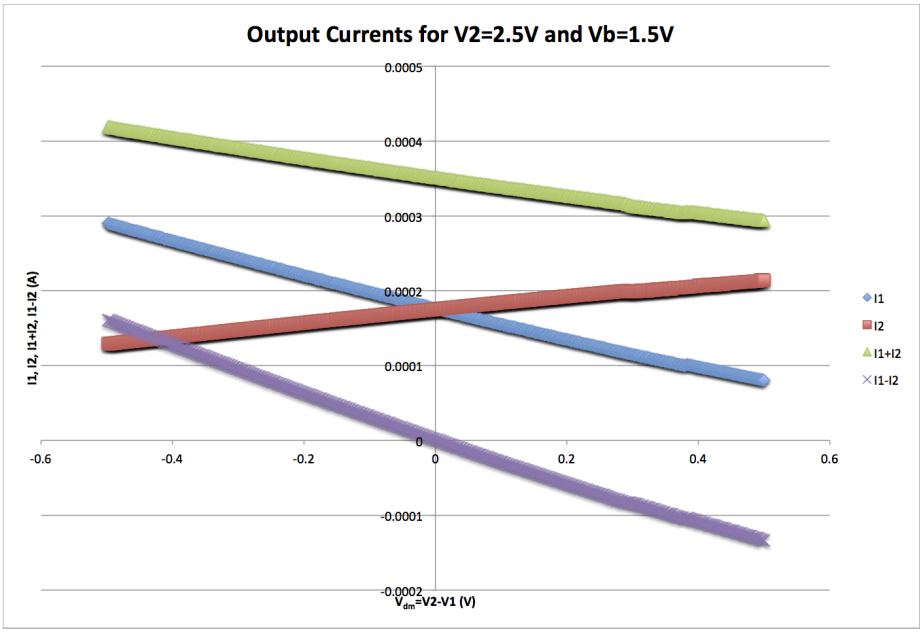

Figure 3: Output current versus V1-V2 with above-threshold bias current

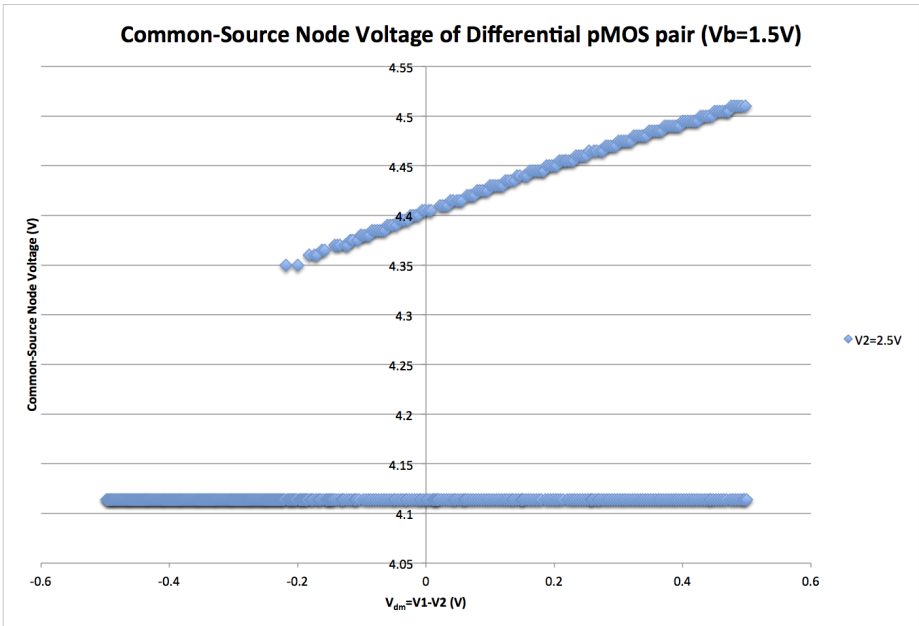

Figure 4: V versus V1-V2 with above-threshold bias current