Circuits Lab 6

Thomas Nattestad and Dimitar Dimitrov

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1 Experiment 1: Transistor Matching

We swept the gate voltage and measured the current-voltage characteristics for each of the 4 chip nMOS transistors by collecting 500 points between 0 and 5 volts. We extracted values for I_s V_T κ as shown below:

	I_s	V_T	κ
T1	$2.6149e-6A$	.55713 V	.70243
T2	$3.5518e-6A$	.56059 V	.59690
T3	$3.5974e-6A$	.56126 V	.59468
T4	$2.4483e-6A$	.55304 V	.70956

We next constructed a semilog plot, shown in figure Figure 1 on page 3 with EKV fits for the data. Since the data is so incredibly dense and very well matched, it is basically impossible to see distinct lines, since they are basically all on top of one another.

We then constructed a semilog plot showing the percentage difference between each transistor's channel current and the mean value of all four channel currents as a function of the mean value of all four channel currents, as shown in figure Figure 2 on page 3

The 4 transistors are very well matched. The percent difference from mean starts very high for extremely low current values but then drops almost immediately to very low values of no more than a few percent. The percent difference from mean is only a few percent after .0001 Amps. The percent difference seems to be much lower for current values in the strong inversion region.

2 Experiment 2: MOS Transistors in Series and Parallel

We used the same ALD1106 quad nMOS array we used in Experiment 1, with the V- (common base) and V+ pins tied to the ground and 5V probes of the SMU, respectively. We used a python script to collect 6 sets of channel currents, each over 501 gate voltages, evenly spaced from 0V to 5V. For the first two sets, we tied the source of nMOS1 to ground and set the drain voltage first

to to 0.010V and then to 5.000V. For the next two sets, we additionally tied the source, drain and gate of nMOS2 to the source, drain and gate of nMOS1 (forming a parallel arrangement) and repeated the same two measurements. Finally, we moved the voltage source from the nMOS1 drain to the nMOS2 drain and connected the nMOS1 drain to the nMOS2 source, keeping the nMOS1 source tied to ground and the two gates tied to the same probe as before (forming a series arrangement). We repeated the sweep for both drain voltages. All six results are graphed in Figure 3 on page 4. For the large value of V_{DS} and higher values of V_G, the series configuration consistently produced about half of the current that an individual FET produced, and the parallel configuration produced about twice that. The $\log 2$ scale on the graph helps demonstrate that. For the small value of V_{DS}, this was less consistent and at times far from true (although the order stayed "correct").

Overall the equivalences are very accurate, but only in saturation.

3 Experiment 3: MOS Current Dividers

We constructed a current divider by setting up two pairs of transistors. The first pair was connected in parallel, yielding a strength equivalent to twice the strength of a single nMOS transistor. The second pair was in series, yielding a strength equivalent to half the strength of a single nMOS transistor. Thus, the ratio of strengths was 4 and the predicted output currents were one fifth and four fifths of the input current. We set the gate voltage to about half of V_{dd} using a potentiometer for all sections of the experiment.

First we connected the sinks of the two nMOS pairs and swept a negative current from 0mA to 10mA. We tied the drains to V_{dd}. The current flowing through each drain is graphed in Figure 6 on page 7. The extracted ratios were .802 and .194, which are extremely close to the theoretical values of .8 and .2.

Next, we connected the drains instead and sourced a current. We tied the sources to ground. We measured the currents through the sources and graphed the results in Figure 7 on page 8. The extracted ratios were .783 and .161, which are fairly close to the theoretical values of .8 and .2.

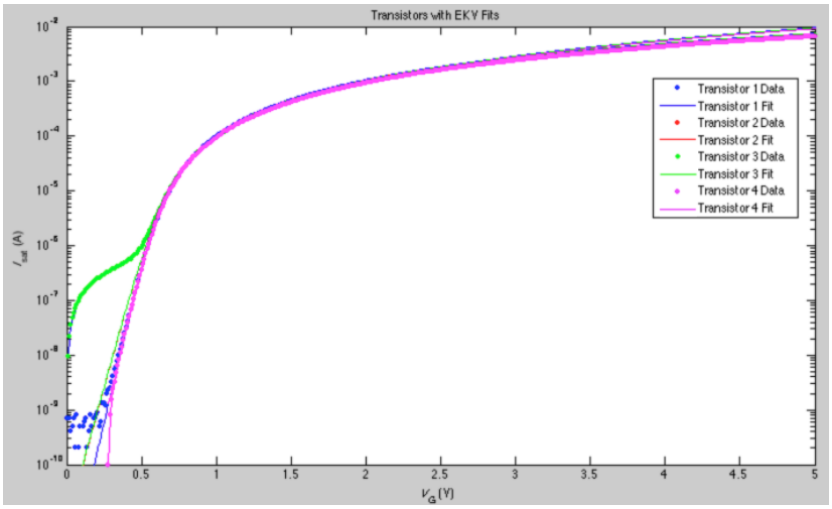

Figure 1: A semilog plot showing 4 transistors current-voltage characteristics with EKV fits for each. Note that most lines are on top of one another so are hard to distinguish

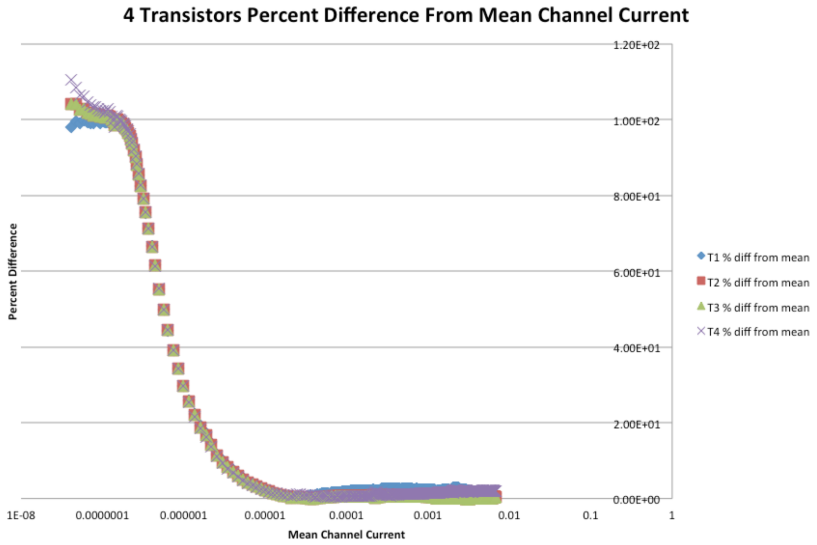

Figure 2: a semilog plot showing the percentage difference between each transistor's channel current and the mean value of all four channel currents as a function of the mean value of all four channel currents, ignoring the first 5 points of completely random noise

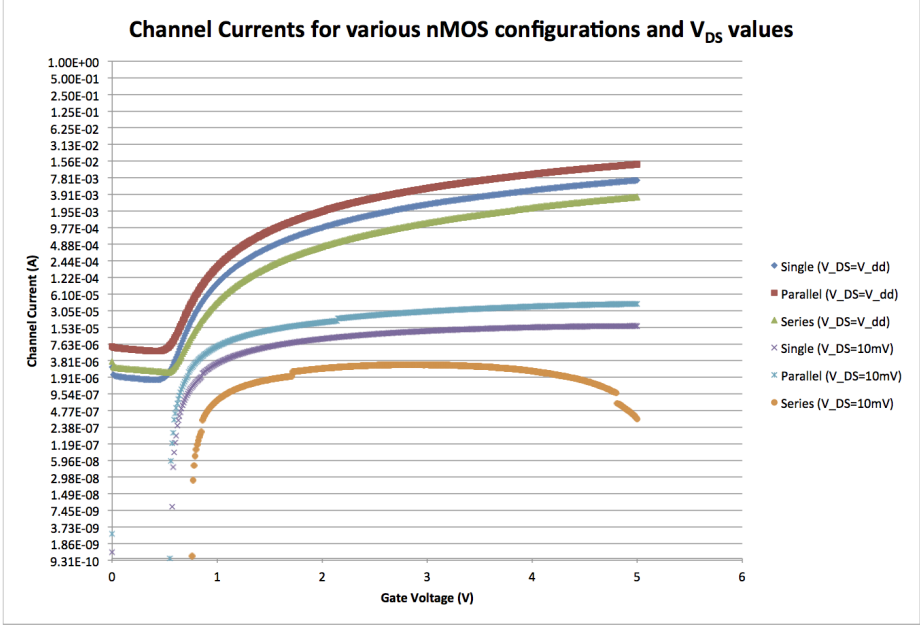

Figure 3: A semilog plot showing the the channel currents for three nMOSFET configurations (individual FET, two FETs in parallel, two FETs in series) and 2 distinct drain voltages over a 501-sample range of gate voltages (source at ground, all voltages with respect to to the base voltage).

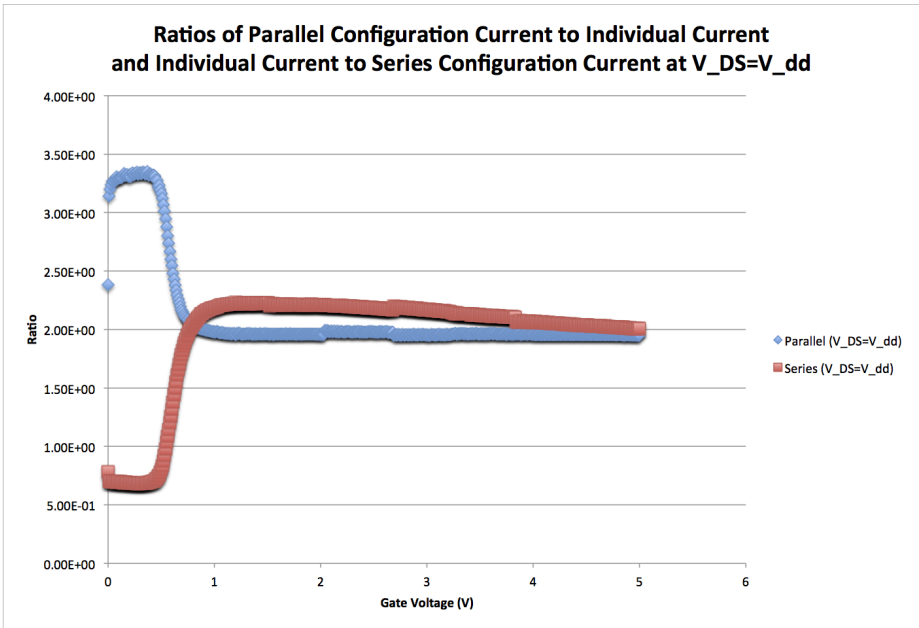

Figure 4: A plot showing the ratio of the channel current in the parallel configuration to that in an individual FET as well as the ratio of the channel current in an individual FET to that in the series configuration, both at large values of V_{DS}. Both clearly converge to the value 2, as expected.

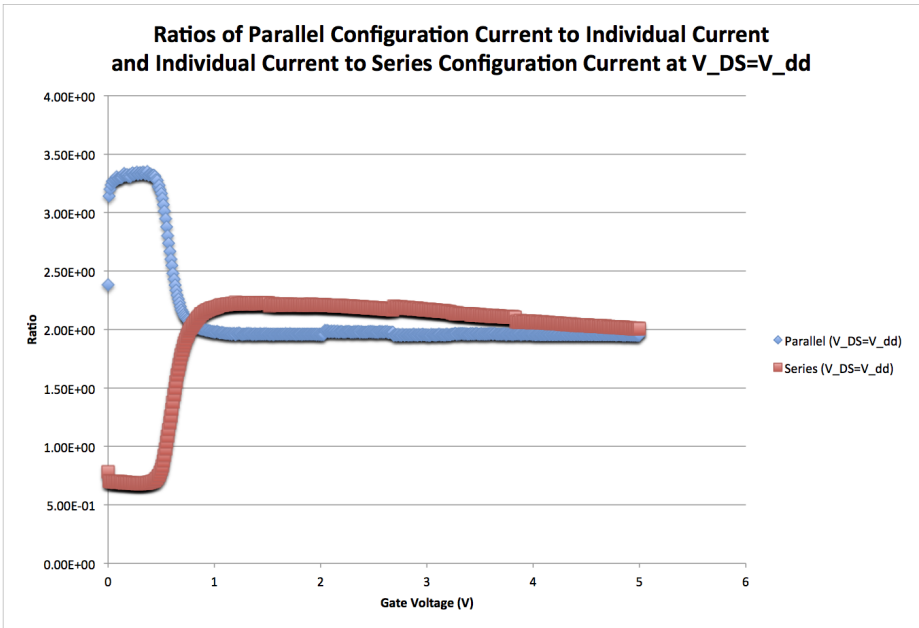

Figure 5: A plot showing the ratio of the channel current in the parallel configuration to that in an individual FET as well as the ratio of the channel current in an individual FET to that in the series configuration, both at small values of V_{DS}. The former stays closer to the predicted value of 2, but both vary wildly.

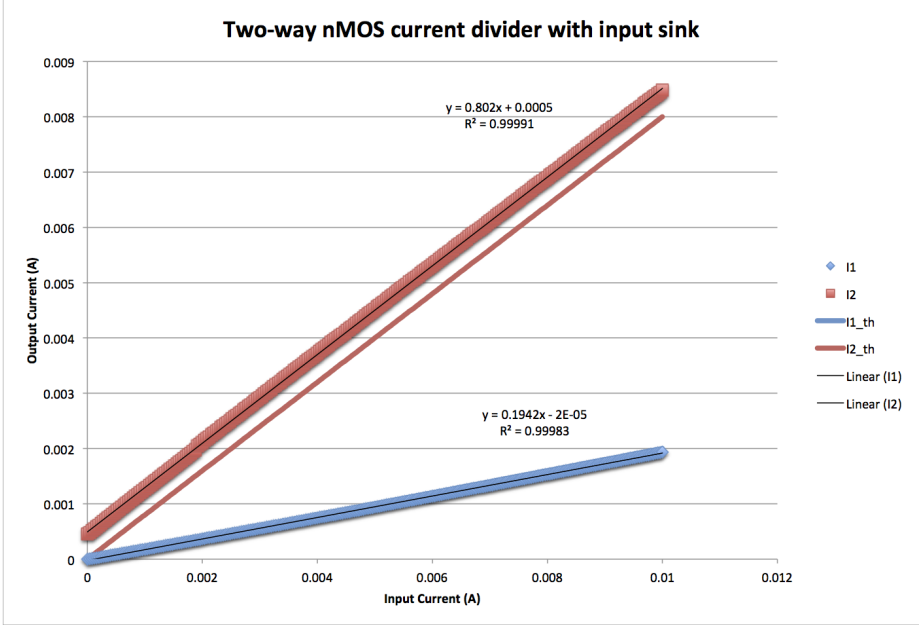

Figure 6: Two-way nMOS divider (one parallel pair, one series pair, all four matched) - input current sunk from both sources, output currents measured at drains

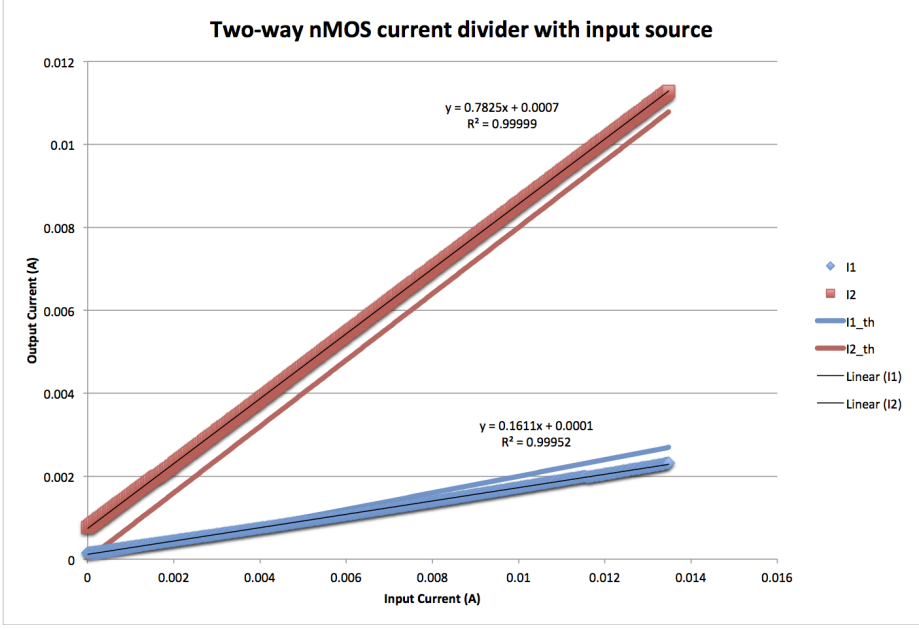

Figure 7: Two-way nMOS divider (one parallel pair, one series pair, all four matched) - input current sourced to both drains, output currents measured at sources