Circuits Lab 4

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1 Experiment 1: Bipolar Transistor Modeling

We swept base voltage as we meaured base and emitter current, which we then used to calculate collector current. Using these values, for all 4 transistors we extracted I_s and β.

	I_s	β
T1	$5E-13$	635
T2	$5E-13$	640
T3	$3E-13$	650
T4	$7E-13$	638

We next constructed a plot showing all four collector currents and all four base currents as a function of the base voltage, which can be seen in Figure 1 on the following page.

We then created a plot showing the percentage difference between each transistor's collector current and the mean value of all four collector currents as a function of base voltage, shown in figure Figure 2 on page 3 The first transistor had some values at low voltages that did not match very well for the first transistor. These values were so high that it made all other values appear as zero and so were excluded to make the graph actually meaningful. The transistors are generally match well enough however that we can abstract that they are matched. There is a steady decline in the percent difference from the mean for some of them for between .2 and .5 volts, but aside from taht there are no systematic differences. After around .62 the percent difference is so low as to be neglible.

Lastly, we generated a plot showing the beta value for all 4 transistors as a function of base current, as show in Figure 5 on page 5

The transistors had reasonable

2 Experiment 2: Translinear Circuit 1

For Experiment 2 we constructed the circuits shown in figures 4.1b, 4.2a and 4.2b in the lab packet (connecting the substrate to ground after long pondering over incconsistent data). We used one each of an MAT14 quad *npn* array, an LMC6482 op-amp, an 2N3904 *npn* and an 2N3906 *pnp* as well as three different

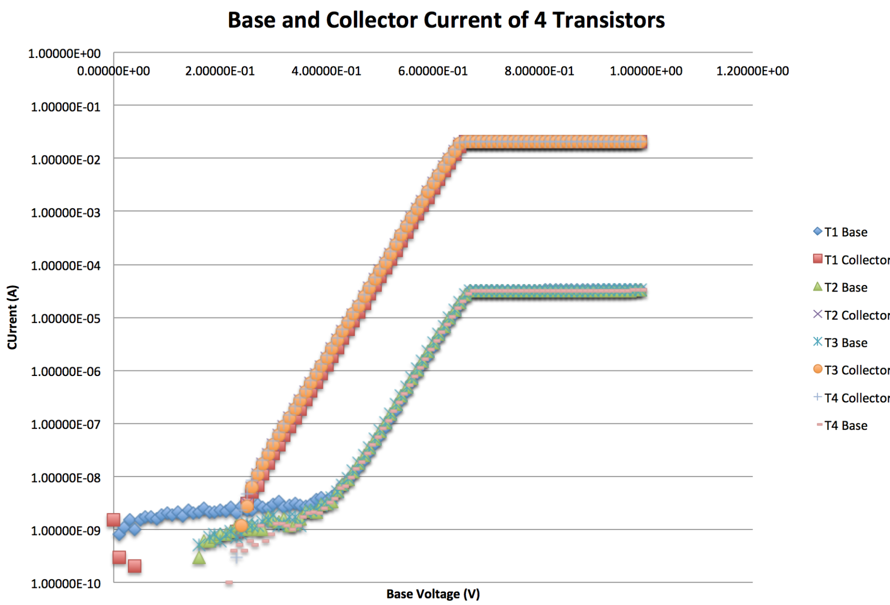

Figure 1: a plot showing all four collector currents and all four base currents as a function of the base voltage

resistors as discussed ahead. We tied the collectors of the two top transistors to the $5V$ (actually $4.91V$) rail to ensure that all transistors stay in the forward active region. Instead of connecting the bottom right transistor to ground, we connected it to the positive terminal of the SMU's Channel 2 (the negative connected to ground) so that we could measure an estimate for I_z (all base currents are assumed to be small, and therefore the vast majority of current at the bottom comes from the top collector).

For the first part of the experiment, we tied the positive Channel 1 terminal to the bases of the top two transistors (the negative connected to ground) and swept currents from 10nA to 10mA, spread logarithmically, sourcing I_x. We used, in turn, a $1k\Omega$, $10k\Omega$ and $100k\Omega$ resistor for R in the sink circuit, and tied the collector of the *pnp* to the base of the bottom-left transistor in the circuit, sinking I_y. We set the potentiometer so that its output (while connected to the op-amp) was $.19V$ - yielding final sink currents of about $.19mA$, $.019mA$ and $.0019mA$ (respectively), using the formula calculated in the prelab. This was sufficient to keep the transistor in soft saturation. We recorded current readings from Channel 2, estimating I_z for each I_x value. The results are plotted in Figure **??** on page ?? for each resistor on a log-log scale against a theoretical estimation, according to the following formula, derived too in the prelab:

$$I_z = \sqrt{I_x I_y}$$

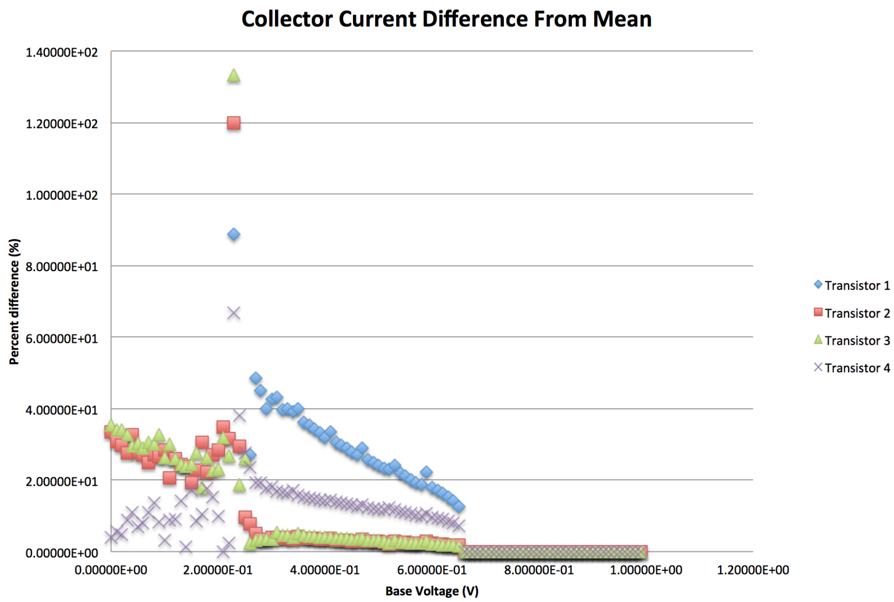

Figure 2: A plot showing the percentage difference between each transistor's collector current and the mean value of all four collector currents as a function of base voltage

using the values of I_y calculated above.

For the **second** part of the experiment, we tied the positive Channel 1 terminal **to the base of the bottom-left transistor in the circuit** (the negative connected to ground) and swept currents from **-10nA to -10mA**, spread logarithmically, **sinking** I_y. We used, in turn, a $1k\Omega$, $10k\Omega$ and $100k\Omega$ resistor for R in the **source** circuit, and tied the collector of the ***npn*** **to the bases of the top two transistors, sourcing** I_x. We set the potentiometer so that its output (while connected to the op-amp) was $3.44V$ **- yielding final source currents of about** $1.47mA$**,** $.147mA$ **and** $.0147mA$ (respectively), using the formula calculated in the prelab. This was sufficient to keep the transistor in **the forward active region**. We recorded current readings from Channel 2, estimating I_z for each I_y value. The results are plotted in **Figure ?? on page ??** for each resistor on a log-log scale against a theoretical estimation, according to the following formula, derived too in the prelab:

$$I_z = \sqrt{I_x I_y}$$

using the values of I_x calculated above.

All data matches the predicted data very well in FAR.

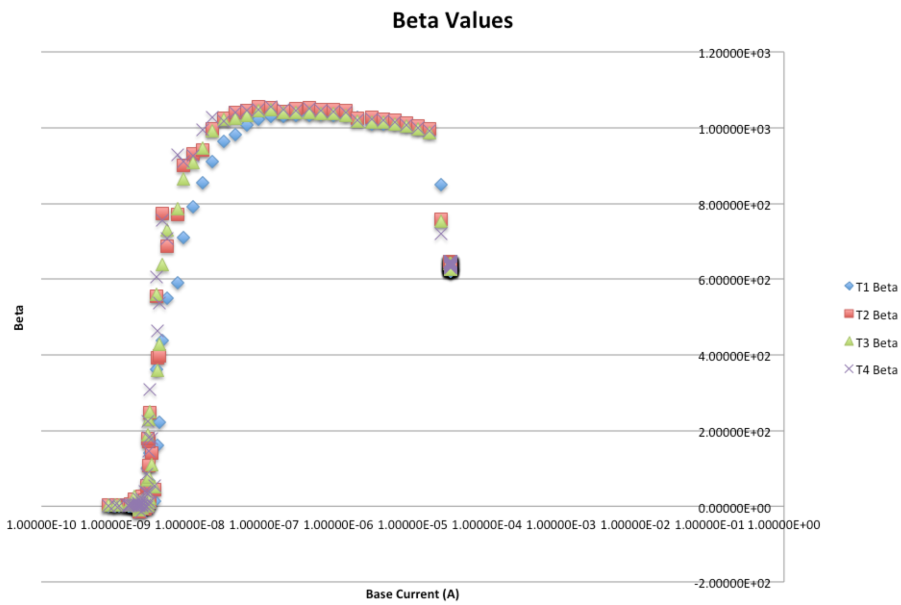

Figure 3: A plot showing the beta value for all 4 transistors as a function of base current

3 Experiment 3: Translinear Circuit 2

For Experiment 3 we also constructed the circuit form figure 4.1c in the lab packet, reusing our source and sink circuits from Experiment 2. The steps we took were nearly identical, except for one resistor change in the sink tests - since sink current is in the denominator of the output current, large values for the resistor in the sink circuit quickly railed our output current - we therfore used a 100Ω instead of a $100k\Omega$ resistor for our third test. We also used slightly different potentiometer set ups, resulting in currents of 1.2mA .12mA and .012mA for the source circuit and .021mA, .21mA and 2.1mA for the sink ciruit. The formula we used for out theoretical lines was derived in the prelab:

$$I_z = \frac{I_x^2}{I_y}$$

Our results of sweeping sink current are shown in Figure 7 on page 6 and the results for sweeping source current are Figure **??** on page ??.

All data matches the predicted data very well in FAR.

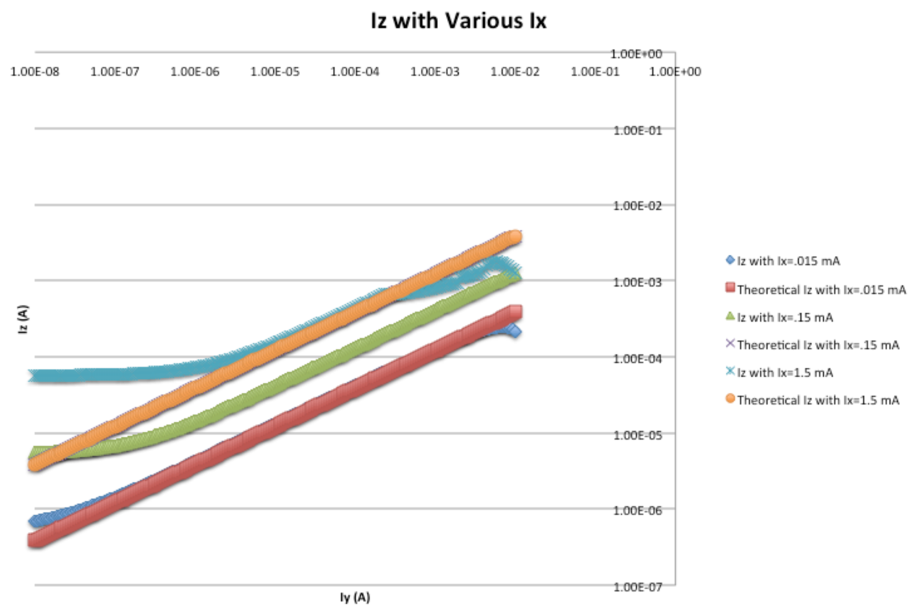

Figure 4: A log plot showing Iz (amps) of the first translinear circuit when the current source Ix is set at various values

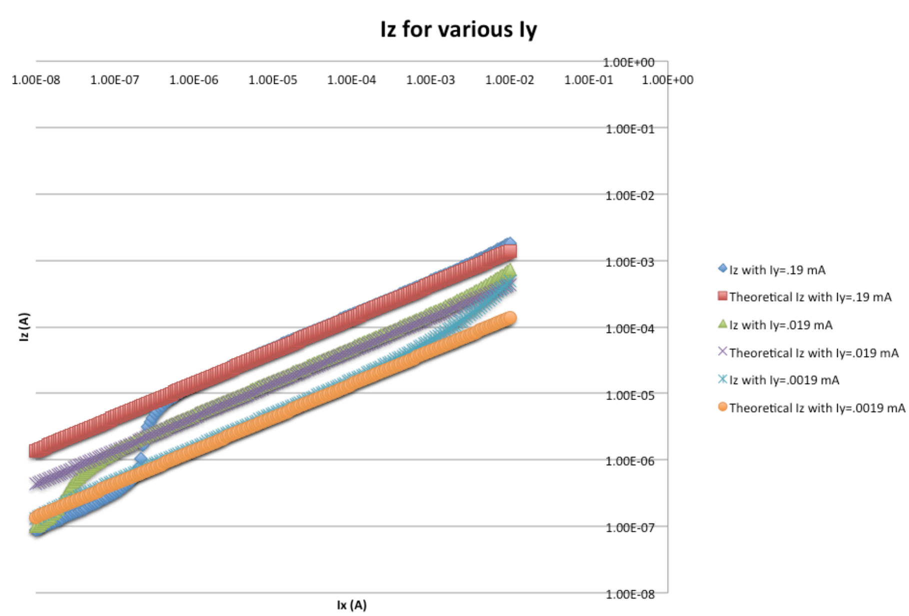

Figure 5: A log plot showing Iz (amps) of the first translinear circuit when the current sink Iy is set at various values

Figure 6: A plot showing Iz in the second translinear circuit as a function of Ix (both in amps)

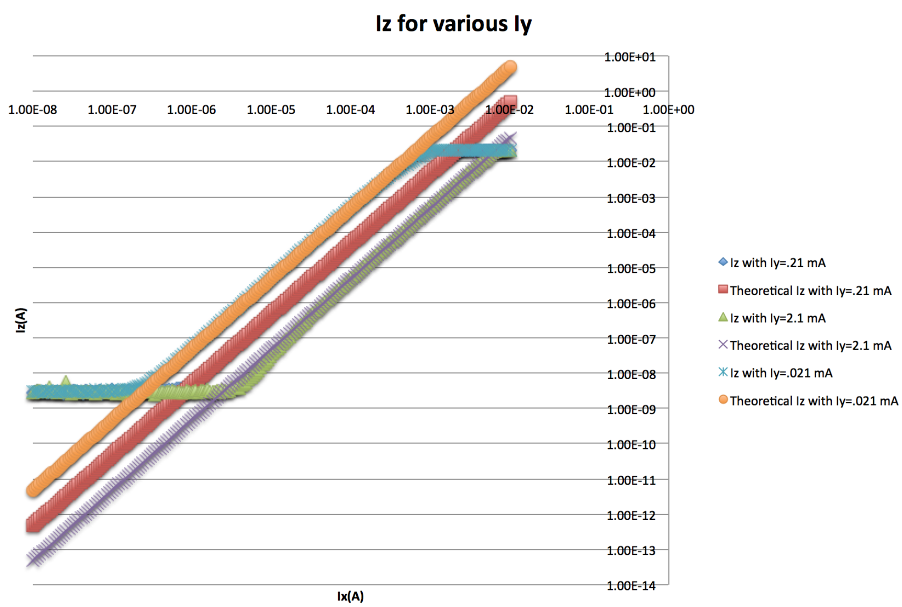

Figure 7: A plot showing Iz in the second translinear circuit as a function of Ix (both in amps)