Circuits Lab 5

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1 Experiment 1: Gate Characteristics

For both a nMOS and pMOS transistor we swept gate voltage and measured the channel current.We fit the EKV model to the collected data for both.

1.1 nMOS

The EKV model of: $I_{sat} = I_s log^2(1 + e^{(\kappa(V_{GB}-V_{TO})-V_{SB})/2U_T})$ was fit to the data and parameters were extraced, listed below:
$I_s = 7.1652e-06A$
$V_{TO} = .5844V$
$\kappa = 0.40639$ The data and fitted model is shown in figure Figure 1 on page 3:

1.2 pMOS

The EKV model of: $I_{sat} = I_s log^2(1 + e^{(\kappa(V_{BG}-V_{TO})-V_{BS})/2U_T})$ was fit to the data and parameters were extraced, listed below:
$I_s = 6.1023e-07A$
$V_{TO} = -0.6644V$
$\kappa = -0.7974$
The data and fitted model is shown in figure Figure 2 on page 3:

1.3 Incremental Transconductance Gain

We used the diff and ./ MATLAB function to obtain a crude finite-difference approximation to the partial derivative of the channel current with respect to the gate voltage for both nMOS and pMOS transistors. We then plotted the weak inversion and strong inversion theoretical fits. The weak inversion model used was $\frac{I_{sat}}{U_T}$ for strong inversion it was $\frac{\sqrt{I_s I_{sat}}}{U_T}$ with values extracted above for nMOS and pMOS appropriately and $U_T = .025V$
The plot for an nMOS can be seen in Figure 3 on page 4. The theoretical fit for the weak inversion region is reasonable but a little off, likely due to imperfectly extracted kappa value. The theoretical fit for strong inversion fits the data very

well.

The plot for the pMOS can be seen in Figure 4 on page 5. The gain values were all multiplies by -1 so that a loglog could be properly constructed. Once again the weak inversion line is somewhat higher than the data suggests, but the strong inversion is well fitted to the plot.

2 Experiment 2: Source Characteristics

3 Experiment 3: Drain Characteristics

For both nMOS and pMOS transistors we attempted to force them into weak, moderate, and strong inversion by picking and setting appropriate values of gate voltage. We then swept the drain voltages and recorded the resulting channel current. These are shown in Figure 7 on page 7 for the nMOS and Figure **??** on page ?? for the pMOS.

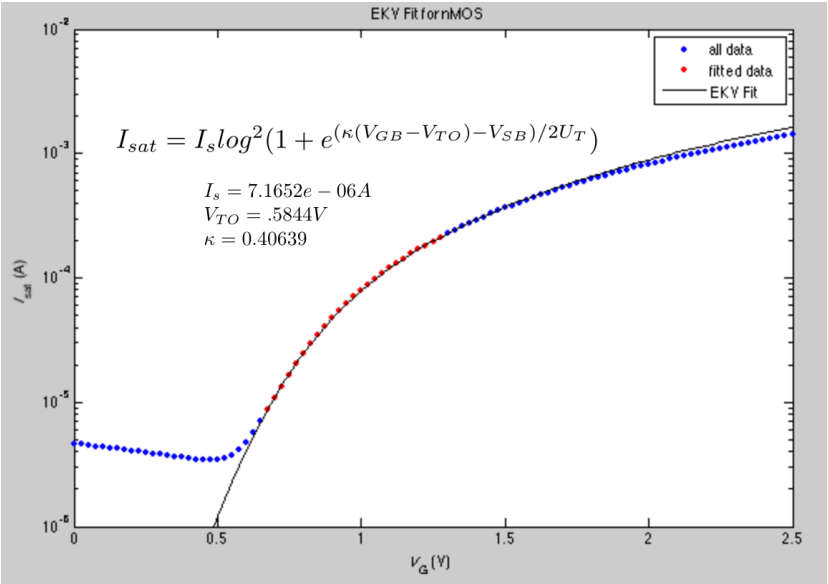

Figure 1: A plot showing the I_{sat} for an nMOS transistor as a function of gate voltage

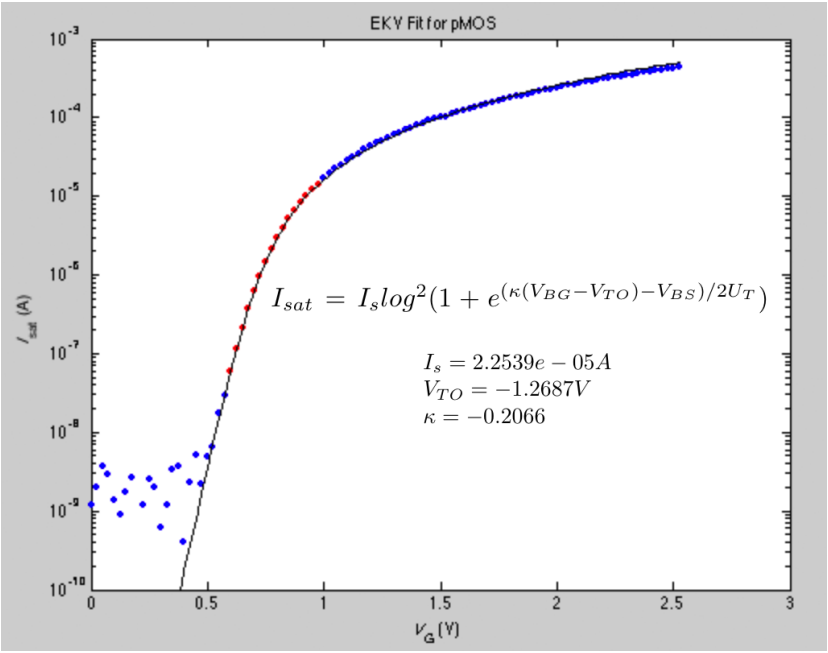

Figure 2: A plot showing the I_{sat} for an pMOS transistor as a function of gate voltage

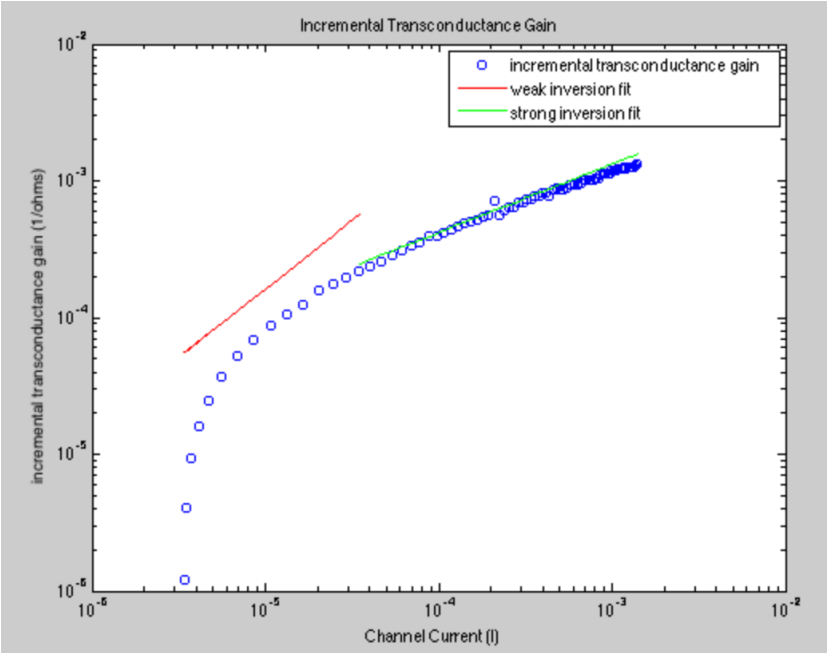

Figure 3: A plot showing transconductance gain as a function of channel current for a nMOS transistor

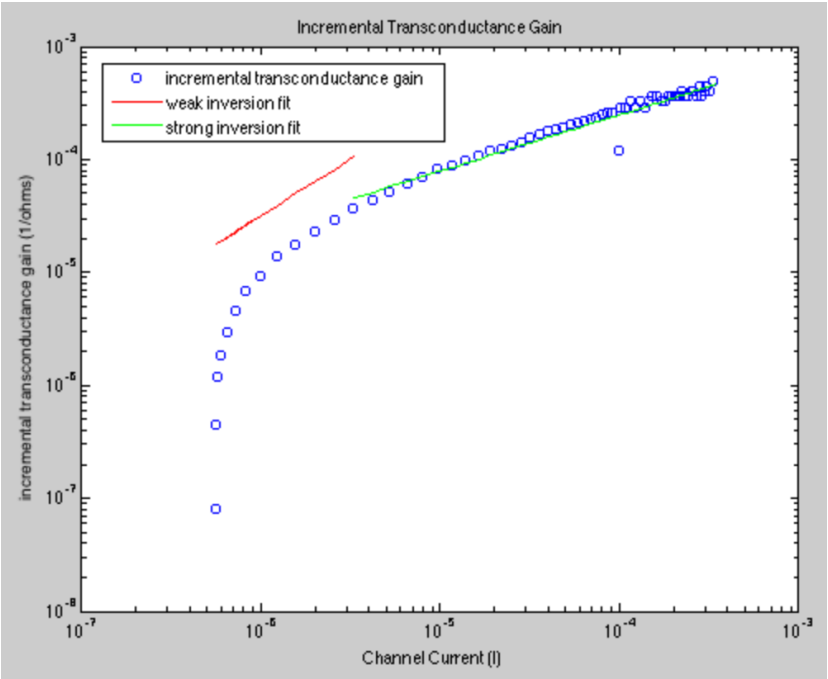

Figure 4: A plot showing transconductance gain as a function of channel current for a pMOS transistor

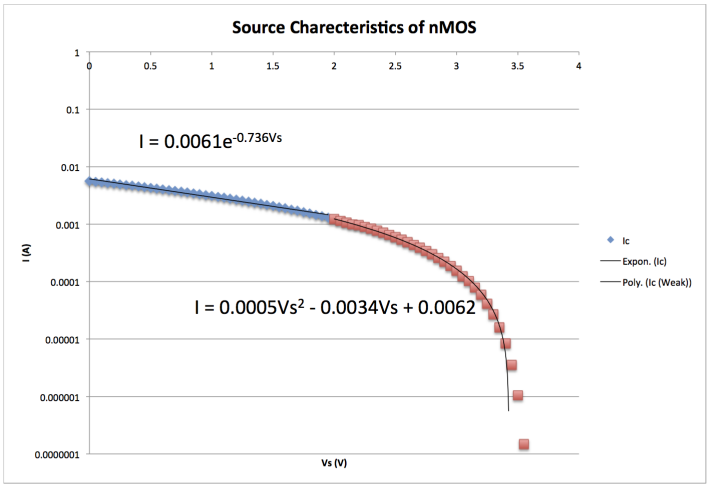

Figure 5: A plot showing the nMOS channel current as a function of source voltages for gate and drain voltages of Vdd

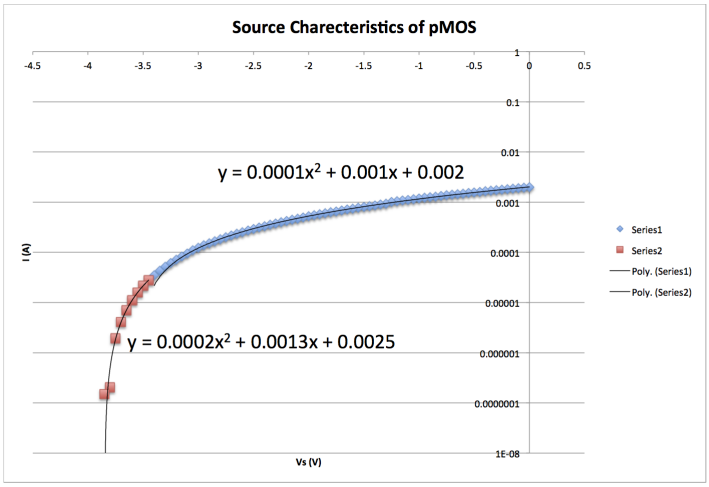

Figure 6: A plot showing the pMOS channel current as a function of source voltages for gate and drain voltages of ground

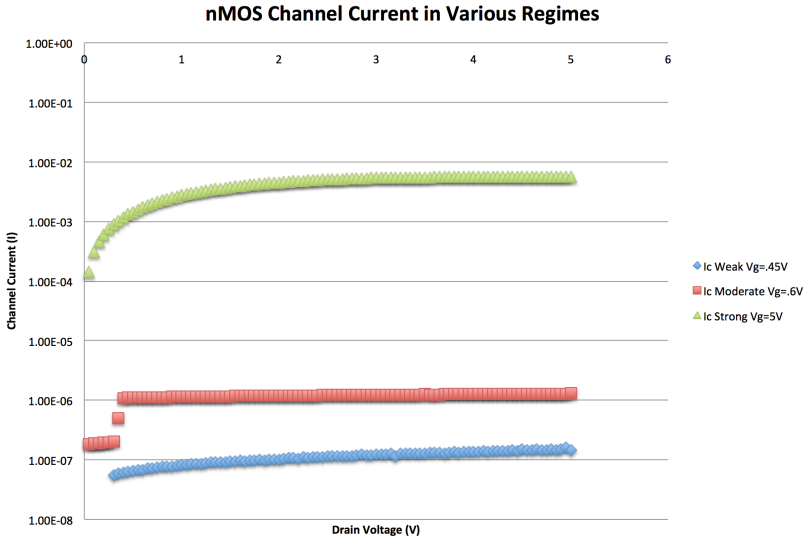

Figure 7: A plot showing the nMOS channel current as a function of drain voltages for various gate voltages