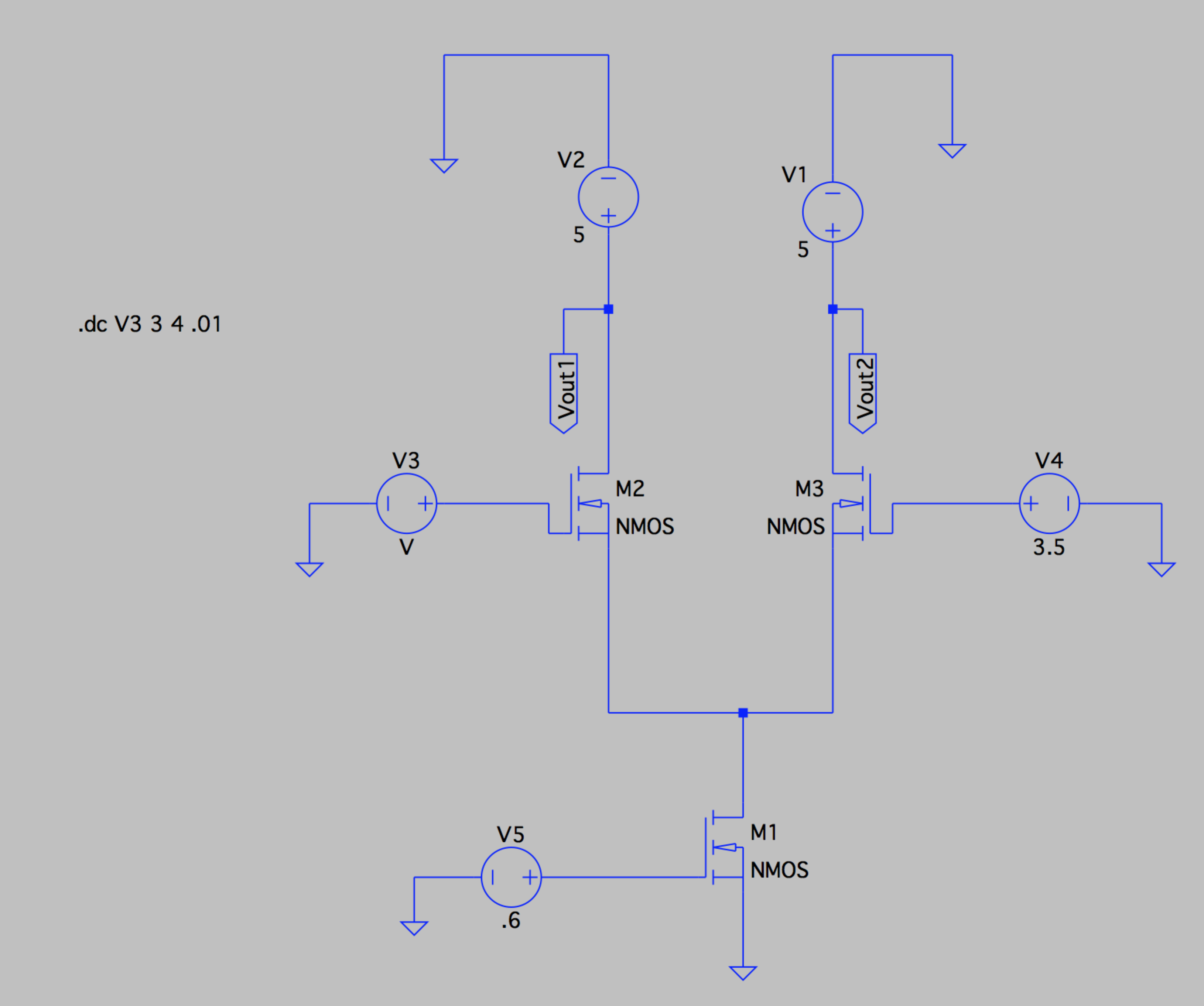
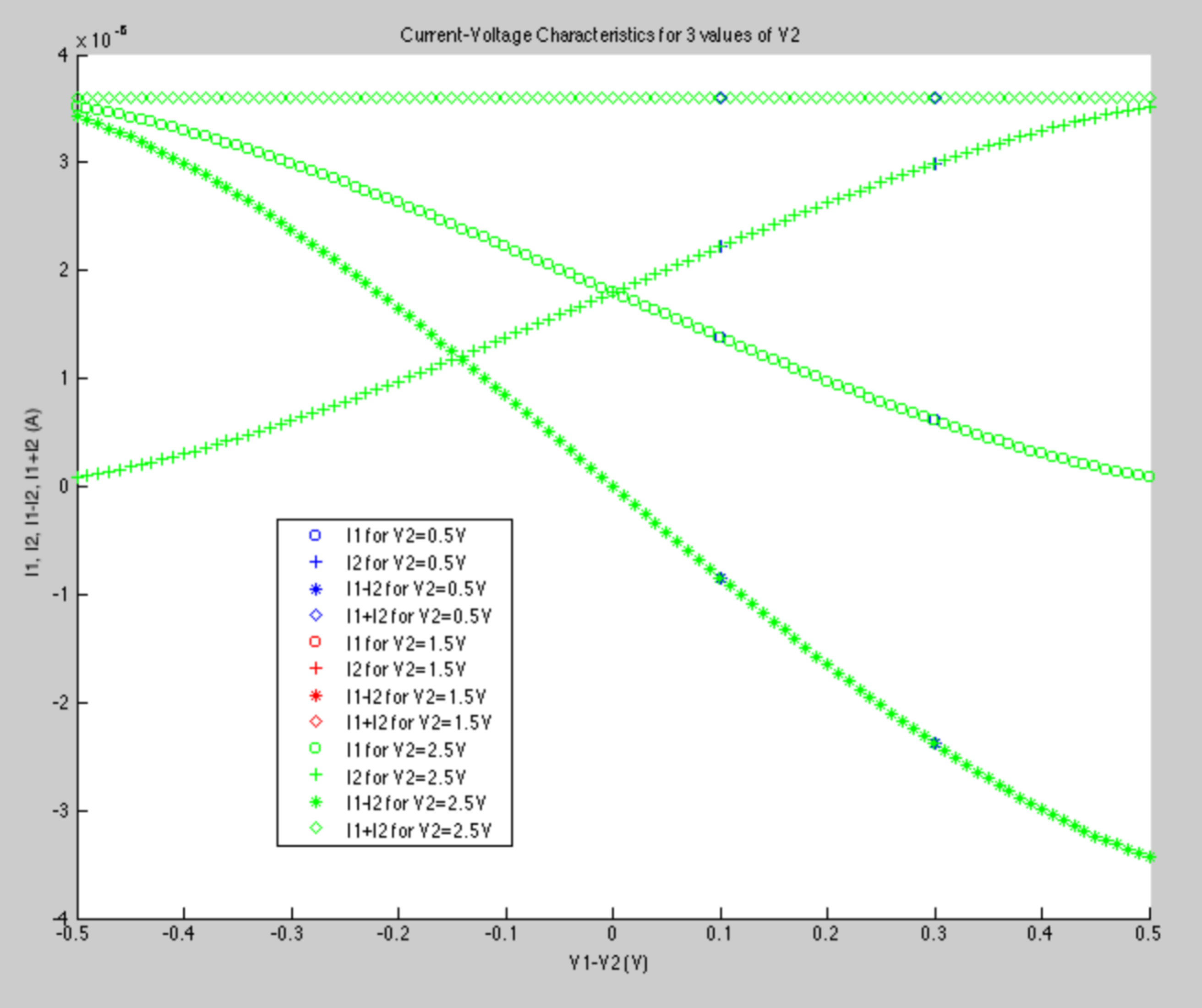
Thomas Nattestad

Postlab 7:

For this postlab, I constructed the nMOS differential pair in LTSpice and collected data from the simulation. The circuit I constructed is seen below:



The plot for 3 different values of V2 (V4 in LTSpice circuit) is shown below. Note that the three different lines are so identical they are perfectly on top of one another:



We then put the bias transistor in deep saturation by setting Vb to be 1.3V. We collected the simulated data for a single value of V2 = 3.5, which is shown below:

