Student Name (Please print)_____

Student Number_____ Section:_____

ITI1200A-Digital Systems I

Examiners:
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Professor Abdul Al-Dhaher

Date: April 23, 2006
Time: 3 hours

Instructions:

- Answer ALL questions.
- This is a close-book examination**.**
- Use the provided space to answer the following questions. If more space is needed, use the back of the page.
- Show all your calculations to obtain full marks.
- Calculators are allowed.
- Read all the questions carefully before you start.

(the following space is reserved for professor)

Question	Points	Percentage
1		20%
2		25%
3		15%
4		20%
5		20%
Total		100%

Question 1: (10 + 10 = 20 points)

(a) Perform the following arithmetic operations using non signed numbers representation.

1- $(1001.01)_2$ - $(10101.0)_2$
(show the carry after each addition of two digits)

2- $(10100.011)_2$ + $(11001)_2$ **(show the carry after addition of each two digits)**

(b) Convert **$A = (20.5)_{10}$ and $B = (12.4)_{10}$** into binary format employing 6 bits for the integer part and 3 for the fractional part, including the sign bit. Perform the following operations using the signed 1's complement representation.

(i) $C = A + B$ (ii) $D = -A + B$

Important note: ***Explain clearly your solution! Please note that if you give directly the result of the conversion of the two numbers (A and B), without explaining the conversion method you have used, your mark for this part of the question will be zero!***

Question 2 (10 + 10 +10 = 30 points)

Given the following Boolean function together with the "*don't care*" conditions *d*:

F(a,b,c,d) = Σm(2,3,4,6,9, 11,12) and *d*(a,b,c,d) = Σm(0,1,14,15)
G(a,b,c,d) = Σm(2,6,10,11,12) and *d*(a,b,c,d) = Σm(0,1,14,15)

i. Find the minimal Sum-of- products expressions of the given functions using K-map.

ii. Implement your minimized functions with NAND gates only and draw the logic diagram of your circuit.

iii. Use a multiplexer to implement G

Note: Any type of gate with any number of inputs are available.

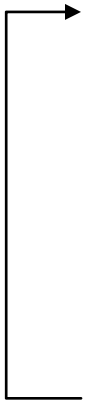
Question 3: (15 points)

Design a ripple (asynchronous) counter with JK flip flops that having to count sequences from 0000 (zero) to 1001 (9) and draw the corresponding logic circuit.

(i) Build the state table for the counter
(ii) Draw the logic circuit

Question 4: (15 points)

Design a synchronous counter having the count sequence given by the following table. Use negative edge-triggered T flip-flops provided with a clock.



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	1	0	1
0	0	1	0
1	0	1	1
0	1	1	0
0	1	0	0
1	1	0	0
1	0	0	1
1	1	1	0

(i) Draw the state diagram of the counter.
(ii) Build the counter's state table showing the synchronous inputs of the T flip-flops as well.
(iii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the flip-flops; assume the next states of the unused combinations to be "don't care states"
(iv) Draw the logic diagram of the counter

Question 5: (12 + 8 = 20 points)

a) Design a serial Adder with JK Flip Flop and draw the corresponding logic circuit. The two binary numbers to be added, X and Y, are stored in two shift registers A and B respectively. The result (sum) of the adder must be stored in the register B. Use a full adder to add the two numbers. Answer the following questions

(i) Give a table that shows
   a. the inputs and outputs for the full adder
   b. the states (present and next) for the JK flip Flop
   c. The Flip Flop inputs

(ii) Obtain the logic expressions for the inputs and outputs

(iii) draw the logic circuit of the serial Adder (use a diagram to represent the full adder and the registers)

If needed, use this page and indicate the question number.

(c) Design a code converter that converts a decimal digit from the code 8,4,-2,-1 to 8,4,2,1 code

(d) Build truth table for the converter

(e) Design the circuit with a decoder.