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Student Name (Please print)_____

Student Number_____ Section:_____

# ITI1200A-Digital Systems I

Examiners:
Professor Ahmed Karmouch
Professor Abdul Al-Dhaher

Date: April 25, 2007
Time: 3 hours

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**Instructions:**

- Answer ALL questions.
- This is a close-book examination**.**
- Use the provided space to answer the following questions. If more space is needed, use the back of the page.
- Show all your calculations to obtain full marks.
- Calculators are allowed.
- Read all the questions carefully before you start.

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(the following space is reserved for professor)

| Question | Points | Percentage |
|---|---|---|
| 1 | | 20% |
| 2 | | 30% |
| 3 | | 15% |
| 4 | | 20% |
| 5 | | 15% |
| Total | | 100% |

**Question 1: (2 + 18 = 20 points)**

(a) Perform the following arithmetic operations using non signed numbers representation.

1- $(1011.01)_2$ - $(11101.11)_2$
**(Show the carry after each addition of two digits)**

(b) Convert **$A = (12.5)_{10}$ and $B = (1.45)_{16}$** into binary format employing 6 bits for the integer part and 3 for the fractional part, including the sign bit. Perform the following operations

| | | |
|---|---|---|
| (ii) | C = -A - B | using signed 1's complement |
| (ii) | D = – A + B | using signed 2'a complement |
| (iii) | E= A – B | using 9's complement (show all intermediate steps) |

**Important note:** ***Explain clearly your solution! Please note that if you give directly the result of the conversion of the two numbers (A and B), without explaining the conversion method you have used, your mark for this part of the question will be zero!***

**Question 2: (12+ 8 = 20 points)**

**(A)** Design a combinational circuit that generates the 10's complement of a BCD (Binary Coded Decimal) digit.

**(i)** Built the truth table of your circuit
**(ii)** Simplify the outputs in their some of products form using K-map
- a- List all prime implicants
- b- List essential prime implicants

**(iii)**Draw your circuit with NAND gates only

**(B)** Given the following Boolean functions
(from winter 2007 final exam)

$F(a,b,c) = \Sigma m(0,2,3,7)$
$G(a,b,c,) = \Sigma m(1,4,6,7)$

**(i)** Use a NAND implementation decoder with external NAND gates only to implement F and G in **their some of products form.** (Assume that any type of gates with any number of inputs is available).
**(ii)** Use a multiplexer to implement G.

**Question 3: (15 points)**

Design a modulo-5 ripple (asynchronous) up-counter with JK flip-flops and draw the corresponding logic circuit. (From winter 2007 final exam)
Also in "EXAM 1 PAGE 2" in dropbox!

(i) Build the state diagram
(ii) Draw the logic circuit
(iii) What is the maximum modulus of the counter?

**Question 4: (20 points)**

Design a synchronous BCD counter. Use negative edge-triggered D flip-flops provided with a clock. (from Winter 2007 final exam)

(i) Draw the state diagram of the counter.
(ii) Build the counter's state table showing the synchronous inputs of the T flip-flops as well.
(iii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the flip-flops; assume the next states of the unused combinations to be "don't care states"
(iv) Draw the logic diagram of the counter
(v) Modify your diagram (of (iv)) to show how your DCB counter can be cleared when it reaches the value 7. Use active low clear and NAND gate.

**Question 5: ( 15 points)**

(from winter 2007 and 2006 final exams)

a) Design a serial Adder with JK Flip Flop and draw the corresponding logic circuit. The two binary numbers to be added, X and Y, are stored in two shift registers A and B respectively. The result (sum) of the adder must be stored in the register B. Use a full adder to add the two numbers. Answer the following questions

(i) Give a table that shows
   a. the inputs and outputs for the full adder
   b. the states (present and next) for the JK flip Flop
   c. The JK Flip Flop inputs

(ii) Obtain the logic expressions for the JK inputs and the outputs of the full adder

(iii) draw the logic circuit of the serial Adder (use a diagram to represent the full adder and the registers)

*If needed, use this page and indicate the question number.*