Treasurer's
March 21st, 20

ITI1100- Exam -previous

Question 1: (4 + 16 = 20 points)

(a) Perform the following arithmetic operations using non signed numbers representation.

$(1011.01)_2 - (11101.11)_2$

(Show the carry after each addition of two digits)

(b) Convert **A = $(12.5)_{10}$ and B= $(1.40)_{16}$** into binary format employing 7 bits for the integer part and 3 for the fractional part, including the sign bit. Perform the following operations in specific signed complement as indicated for each operation.

(i)	C = -A - B	using signed 1's complement
(ii)	D = – A + B	using signed 2's complement
(iii)	E= A – B	using 9's complement (show all intermediate steps)

Important note: ***Explain clearly your solution! Please note that if you give directly the result of the conversion of the two numbers (A and B), without explaining the conversion method you have used, your mark for this part of the question will be zero!***

Question 2: (20+ 10 = 30 points)

Part A: Design a combinational circuit that generates the 10's complement of a BCD (Binary Coded Decimal) digit.

(i) Built the truth table of your circuit
(ii) Simplify the outputs in their sum of products form using K-map (assume unused combinations to be "don't care".

a- List all prime implicants
b- List essential prime implicants

(iii) Draw your circuit with NAND gates only (Assume NAND gates with any number of inputs are available).

Part-B: Given the following Boolean functions

F (a,b,c) = $\Sigma m(0,2,3,7)$
G (a,b,c,) = $\Sigma m(1,4,6,7)$

(i) Use a NAND implementation decoder with external NAND gates only to implement F and G in **their sum of products form.** (Assume NAND gates with any number of inputs are available).

(ii) Use a multiplexer to implement G.

Question 3: (15 points)

Design a modulo-5 ripple (asynchronous) up-counter with JK flip-flops and draw the corresponding logic circuit.

(i) Build the state diagram
(ii) Draw the logic circuit
(iii) What is the maximum modulus of the counter?

Question 4: (25 points)

Design a "**synchronous** BCD counter". Use negative edge-triggered D flip-flops provided with a clock.

(i) Draw the state diagram of the counter.
(ii) Build the counter's state table showing the synchronous inputs of the D flip-flops as well.
(iii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the flip-flops; assume the next states of the unused combinations to be "don't care states"
(iv) Draw the logic diagram of the counter
(v) Modify your diagram (of (iv)) to show how your BCD counter can be cleared when it reaches the value 7. Use active low clear and NAND gate.

Question 5: (10 points)

(From "EXAM 1 PAGE 2" and "Final Exam Practice" in dropbox)

a) Design a serial Adder with T Flip Flop and draw the corresponding logic circuit.
The two binary numbers to be added, X and Y, are stored in two shift registers A and B respectively. Y is stored in its 1's complement. Before adding X to Y you should obtain the 1's complement of Y. The result (sum) of the adder must be stored in a third shift register C. Use a full adder to add X and the 1's complement of Y. Answer the following questions:

(i) Give a table that shows
   a. the inputs and outputs for the full adder
   b. the states (present and next) for the T flip Flop
   c. The T Flip Flop inputs
(ii) Obtain the logic expressions for the T inputs and the outputs of the full adder
(iii) draw the logic circuit of the serial Adder (use a diagram to represent the full adder and the registers)

March 24th, 2011

ITI1100

Question 1: (10 + 10 = 20 points)

(a) Perform the following arithmetic operations using non signed numbers representation.

1- $(1001.01)_2$ - $(10101.10)_2$ **(show the carry after each addition of two digits)**

2- $(10100.011)_2$ + $(11001)_2$ **(show the carry after addition of each two digits)**

(b) Convert **A = $(15.5)_{10}$ and B= $(16.45)_{10}$** into binary format employing 6 bits for the integer part and 2 for the fractional part, including the sign bit. Perform the following operations using the signed 1's complement representation.

(i) C = A + B (ii) D = – A + B

Question 2: (10 + 10 +10 = 30 points)

Given the following Boolean function together with the "*don't care*" conditions *X*:

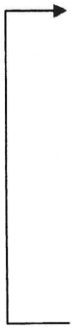
$F(a,b,c,d) = \Sigma m(2,3,4,6,9, 11,12)$ and $X(a,b,c,d) = \Sigma m(0,1,14,15)$
$G(a,b,c,d) = \Sigma m(2,6,10,11,12)$ and $X(a,b,c,d) = \Sigma m(0,1,14,15)$

i. Find the minimal Sum-of- products expressions of the given functions using K-map.
ii. Implement your minimized functions with NAND gates only and draw the logic diagram of your circuit.
iii. Use a multiplexer to implement G (assume that any type of gates with any number of inputs are available)

Question 3: (15 points)
Design a ripple (asynchronous) counter with JK flip flops that having to count sequences from 0000 (zero) to 1001 (9) and draw the corresponding logic circuit.

(i) Build the state table for the counter the first 8 clock pulse
(ii) Draw the logic circuit
(iii) What is the Modulus of the counter?

Question 4: (20 points)
Design a synchronous counter having the count sequence given by the following table. Use negative edge-triggered T flip-flops provided with a clock.



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	1	0	1
0	0	1	0
1	0	1	1
0	1	1	0
0	1	0	0
1	1	0	0
1	0	0	1
1	1	1	0

(i) Draw the state diagram of the counter.
(ii) Build the counter's state table showing the synchronous inputs of the T flip-flops as well.
(iii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the flip-flops; assume the next states of the unused combinations to be "don't care states"
(iv) Draw the logic diagram of the counter

Question 5: (15 points)

a) Design a serial Adder with JK Flip Flop and draw the corresponding logic circuit. The two binary numbers to be added, X and Y, are stored in two shift registers A and B respectively. The result (sum) of the adder must be stored in the register B. Use a full adder to add the two numbers. Answer the following questions

(i) Give a table that shows
   a. the inputs and outputs for the full adder
   b. the states (present and next) for the JK flip Flop
   c. The JK Flip Flop inputs
(ii) Obtain the logic expressions for the JK inputs and the outputs of the full adder
(iii) draw the logic circuit of the serial Adder (use a diagram to represent the full adder and the registers)