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- (i) Use a NAND implementation decoder with external NAND gates only to implement F and G in **their sum of products form**. (Assume NAND gates with any number of inputs are available).
 - (ii) Use a multiplexer to implement G.

Question 3: (15 points)

Design a modulo-5 ripple (asynchronous) up-counter with JK flip-flops and draw the corresponding logic circuit. (from "EXAM PAGE 2" in dropbox)

- (i) Build the state diagram
- (ii) Draw the logic circuit
- (iii) What is the maximum modulus of the counter?

Question 4: (25 points)

Design a "synchronous BCD counter". Use negative edge-triggered D flip-flops provided with a clock. (From "EXAM 1 PAGE 2" in dropbox and Winter 2007 Final exam)

- (i) Draw the state diagram of the counter.
- (ii) Build the counter's state table showing the synchronous inputs of the D flip-flops as well.
- (iii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the flip-flops; assume the next states of the unused combinations to be "don't care states"
- (iv) Draw the logic diagram of the counter
- (v) Modify your diagram (of (iv)) to show how your BCD counter can be cleared when it reaches the value 7. Use active low clear and NAND gate.

Question 5: (10 points)

(From "EXAM 1 PAGE 2" in dropbox)

- a) Design a serial Adder with T Flip Flop and draw the corresponding logic circuit. The two binary numbers to be added, X and Y, are stored in two shift registers A and B respectively. Y is stored in its 1's complement. Before adding X to Y you should obtain the 1's complement of Y. The result (sum) of the adder must be stored in a third shift register C. Use a full adder to add X and the 1's complement of Y. Answer the following questions:

- (i) Give a table that shows
 - a. the inputs and outputs for the full adder
 - b. the states (present and next) for the T flip Flop
 - c. The T Flip Flop inputs
 - (ii) Obtain the logic expressions for the T inputs and the outputs of the full adder
 - (iii) draw the logic circuit of the serial Adder (use a diagram to represent the full adder and the registers)
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