

Université d'Ottawa  
Faculté de génie



University of Ottawa  
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**ITI 1100**

**SAMPLE FINAL EXAM GIVEN in 2013  
Solutions**

**Name:**

**Student Number:**

**Good Luck!**

**Question 1 (8 points)**

- a. The solutions to the quadratic equation  $x^2 - 10x + 14 = 0$  are  $x = 2$  and  $x = 6$ . What is the base of the numbers? Show your work.

**base=8**

- b. Show that the dual of the exclusive-OR is equal to its complement.

**Q2.24 of the book**

$$x \text{ xor } y = x'y + xy' \text{ and } (x \text{ xor } y)' = (x + y')(x' + y)$$

$$\text{Dual of } x'y + xy' = (x' + y)(x + y') = (x \text{ xor } y)'$$

- c. Find the complement of  $F = wx + yz$ ; What is the value of  $FF'$  ?

**Q2.8 of the book**

$$F' = (wx + yz)' = (wx)'(yz)' = (w' + x')(y' + z')$$

$$FF' = wx(w' + x')(y' + z') + yz(w' + x')(y' + z') = 0$$

$$F + F' = wx + yz + (wx + yz)' = A + A' = 1 \text{ with } A = wx + yz$$

**Question 2 (8 points)**

A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise.

Design a 3 input majority circuit by finding the circuit's truth table, Boolean equation and a logic diagram.

**Q4.6 of the book**

$$F = xz + yz + xy$$

**Question 3 (11 points)**

Design a combinational circuit that generates the 9's complement of a BCD digit by finding the circuit's truth table, Boolean equation and a logic diagram.

**Q4.18 of the book**

**Inputs:**                    **ABCD**

**Outputs:**        **wxyz**

$$d(A, b, c, d) = \Sigma(10, 11, 12, 13, 14, 15)$$

$$w = A'B'C'$$

$$x = BC' + B'C = B \text{ xor } C$$

$$y = C$$

$$z = D'$$

**Question 4 (5 points)**

A combinational circuit is specified by the following two Boolean functions:

$$F_1(A,B,C) = \sum(1,4,6)$$

$$F_2(A,B,C) = \sum(3,5)$$

Implement the circuit with a decoder. Use a block diagram for the decoder and use NAND gates for the gates connected to the decoder outputs.

**Q4.27 of the book**

4.27

4.28 (a)

$$F_1 = x'y'z + y'z' + x'yz' = xy'z + xy'z' + x'yz' = \Sigma(2, 5, 7)$$

$$F_2 = xy'z' + x'y'z' + x'yz' + x'yz' = \Sigma(2, 3, 4)$$

$$F_3 = x'y'z' + xy'(z + z') = x'y'z' + xy'z = \Sigma(0, 6, 7)$$

(b)

**Question 5 (8 points)**

Implement the following Boolean function with a multiplexer.

$$F(A,B,C) = \sum(2,4,6)$$

**Q4.32 of the book**

Similar to this one

4.32 (a)  $F = \sum(0, 2, 5, 8, 10, 14)$

Inputs ABCD	Max input line (ABC)	Value	$F = \sum(0, 2, 5, 8, 10, 14)$
000	0	0	1 $F = D'$
000	1	1	0
001	1	2	1 $F = D'$
001	1	3	0
010	2	4	0 $F = D$
010	2	5	1 $F = D$
011	3	6	0 $F = 0$
011	3	7	0
100	4	8	1 $F = D'$
100	4	9	0
101	5	10	1 $F = D'$
101	5	11	0
110	6	12	0 $F = 0$
110	6	13	0
111	7	14	1 $F = D'$
111	7	15	0

The circuit diagram shows an 8x1 MUX with select lines A, B, and C. The data inputs are connected as follows: Input 0 to  $D'$ , Input 2 to  $D$ , Input 5 to  $D$ , Input 8 to  $D'$ , Input 10 to  $D'$ , and Input 14 to  $D'$ . All other inputs (1, 3, 4, 6, 7, 9, 11, 12, 13, 15) are connected to 0. The output of the MUX is  $F$ .

**Question 6 (11 points)**

A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when the inputs P and N are 00, 01, 10, and 11, respectively.

**Q5.4 of the book**

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5.3  $Q'(t+1) = (JQ' + K'Q)' = (J' + Q)(K + Q') = JQ' + KQ$

5.4

(a) 

P	N	Q(t+1)
0	0	0
0	1	Q(t)
1	0	Q'(t)
1	1	1

(b) 

P	N	Q(t)	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

(c) 

Q(t)	Q(t+1)	P	N
0	0	0	x
0	1	1	x
1	0	x	0
1	1	x	1

(d) Connect P and N together.

5.5

The truth table describes a combinational circuit.  
 The state table describes a sequential circuit.  
 The characteristic table describes the operation of a flip-flop.  
 The excitation table gives the values of flip-flop inputs for a given state transition.  
 The four equations correspond to the algebraic expression of the four tables.

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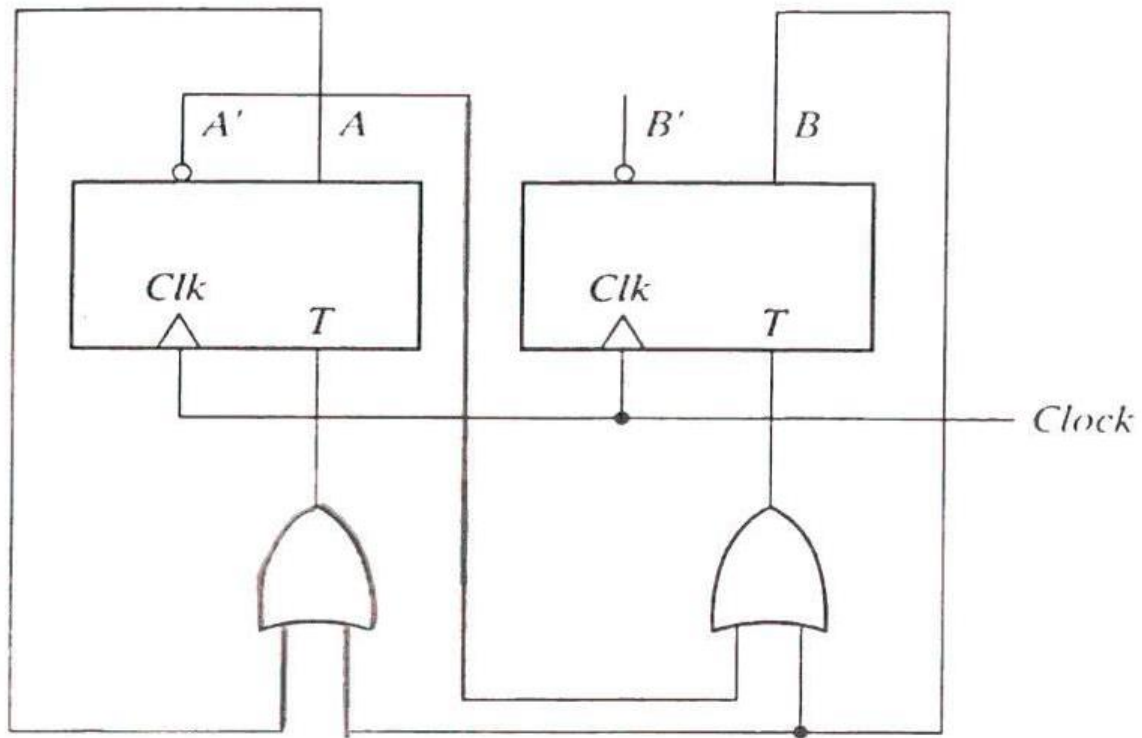
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- a. Tabulate the characteristic table.

- b. Derive the characteristic equation.
- c. Tabulate the excitation table or the transition table.

**Question 7 (8 points)**

Derive the state table, state equations and the state diagram of the following sequential circuit:

**Q5.8 of the book**



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5.8 A counter with a repeated sequence of 00, 01, 10.

Present state		Next state		FF Inputs	
A	B	A	B	$T_A$	$T_B$
0	0	0	0	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	1	1	1

$T_A = A + B$   
 $T_B = A' + B$

Repeated sequence:  
 $00 \rightarrow 01 \rightarrow 10 \rightarrow$

5.9

$J_A = x$        $K_A = B$   
 $J_B = x$        $K_B = A'$

$A(t+1) = J_A A' + K_A A = x A' + B' A$   
 $B(t+1) = J_B B' + K_B B = x B' + A B$

x	A	B	$x A' + B' A$	$x B' + A B$
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

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**Question 8 (10 points)**

For the following state table:

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	e	d	0	0
b	d	c	0	1
c	a	e	1	0
d	a	b	1	0
e	d	c	0	1

**Q5.12 and 5.13 of the book**

The screenshot shows a PDF document titled "0132774232\_ism.pdf" in Adobe Acrobat Pro. The document contains a state machine problem and its solution.

**(c)**

input	state	next st	output
0	0	0	0
1	0	1	0
0	1	0	0
1	1	1	1

State machine: D-flop with direct input of the input to the original machine;  
output logic:  $y = (\text{input}) \ \&\& \ (\text{state} == b)$

**5.12**

Present state	Next state		Output	
	0	1	0	1
a	f	b	0	0
b	d	a	0	0
d	g	a	1	0
f	f	b	1	1
g	g	d	0	1

Digital Design With An Introduction to the Verilog HDL - Solution Manual. M. Mano. M.D. Ciletti. Copyright 2012. All rights reserved.

**5.13 (a)** State:  $a f b c e d g h g g h a$

Input: 0 1 1 1 0 0 1 0 0 1 1

Output: 0 1 0 0 0 1 1 1 0 1 0

**(b) State:**  $a f b a b d g d g g d a$

Input: 0 1 1 1 0 0 1 0 0 1 1

Output: 0 1 0 0 0 1 1 1 0 1 0

- Draw the corresponding state diagram.
- Tabulate the reduced table.
- Draw the state diagram corresponding to the reduced state table.
- Starting from state a, and the input sequence 0111000, determine the output sequence for the above reduced state table.

**Question 9 (12 points)**

- a. The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift.

**Q6.4 of the book**

**6.4 0110 => 0011, 0001, 1000, 1100, 1110, 0111, 1011**

- b. List the sequence of states produced with 3 and 4 flip-flops in a Johnson counter. The initial value of the register is 000 and 0000 respectively.

**Q6.30 of the book**

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6.30

The 5-bit Johnson counter has the following state sequence:

ABCDE decoded output:	00000 A'E'	10000 A'B'	11000 B'C'	11100 C'D'	11110 D'E'
11111 A'E'	01111 A'B'	00111 B'C'	00011 C'D'	00001 D'E'	

6.31

```

module Reg_4_bit_beh (output reg A3, A2, A1, A0, input I3, I2, I1, I0, Clock, Clear);
always @(posedge Clock, negedge Clear)
if (Clear == 0) {A3, A2, A1, A0} <= 4'b0;
else {A3, A2, A1, A0} <= {I3, I2, I1, I0};
endmodule

module Reg_4_bit_Str (output A3, A2, A1, A0, input I3, I2, I1, I0, Clock, Clear);
DFF M3DFF (A3, I3, Clock, Clear);
DFF M2DFF (A2, I2, Clock, Clear);
DFF M1DFF (A1, I1, Clock, Clear);
DFF M0DFF (A0, I0, Clock, Clear);
endmodule

module DFF(output reg Q, input D, clk, clear);
always @(posedge clk, posedge clear)
if (clear == 0) Q <= 0; else Q <= D;
endmodule

module t_Reg_4_bit ();
wire A3_beh, A2_beh, A1_beh, A0_beh;
wire A3_str, A2_str, A1_str, A0_str;
reg I3, I2, I1, I0, Clock, Clear;

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- c. A Johnson counter with  $n$  flip-flops produces a sequence of many states?
- d. What is the characteristic equation for the complement output of a JK flip-flop?

**Q5.3 of the book**

$$5.3 \quad Q'(t+1) = (JQ' + K'Q)' = (J' + Q)(K + Q') = J'Q' + KQ$$

**Question 10 (8 points)**

Using D flip-flops,

**Q6.28 of the book**

6.28

Present state ABC	Next state ABC
000	001
001	010
010	100
011	xxx
100	110
101	xxx
110	000
111	xxx

180

$D_A = A \oplus B$

$D_B = AB' + C$

$D_C = A'B'C'$

Self-correcting

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graph TD
    111((111)) --> 110((110))
    001((001)) --> 110
    111 --> 010((010))
    001 --> 010
  
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- a. Design a synchronous counter with the following repeated binary sequence 0, 1, 2, 4, 6.

- b. Draw the logic diagram of the counter.



**Question 11 (11 points)**

Design a 3-bit ring counter using T Flip-flops. The initial value of the register is 100.  
Draw the logic diagram of the counter.

**Q6.x of the book**