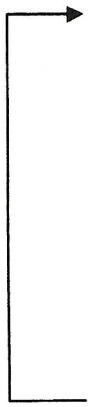
Question 4: (20 points)
Design a synchronous counter having the count sequence given by the following table. Use negative edge-triggered T flip-flops provided with a clock.



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	1	0	1
0	0	1	0
1	0	1	1
0	1	1	0
0	1	0	0
1	1	0	0
1	0	0	1
1	1	1	0

(i) Draw the state diagram of the counter.
(ii) Build the counter's state table showing the synchronous inputs of the T flip-flops as well.
(iii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the flip-flops; assume the next states of the unused combinations to be "don't care states"
(iv) Draw the logic diagram of the counter

Question 5: (15 points)

a) Design a serial Adder with JK Flip Flop and draw the corresponding logic circuit. The two binary numbers to be added, X and Y, are stored in two shift registers A and B respectively. The result (sum) of the adder must be stored in the register B. Use a full adder to add the two numbers. Answer the following questions

(i) Give a table that shows
   a. the inputs and outputs for the full adder
   b. the states (present and next) for the JK flip Flop
   c. The JK Flip Flop inputs
(ii) Obtain the logic expressions for the JK inputs and the outputs of the full adder
(iii) draw the logic circuit of the serial Adder (use a diagram to represent the full adder and the registers)