Université d'Ottawa
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Student Name (Please print)_____

Student Number_____ Section:_____

ITI1100-Digital Systems I

Examiners:
Professor Ahmed Karmouch
Professor Abdul Al-Dhaher

Date: April 16, 2008
Time: 3 hours

Instructions:

- Answer ALL questions.
- This is a close-book examination**.**
- Use the provided space to answer the following questions. If more space is needed, use the back of the page.
- Show all your calculations to obtain full marks.
- Calculators are allowed.
- Read all the questions carefully before you start.

(The following space is reserved for professor)

Question	Points	Percentage
1		15%
2		30%
3		15%
4		20%
5		20%
Total		100%

Question 1: (3 + 12 = 15 points)

(i) Convert the following two numbers into binary

$(2FC)_{16}$ =
$(142.16)_{10}$ =

(ii) The following two numbers are represented in unsigned binary:

A = $(10001)_2$
B = $(10010)_2$

Represent these two numbers in 1's complement form and perform the following binary arithmetic operations using the 1's complement method. Use a total of 7 bits to represent both numbers and results including the sign bit.

C = A + B;
D = -A – B.

Important note: ***Explain clearly your solution! Please note that if you give directly the result of the conversion of the two numbers in part (i)), without explaining the conversion method you have used, your mark for this part of the question will be zero!***

Question 2: (15+ 15 = 30 points)

Part A (10 + 5= 15 points):

A BCD to 7 segment decoder has 4 inputs (X, Y, Z, W) and 7 outputs (a, b, c, d, e, f, g) that select the correspondent segments of the LED display represented in the figure (a). The numeric representation of the decimal numbers is given in the figure (b) shown below.

(a) Segment designation display

(b) Numeric representation of decimal numbers on the LED

(a) Considering the decoder's outputs to being in "don't care" states (marked with "*d*" or "*X*") for any of the 6 unused input combinations,

(i) Find the minimized expression for the output ***c*** only;

(ii) Draw the logic diagram of the **two-level NOR** circuit that implements the above expression (***c***).

(b) Redo part (a) considering that your decoder has to display the letter *E* (*Error*) on the 7-segment display if any of the unused combinations is presented to the decoder's inputs

Note: You can use any type of gates with any number of inputs you may need. Assume, as well, that the input variables are available in both true and complemented form.

Part-B (5 + 10 = 15 points):

Given the following Boolean functions

$F_1(a,b,c) = \Sigma m(1,4,7)$ with don't care inputs $\Sigma d(0,2)$

$F_2(a,b,c,) = \Sigma m(2,1,5,6,)$

(i) Use a NAND (active low) implementation decoder with external NAND gates only to implement F1 in its product of sum form **(**Assume NAND gates with any number of inputs are available).

(ii) Use 2-to-4 decoders to build the necessary decoder to implement F_2. Use an external OR gate at the output of the decoder (Assume OR gates with any number of inputs are available) to implement F2 in it sum of products form.

Question 3: (4 + 8 + 1= 15 points)

Design a modulo-12 ripple (asynchronous) down-counter with T flip-flops and draw the corresponding logic circuit.

(i) Build the state diagram
(ii) Draw the logic circuit
(iii) What is the maximum modulus of the counter?

Question 4: (2 + 10 + 4 + 4 = 20 points)

Design a synchronous binary down counter using 4 negative edge-triggered JK flip-flops provided with a clock. The states (sequences) 0101; 1000; and 1010 are considered as unused states.

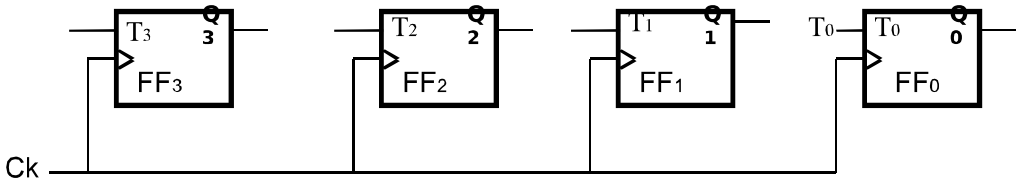
(i) Draw the state diagram of the counter.
(ii) Build the counter's state table showing the synchronous inputs of the JK flip-flops as well.
(iii) Using Karnaugh maps, find the minimal sum-of-products form of the equations for the inputs to the flip-flops; assume the next states of the unused combinations to be "don't care states"
(iv) Draw the logic diagram of the counter

Question 5: (8 + 5 + 5 +1 +1 = 20 points)

The figure below shows four T-type Flip-Flops clocked for synchronous counting. Using AND gates design a logic such that at the positive edge clock, FF_1 changes the states when $Q_0 = 1$, FF_2 changes the states when $Q_0Q_1 = 1$, and FF3 changes the states when $Q_0Q_1Q_2 = 1$

(i) Complete the figure below to include your logic with AND gates
(ii) What is the function of this circuit if $T_0 = 1$.
(iii) What is the function of this circuit if $T_0 = 0$.
(iv) What is the modulus of this counter
(v) What is the maximum modulus of this counter

40v



If needed, use this page and indicate the question number.