LECTURE 3

Introduction To
Microelectronics Fabrication Processes

Semiconductor Manufacturing Processes

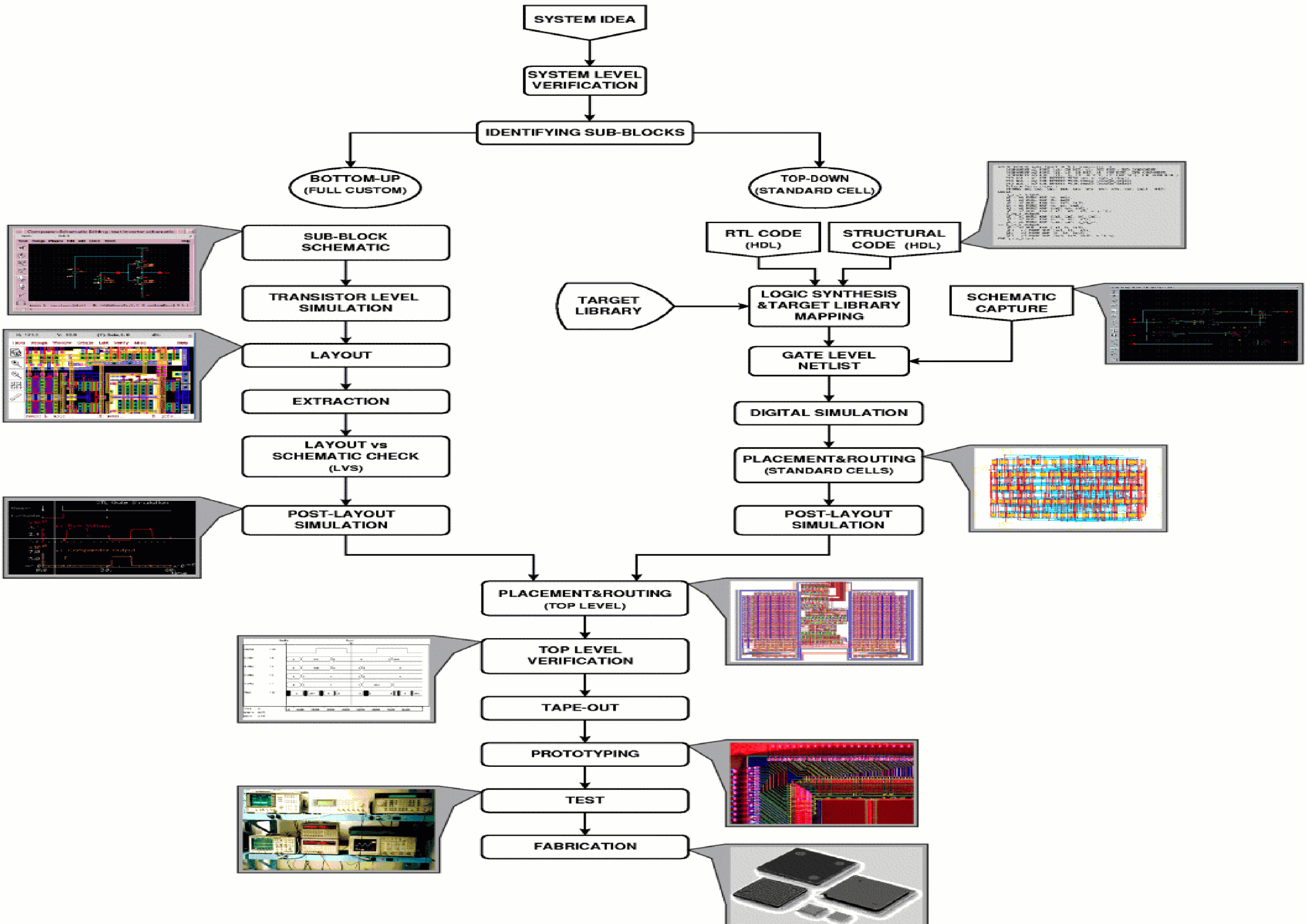
- **Design**
  - **Mask info to MASK-SHOP + GDSII file**
- **Mask making**
- **Generate runcard**
- **Wafer Preparation**
- **Front-end Processes (individual transistor)**
  - **Deposition**
  - **Oxidation**
  - **Diffusion**
  - **Photolithography**
  - **Etch (wet and dry)**
  - **Implantation**

- **Backend Process**
  - **Deposition (oxide, nitride etc)**
  - **Metalization**
  - **Rapid Thermal Process**
  - **Lithography & Etch**

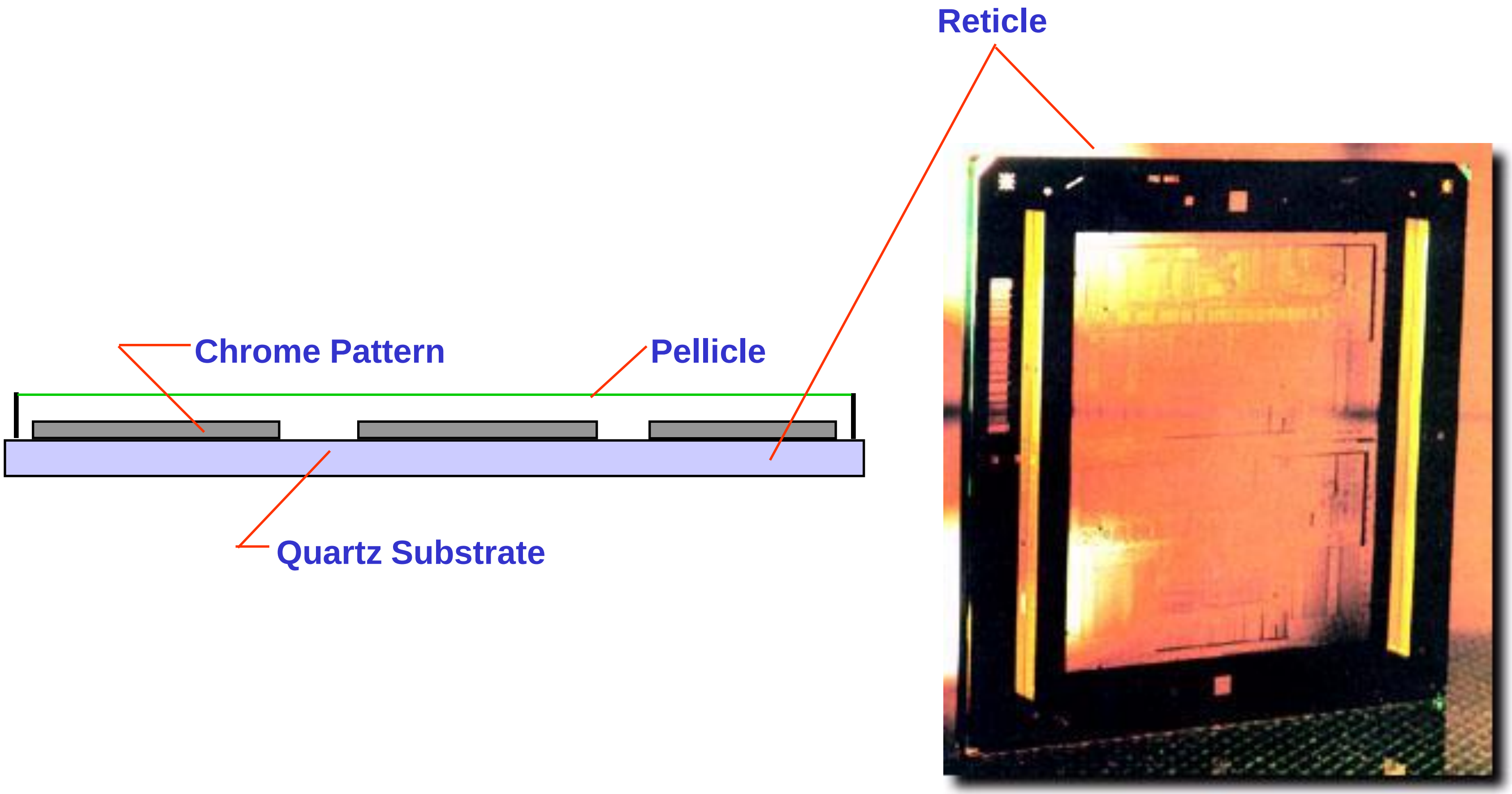
- **Test (Parametric and Functional)**

- **Packaging**

VLSI DESIGN FLOW

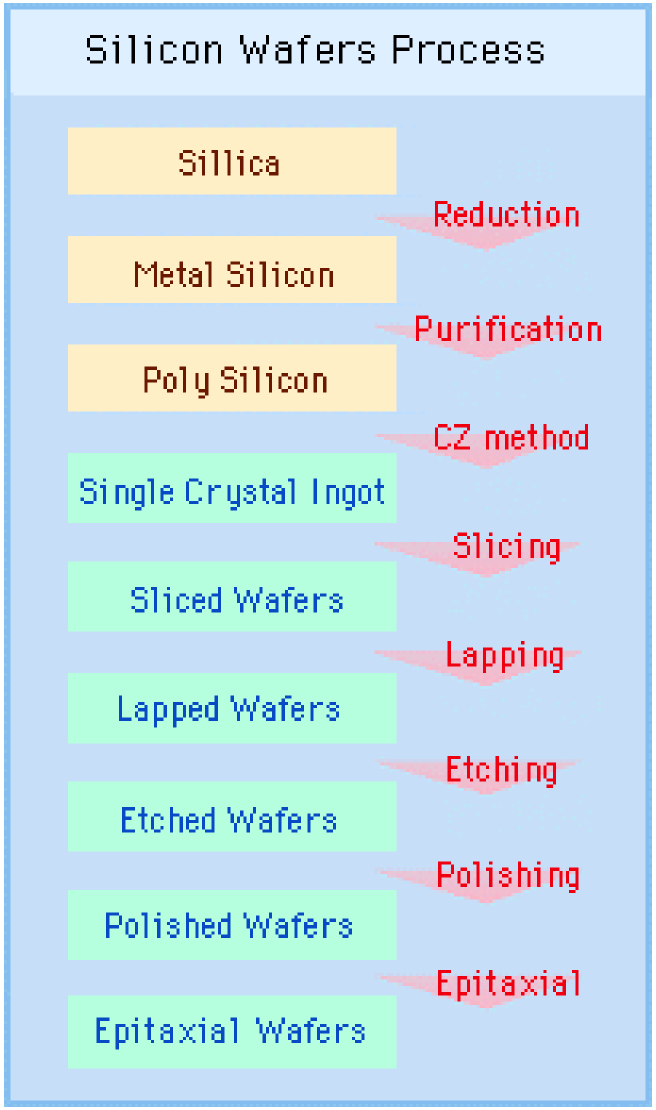


Pattern Preparation



Wafer Preparation

- Silicon Refining
- Crystal Pulling
- Wafer Slicing & Polishing
- Epitaxial Silicon Deposition



Silicon Refining

Chemical Reactions

Silicon Refining: $SiO_2 + 2\,C \rightarrow Si + 2\,CO$
Silicon Purification: $Si + 3\,HCl \rightarrow HSiCl_3 + H_2$
Silicon Deposition: $HSiCl_3 + H_2 \rightarrow Si + 3\,HCl$

Reactants

H_2

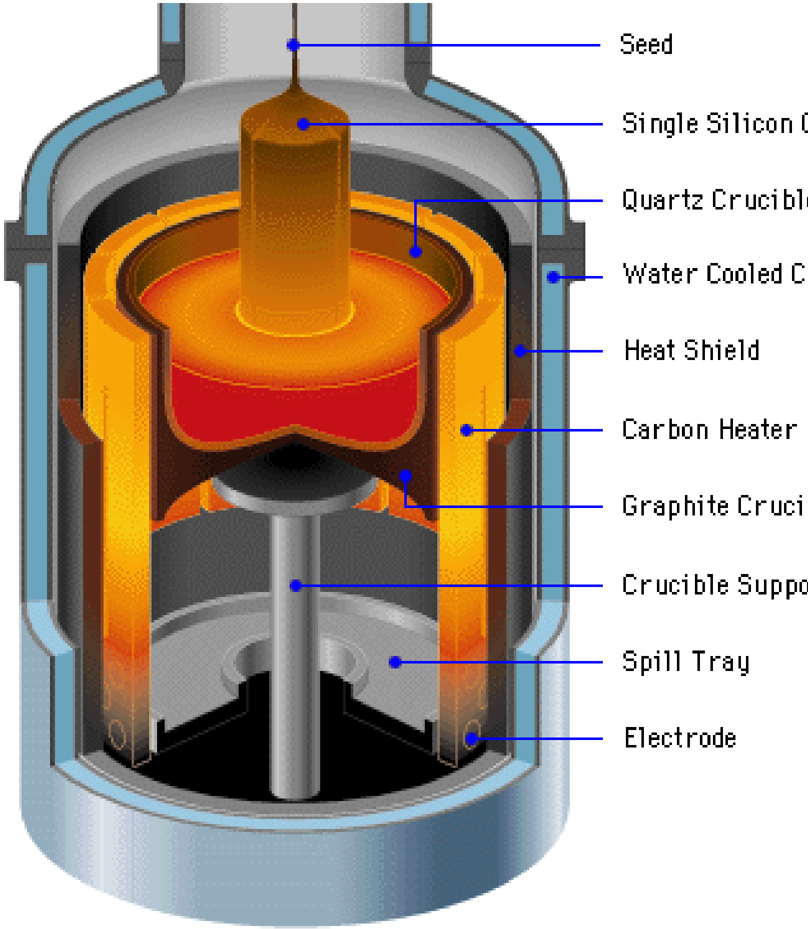
Silicon Intermediates

H_2SiCl_2
$HSiCl_3$

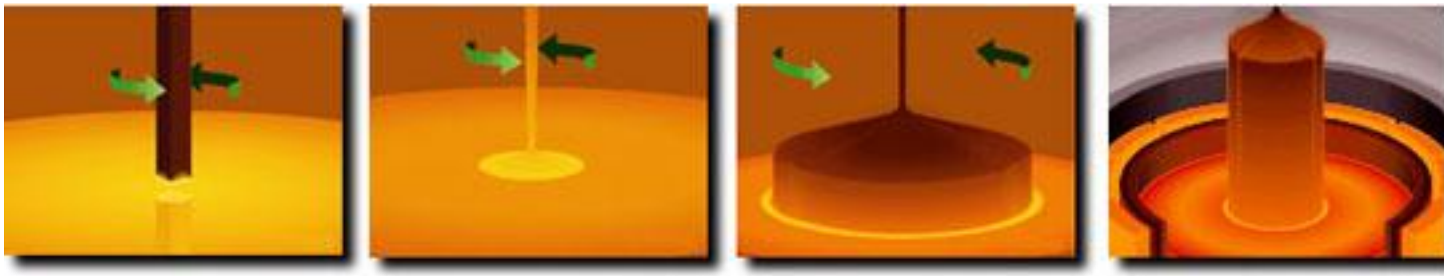
Silicon nugget inside crucible

Crystal Pulling

Czochralski Method
• Silicon quartzite are melted in quartz crucible
• Crucible is placed in high-temperature furnace
• Crystal seed is brought into contact with molten silicon
• The puller is slowly pull-up.
• Deposited silicon melt condenses and large rounded single crystal is formed



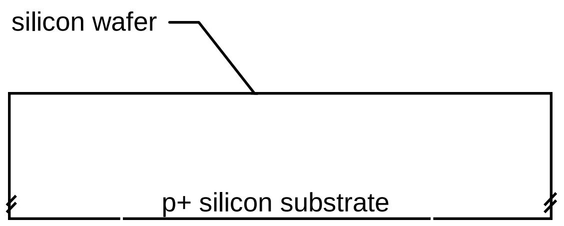
Single Crystal Growth

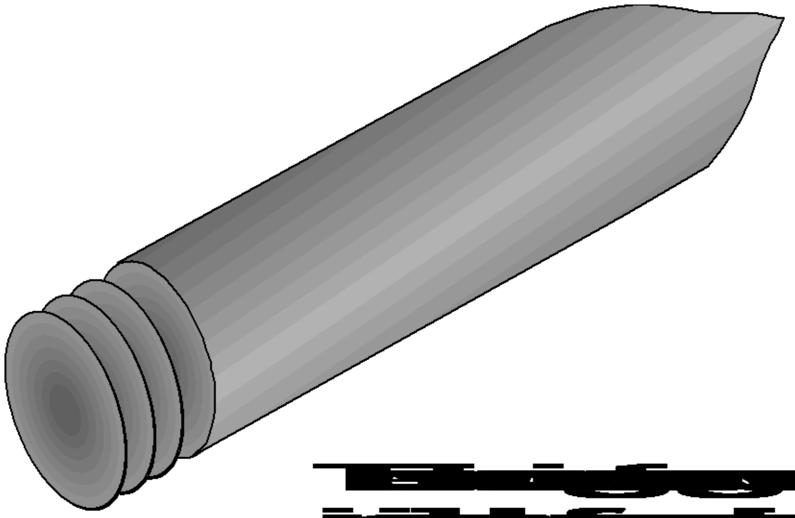


CZ Crystal Pullers
(Mitsubishi Materials Silicon)

Single Crystal Silicon Ingot

Wafer Slicing & Polishing

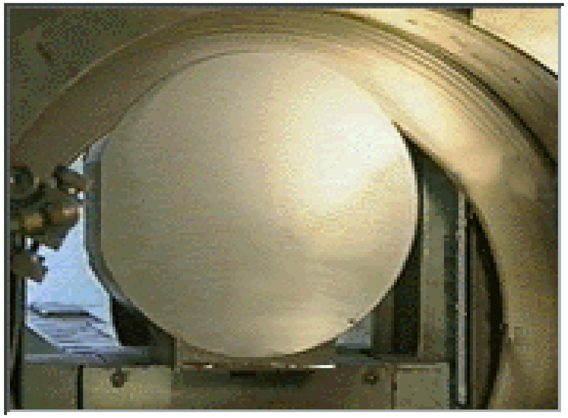


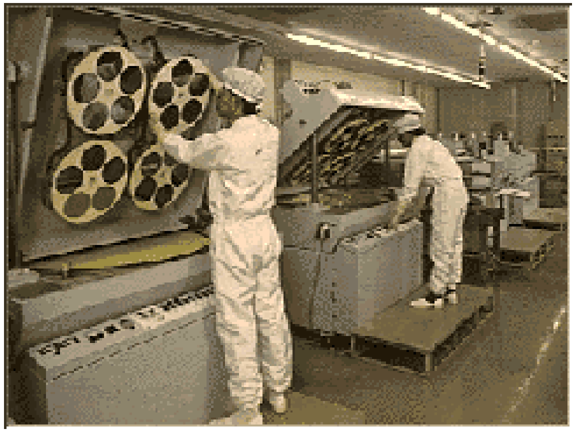


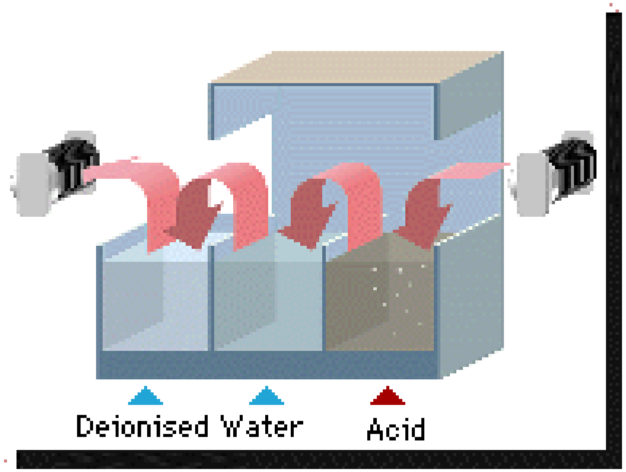
The silicon ingot is sliced into individual wafers, polished, and cleaned.

Wafer Polished

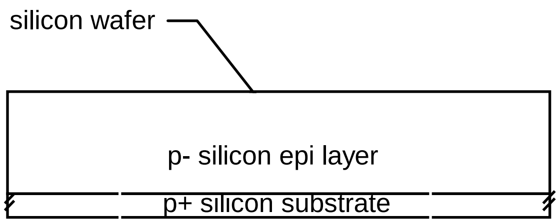
- Grinding
- Edge Polished
- Slicing
- Lapping
- Polished
- Process Control







Epitaxial Silicon Deposition



Chemical Reactions

Silicon Deposition: $HSiCl_3 + H_2 \rightarrow Si + 3\ HCl$

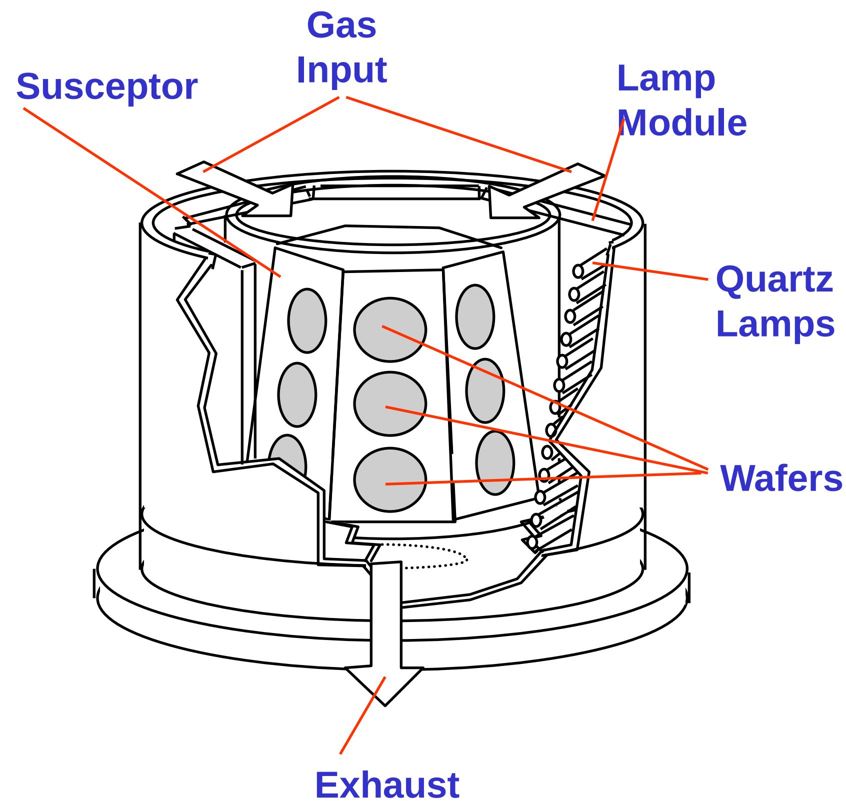
Process Conditions

Flow Rates: 5 to 50 liters/min

Temperature: 900 to 1,100 degrees C.

Pressure: 100 Torr to Atmospheric

Silicon Sources	Dopants	Etchant
SiH_4	AsH_3	HCl
H_2SiCl_2	B_2H_6	**Carriers**
$HSiCl_3$ *	PH_3	Ar
$SiCl_4$ *		H_2 *
		N_2



* High proportion of the total product use

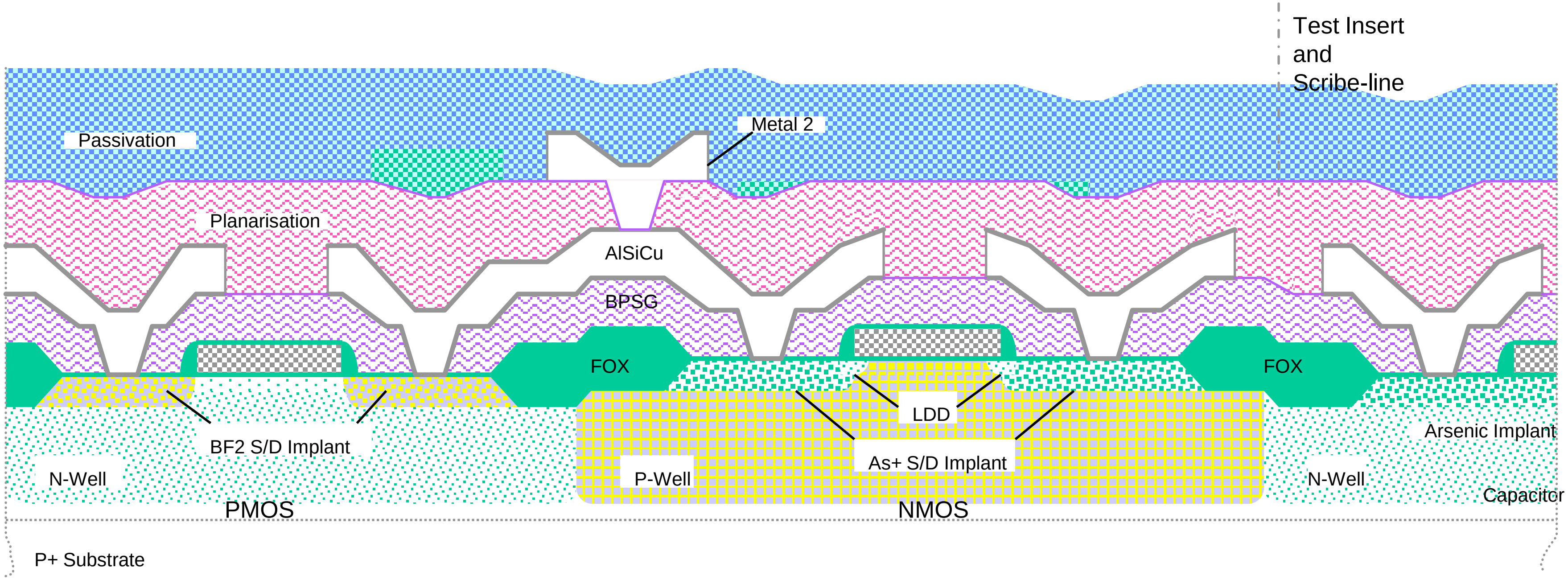
Front-End/Back-end Processes

Front-end

- **Fabrication steps up to the formation of individual transistors which electrically isolated**

Back-end

- **Fabrication steps to connect every single transistors until completed**



Front-end Process

- OXIDATION
- DIFFUSION
- DEPOSITION
- LITHOGRAPHY
- ION IMPLANTATION

OXIDATION

PURPOSE: TO GROW SILICON OXIDE FILM

WHAT IS OXIDATION?

A PROCESS OF ‘GROWING’ SILICON OXIDE ON A WAFER, EITHER ON BARE SILICON OR EXISTING SILICON OXIDE LAYER

PROCESS EQUATIONS

$Si + O_2$ SiO_2 (dry oxidation)

$Si + 2H_2O$ $SiO_2 + 2H_2$ (wet oxidation)

O_2/H_2O DIFFUSE TO SILICON WAFER/OXIDE LAYER AND REACT WITH Si

WHEN REACTION ON SURFACE IS DONE, THICKER FILM WILL REQUIRE THE REACTANT SPECIES TO DIFFUSE DEEPER INTO SILICON
(Deal-Groove Linear - Parabolic Model)

GENERALLY AT HIGH TEMPERATURE OF 600 - 1200 ºC.

GASES USED ARE BASICALLY O_2, OR H_2 AND O_2.

DILUTED PROCESS WHERE SMALL AMOUNT OF O_2 WITH N_2 AS DILUTER TO GET LOWER GROWTH RATE (FOR BETTER CONTROL OF VERY THIN OXIDE)

O_2 ALONE IS CALLED DRY OXIDATION

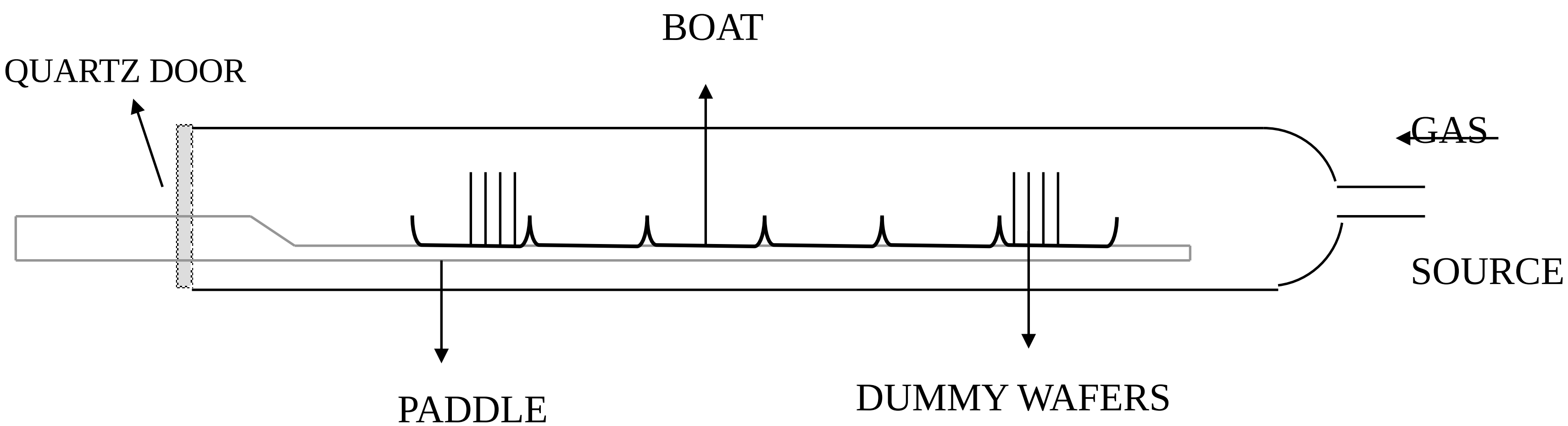
H_2 AND O_2 IS CALLED WET OXIDATION

FURNACE SYSTEM FOR OXIDATION

VERTICAL FURNACE

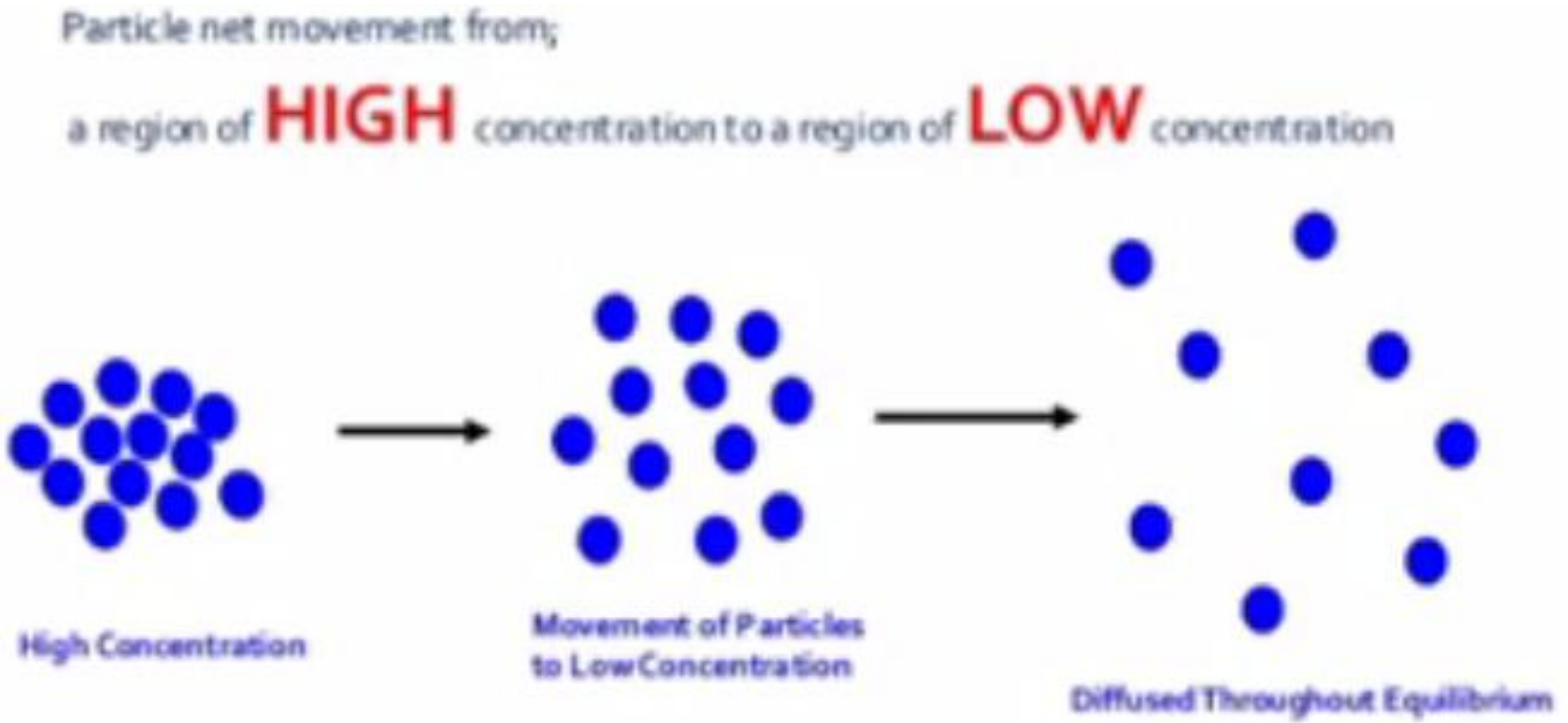
FURNACE SYSTEM FOR OXIDATION

HORIZONTAL FURNACE

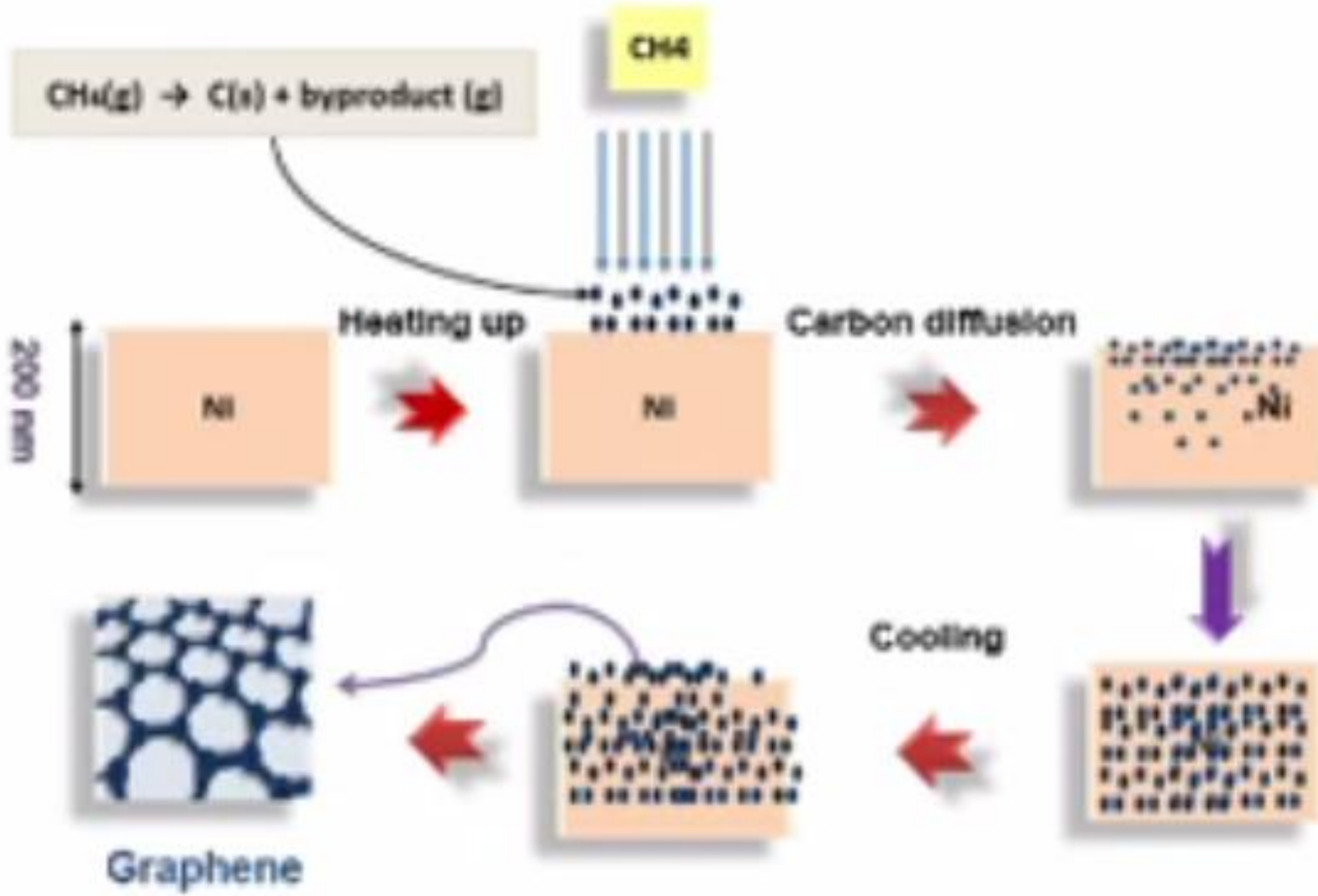

BOAT
QUARTZ DOOR
GAS
SOURCE
PADDLE
DUMMY WAFERS

DIFFUSION

PURPOSE: **TO DRIVE IN DOPANT INTO CERTAIN DEPTH IN SEMICONDUCTOR SUBSTRATE AFTER ION IMPLANTATION PROCESS OR SPIN ON DOPANT TECHNIQUE**



Epitaxial CVD Growth

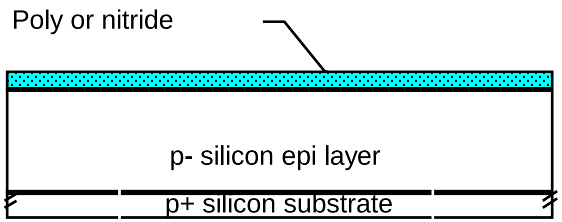


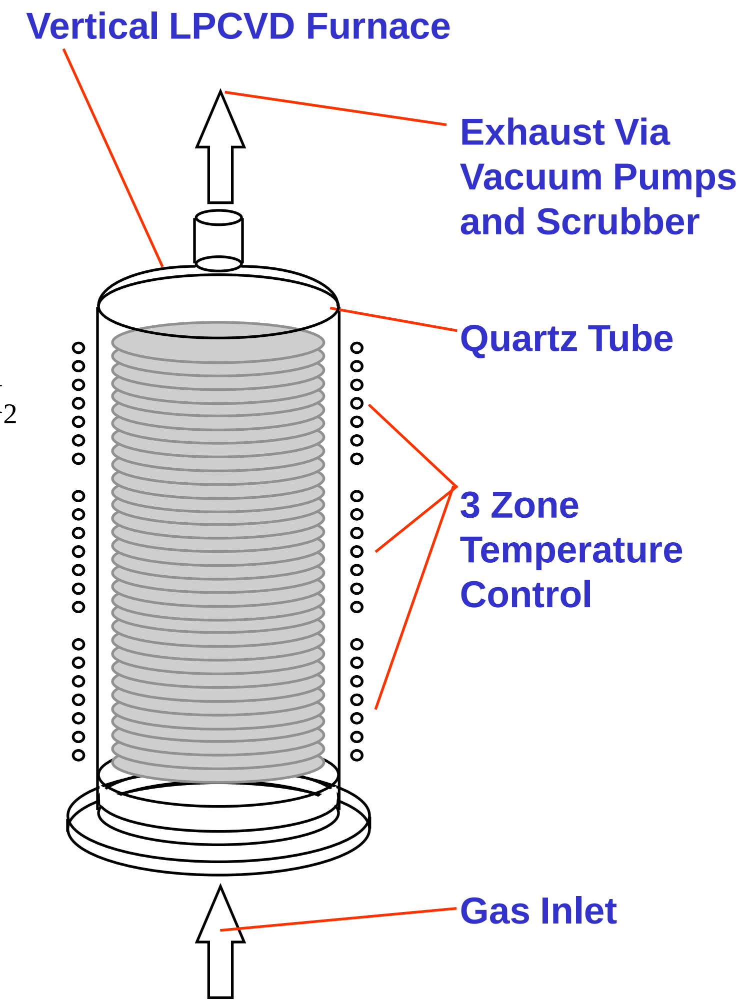
DEPOSITION

PURPOSE: **TO DEPOSIT MATERIALS SUCH AS NITRIDE, OXIDE, POLYSI ETC**

METHODS

- **PECVD**
- **LPCVD**
- **SACVD**
- **PVD**
- **EVAPORATION**





Chemical Reactions

Nitride Deposition: $3\ SiH_4 + 4\ NH_3 \rightarrow Si_3N_4 + 12\ H_2$

Polysilicon Deposition: $SiH_4 \rightarrow Si + 2\ H_2$

Process Conditions (Silicon Nitride LPCVD)

Flow Rates: 10 - 300 sccm

Temperature: 600 degrees C.

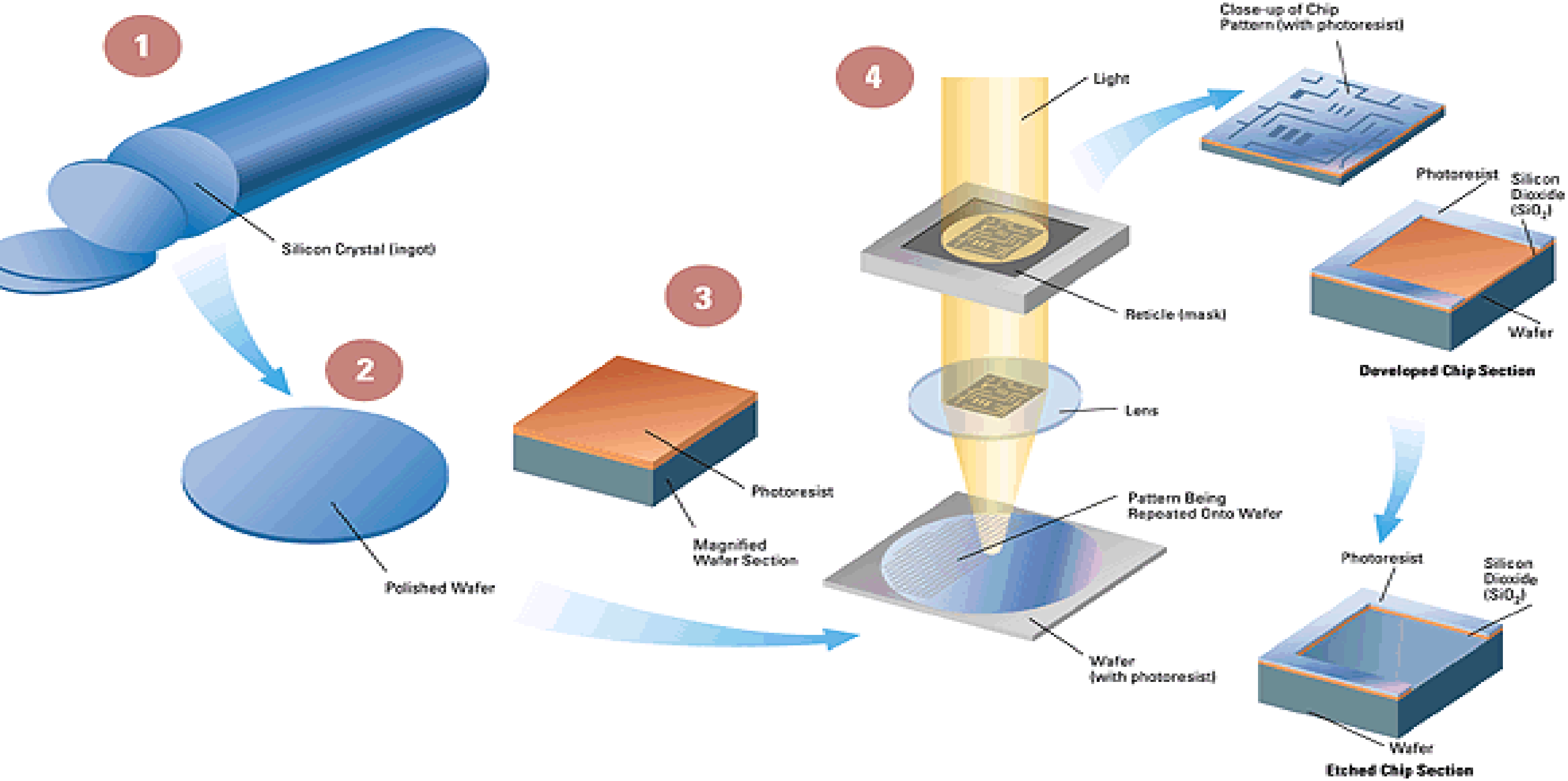
Pressure: 100 mTorr

Polysilicon	Nitride
H_2	NH_3 *
N_2	H_2SiCl_2 *
SiH_4 *	N_2
AsH_3	SiH_4 *
B_2H_6	$SiCl_4$
PH_3	

* High proportion of the total product use

PHOTOLITHOGRAPHY

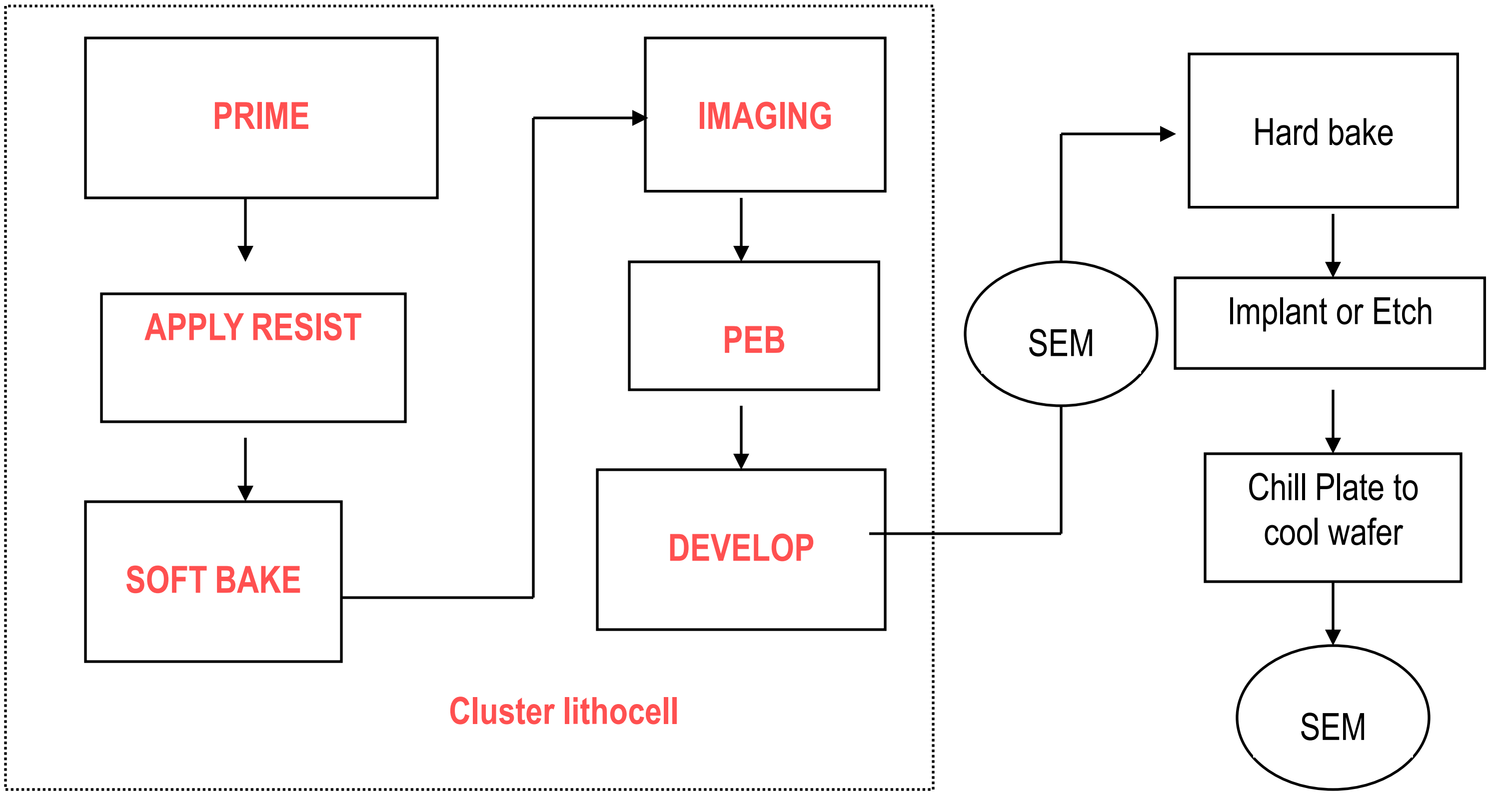
- **A process for producing highly accurate, microscopic, two dimensional patterns in a photosensitive material.**
- **These patterns are replicas of master pattern on a durable photomask, typically made of a thin patterned layer of chromium on a transparent glass plate.**
- **The process is repeated many times to build an integrated circuit**



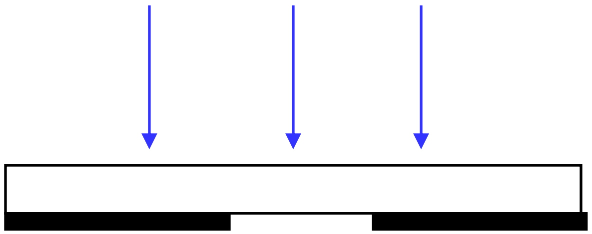
1
Silicon Crystal (ingot)
2
Polished Wafer
3
Photoresist
Magnified
Wafer Section
4
Light
Reticle (mask)
Lens
Pattern Being
Repeated Onto Wafer
Wafer
(with photoresist)
Close-up of Chip
Pattern (with photoresist)
Photoresist
Silicon
Dioxide
(SiO_2)
Wafer
Developed Chip Section
Photoresist
Silicon
Dioxide
(SiO_2)
Wafer
Etched Chip Section

Photolithography Process Flow

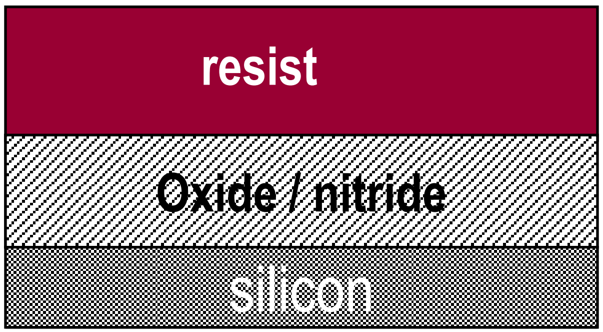
Nine basic microlithographic process steps



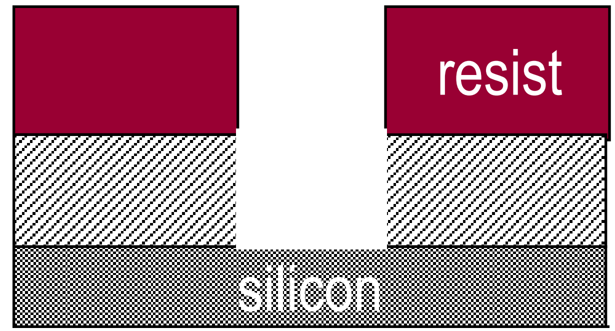
Photoresist Patterning



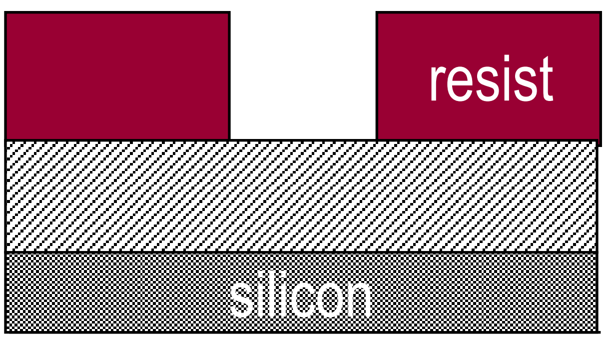
Photomask



Exposure



After etch

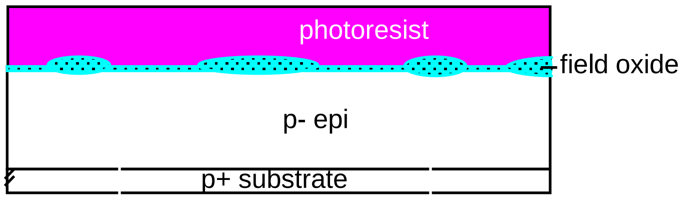


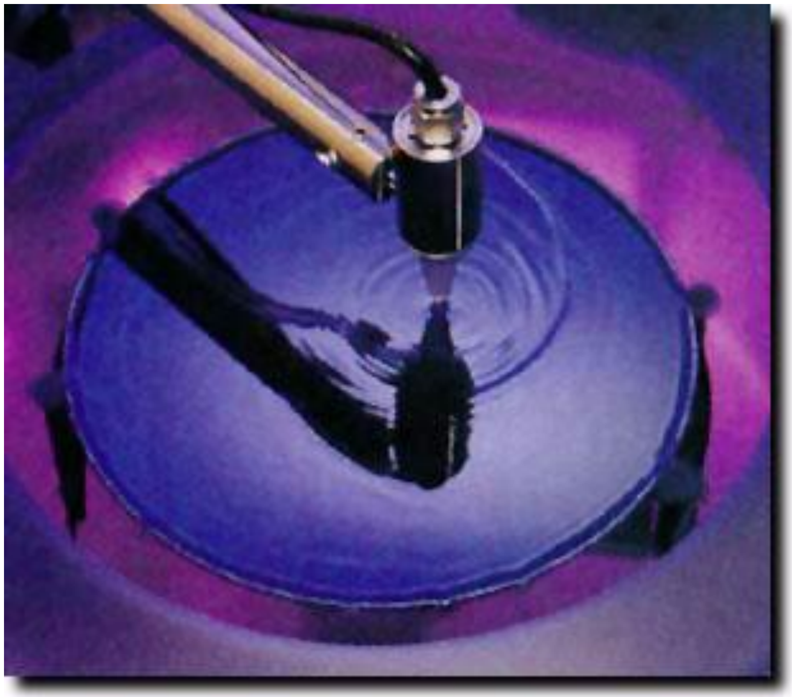
After development

Photolithography room

- **Photolithography area is yellow-lighted to prevent exposure of photoresist coated wafers to the light.**
- **It is a class-10 clean room and is the highest level of cleanliness in the clean room suite.**

Photoresist Coating Processes





Photoresists

- Negative Photoresist *
- Positive Photoresist *

Other Ancillary Materials (Liquids)

- Edge Bead Removers *
- Anti-Reflective Coatings *
- Adhesion Promoters/Primers (HMDS) *
- Rinsers/Thinners/Corrosion Inhibitors *
- Contrast Enhancement Materials *

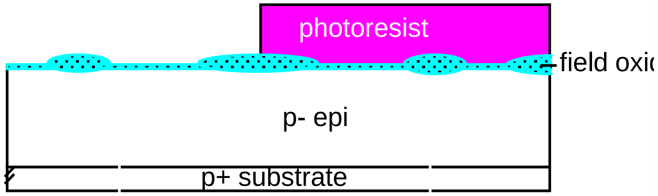
Developers

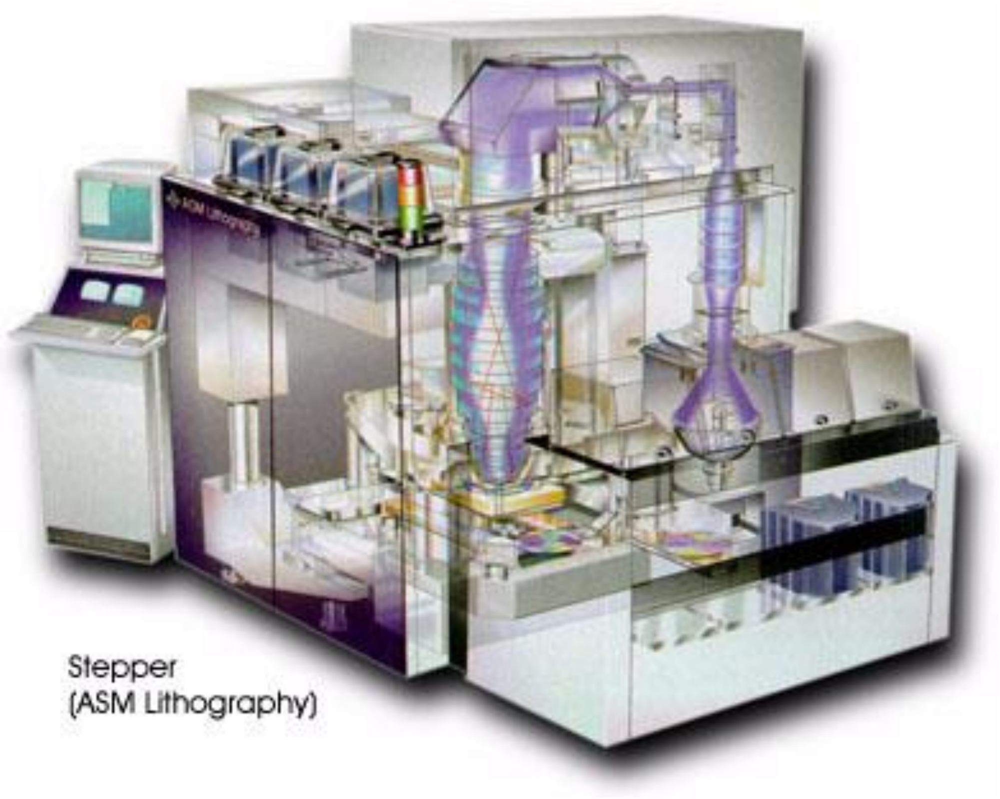
- TMAH *
- Specialty Developers *

Inert Gases

- Ar
- N_2

Exposure Processes





Expose

Kr + F_2 (gas) *

Inert Gases

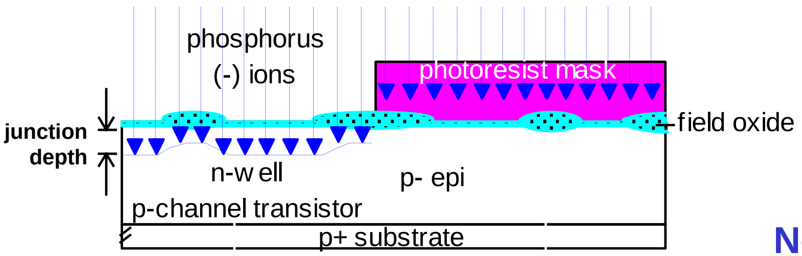
N_2

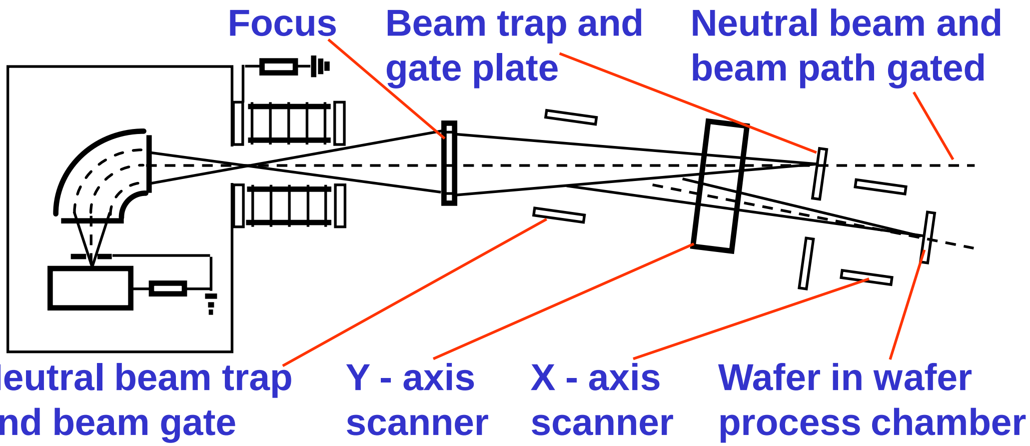
Ion Implantation

To introduce impurities into substrate by bombardments of ions

- Well Implants
- Channel Implants (Vt adjust)
- Source/Drain Implants

Ion Implantation





Process Conditions

Flow Rate: 5 sccm

Pressure: 10^{-5} Torr

Accelerating Voltage: 5 to 200 keV

Gases

Ar

AsH_3

$B^{11}F_3$ *

He

N_2

PH_3

SiH_4

SiF_4

GeH_4

Solids

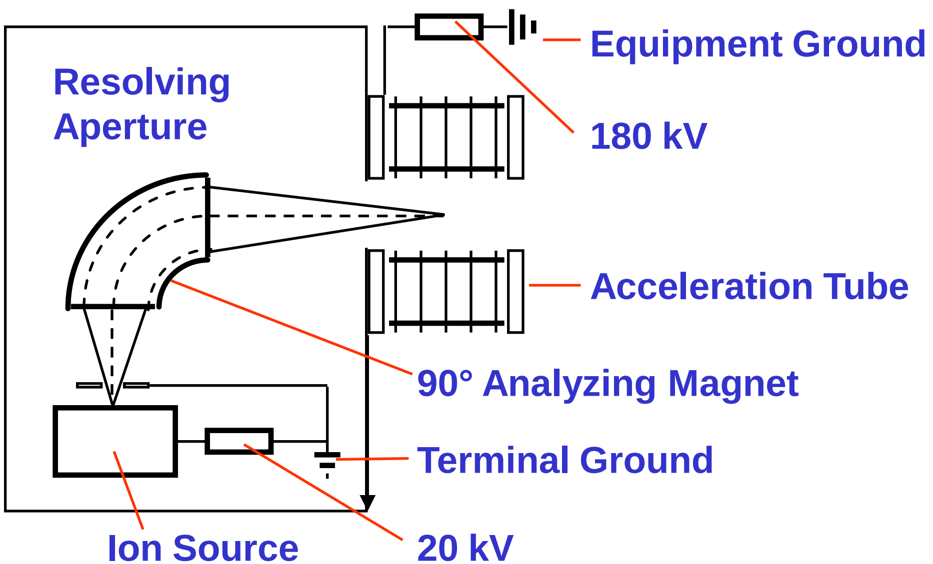
Ga

In

Sb

Liquids

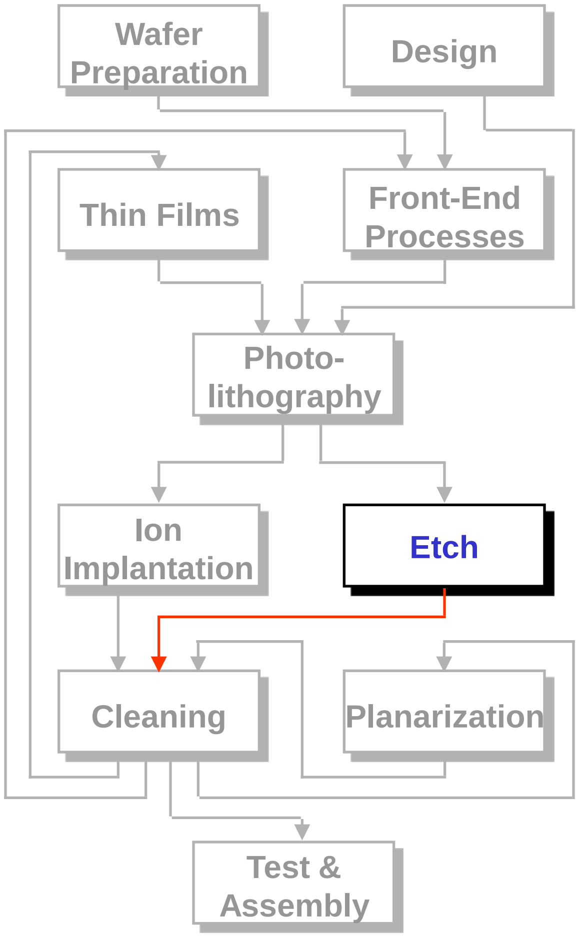
$Al(CH_3)_3$



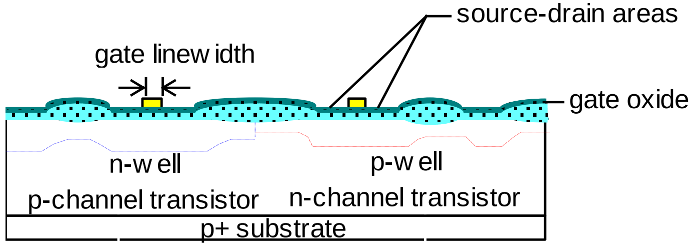
* High proportion of the total product use

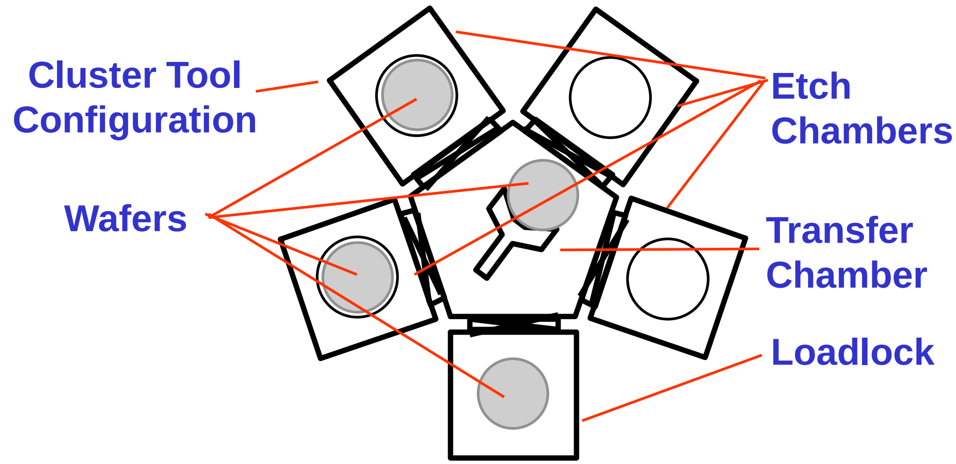
Etch

- Conductor Etch
  - Poly Etch and Silicon Trench Etch
  - Metal Etch
- Dielectric Etch



Conductor Etch





Chemical Reactions

Silicon Etch: $Si + 4\ HBr \rightarrow SiBr_4 + 2\ H_2$

Aluminum Etch: $Al + 2\ Cl_2 \rightarrow AlCl_4$

Process Conditions

Flow Rates: 100 to 300 sccm

Pressure: 10 to 500 mTorr

RF Power: 50 to 100 Watts

Polysilicon Etches

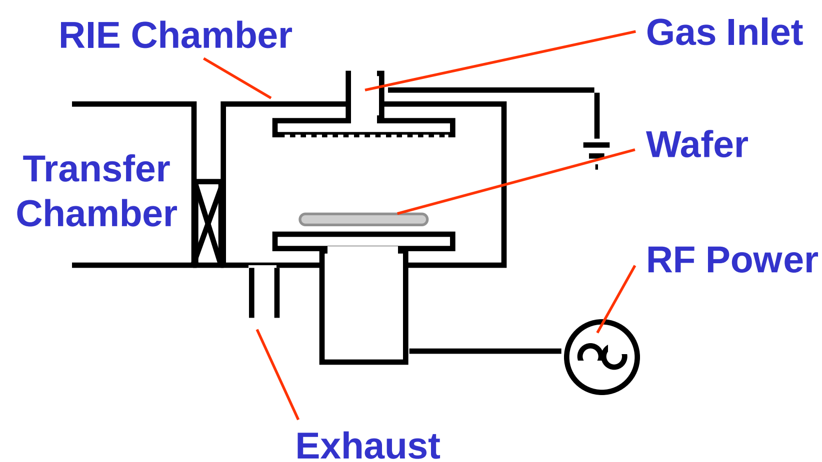
HBr *
C_2F_6
SF_6 *
NF_3 *
O_2

Aluminum Etches

BCl_3 *
Cl_2

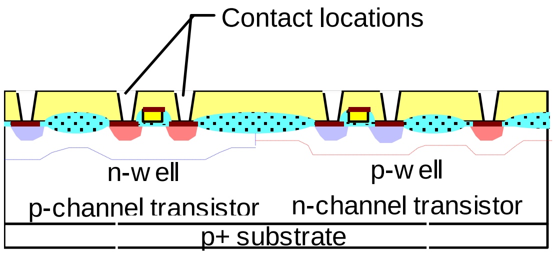
Diluents

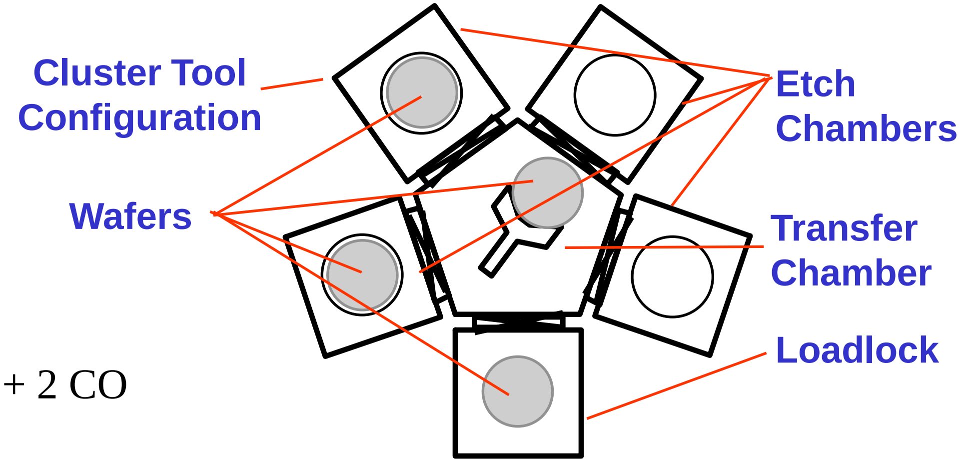
Ar
He
N_2



* High proportion of the total product use

Dielectric Etch





Chemical Reactions

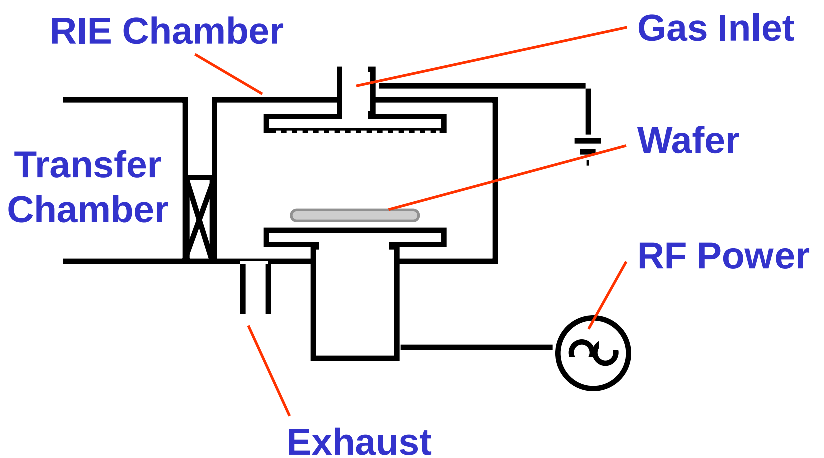
Oxide Etch: $SiO_2 + C_2F_6 \rightarrow SiF_4 + CO_2 + CF_4 + 2\ CO$

Process Conditions

Flow Rates: 10 to 300 sccm

Pressure: 5 to 10 mTorr

RF Power: 100 to 200 Watts

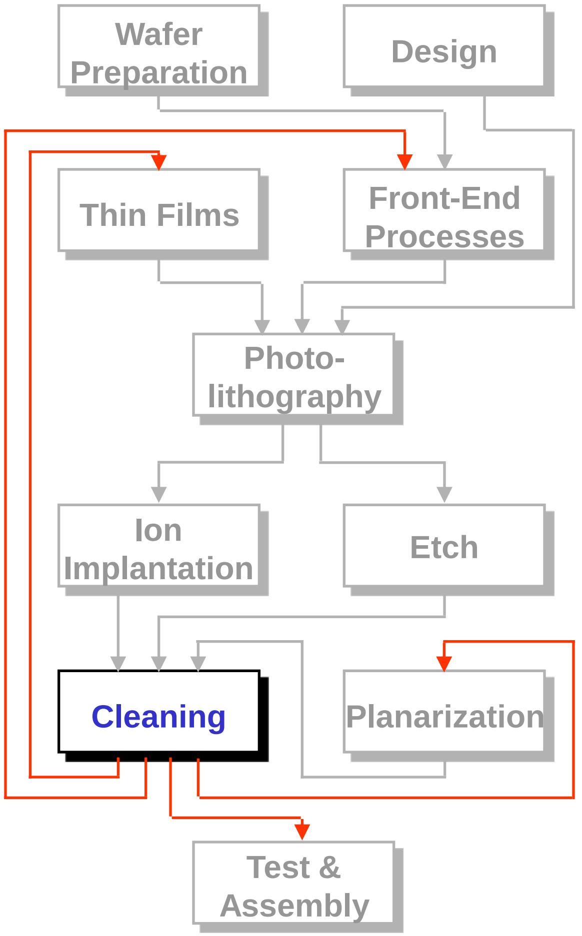


Plasma Dielectric Etches		Diluents
CHF_3 *	CO_2	Ar
CF_4	O_2	He
C_2F_6	SF_6	N_2
C_3F_8	SiF_4	
CO *		

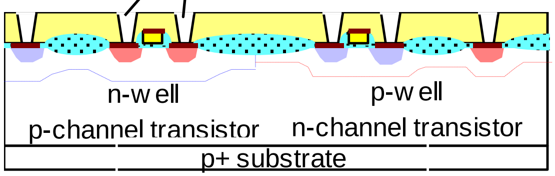
* High proportion of the total product use

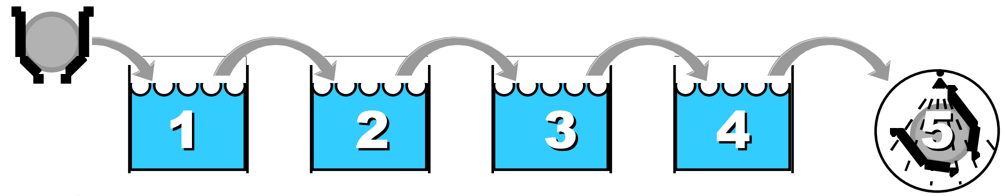
Cleaning

- Critical Cleaning
- Photoresist Strips
- Pre-Deposition Cleans



Critical Cleaning





1 Organics
H_2SO_4 +
H_2O_2
H_2O Rinse

2 Oxides
HF +
H_2O
H_2O Rinse

3 Particles
NH_4OH +
H_2O_2 + H_2O
H_2O Rinse

4 Metals
HCl +
H_2O_2 + H_2O
H_2O Rinse

5 Dry
H_2O or IPA +
N_2

Process Conditions

Temperature: Piranha Strip is 180 degrees C.

RCA Clean

SC1 Clean (H_2O + NH_4OH + H_2O_2) *
* SC2 Clean (H_2O + HCl + H_2O_2) *

Piranha Strip

* H_2SO_4 + H_2O_2 *

Nitride Strip

H_3PO_4 *

Oxide Strip

HF + H_2O *

Dry Strip

N_2O
O_2
CF_4 + O_2
O_3

Solvent Cleans

NMP
Proprietary Amines (liquid)

Dry Cleans

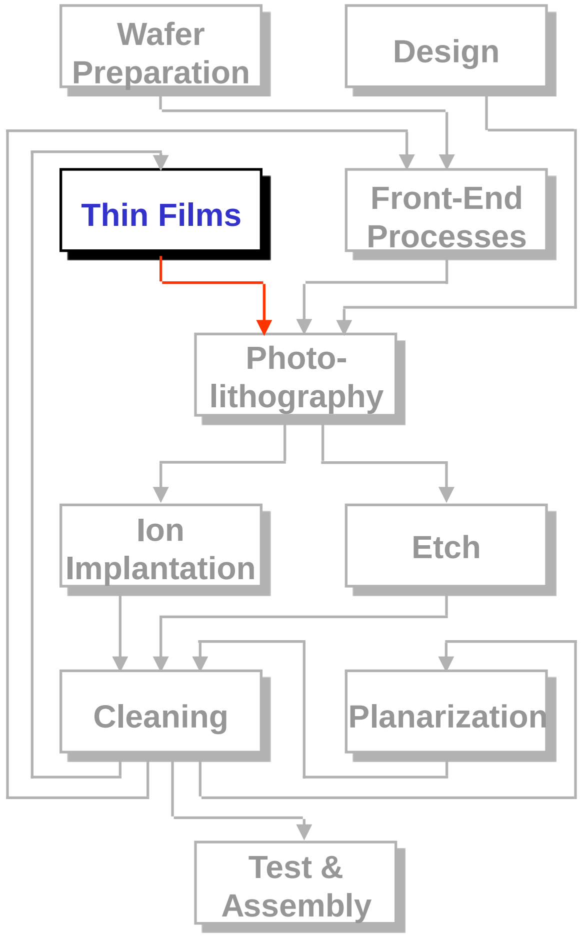
HF
O_2 Plasma
Alcohol + O_3

Back-end Process

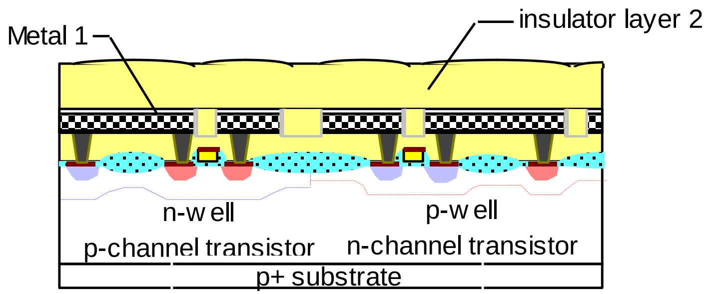
- CVD Dielectrics
- CVD Tungsten
- PVD Metal
- Planarization
    - local (deposit-etch)
    - global (CMP)

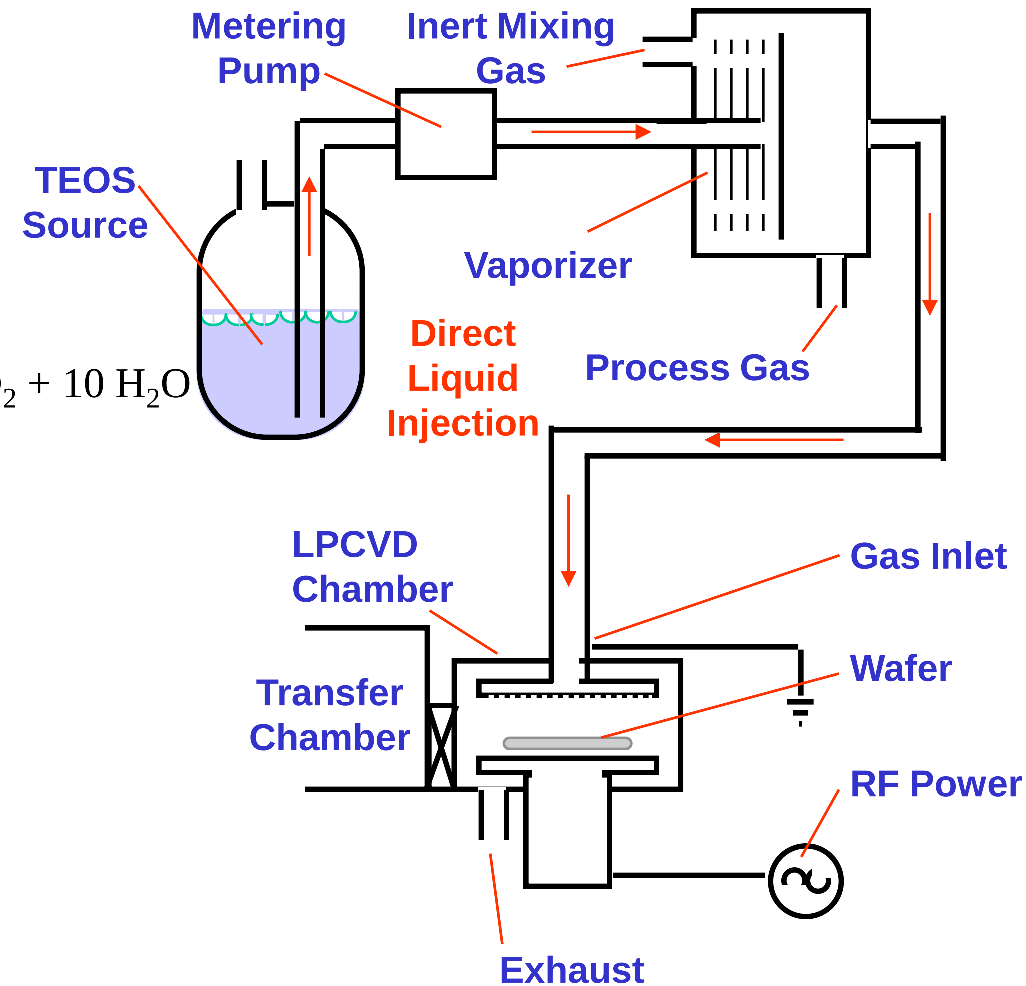
Thin Films

- Chemical Vapor Deposition (CVD) Dielectric
- CVD Tungsten
- Physical Vapor Deposition (PVD)
- Chamber Cleaning



Chemical Vapor Deposition (CVD) Dielectric





Chemical Reactions

$Si(OC_2H_5)_4 + 9\ O_3 \rightarrow SiO_2 + 5\ CO + 3\ CO_2 + 10\ H_2O$

Process Conditions (ILD)

Flow Rate: 100 to 300 sccm

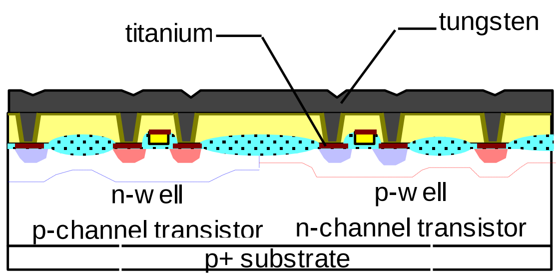
Pressure: 50 Torr to Atmospheric

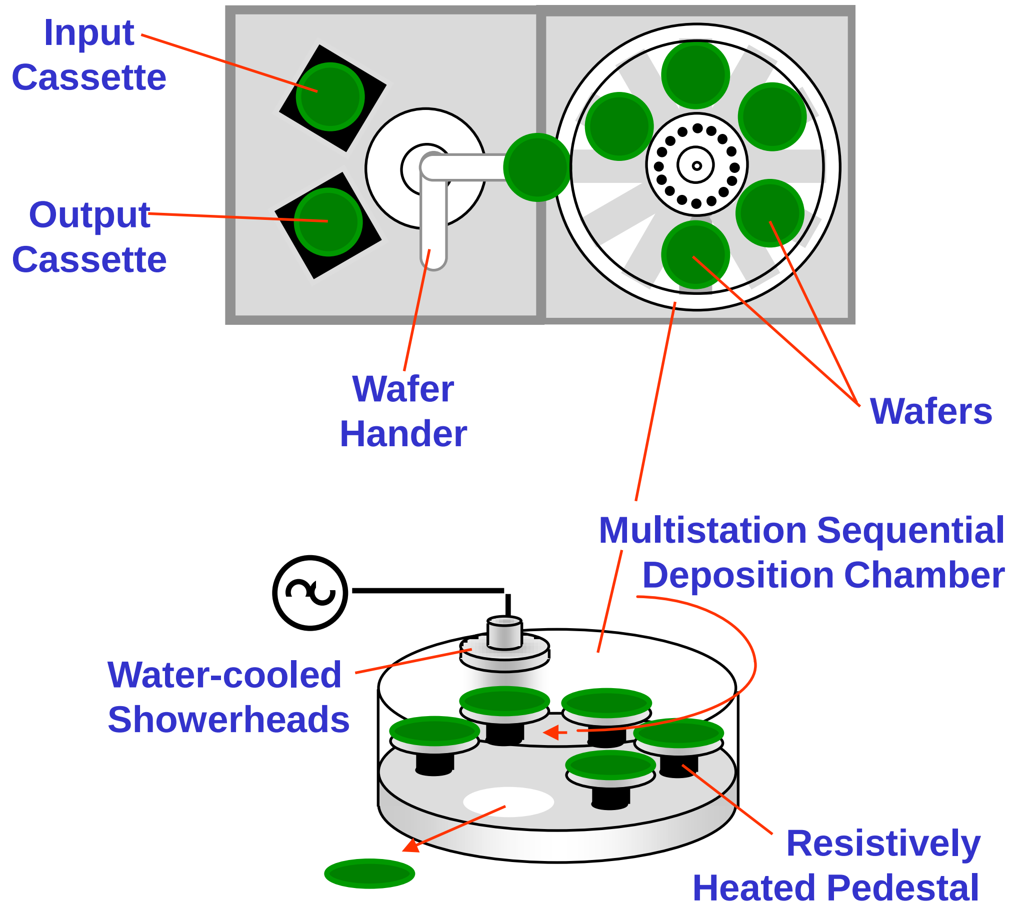
CVD Dielectric

O_2
O_3
TEOS *
TMP *

* High proportion of the total product use

Chemical Vapor Deposition (CVD) Tungsten





Chemical Reactions

$WF_6 + 3\ H_2 \rightarrow W + 6\ HF$

Process Conditions

Flow Rate: 100 to 300 sccm

Pressure: 100 mTorr

Temperature: 400 degrees C.

CVD Dielectric

WF_6 *

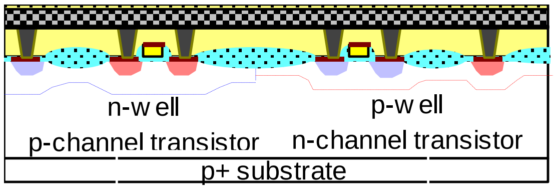
Ar

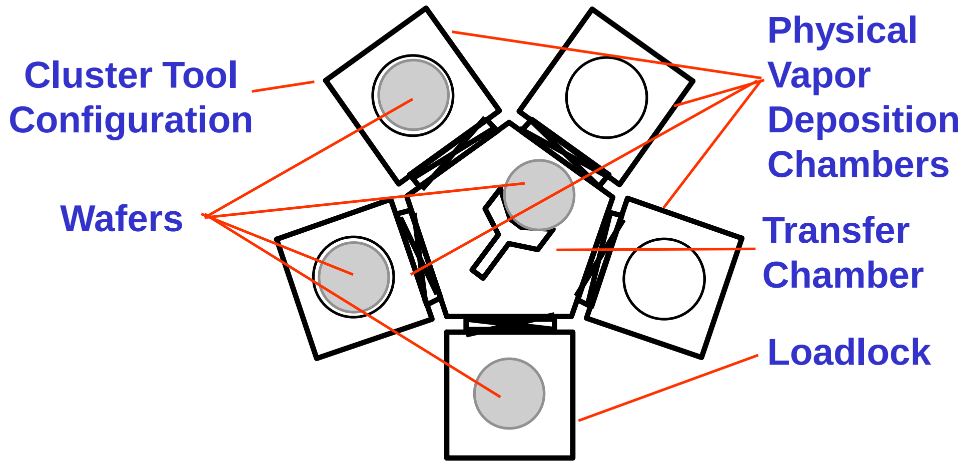
H_2

N_2

* High proportion of the total product use

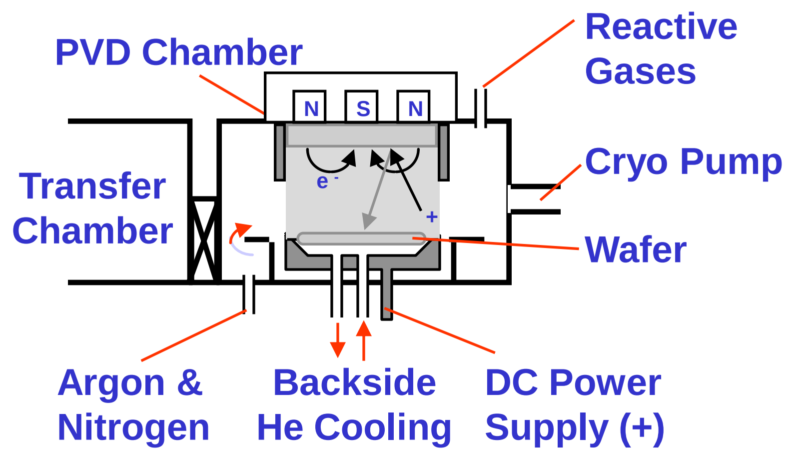
Physical Vapor Deposition (PVD)





Process Conditions

Pressure: < 5 mTorr
Temperature: 200 degrees C.
RF Power:

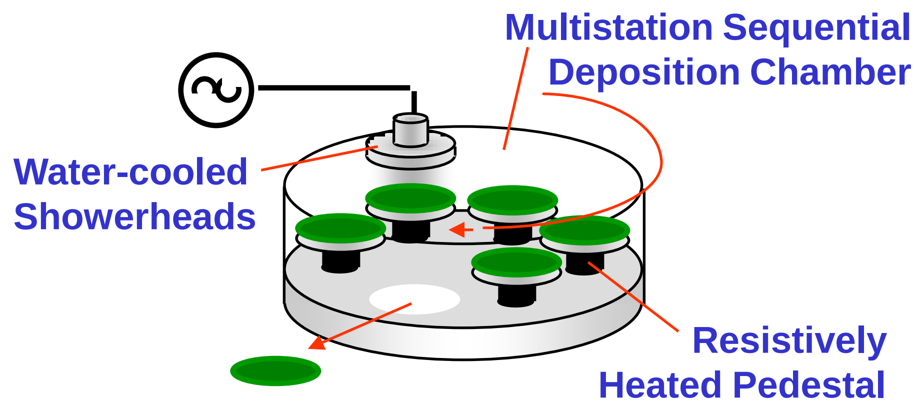


Barrier Metals

SiH_4
Ar
N_2
N_2
Ti PVD Targets *

* High proportion of the total product use

Chamber Cleaning



Chemical Reactions

Oxide Etch: $SiO_2 + C_2F_6 \rightarrow SiF_4 + CO_2 + CF_4 + 2\,CO$

Process Conditions

Flow Rates: 10 to 300 sccm

Pressure: 10 to 100 mTorr

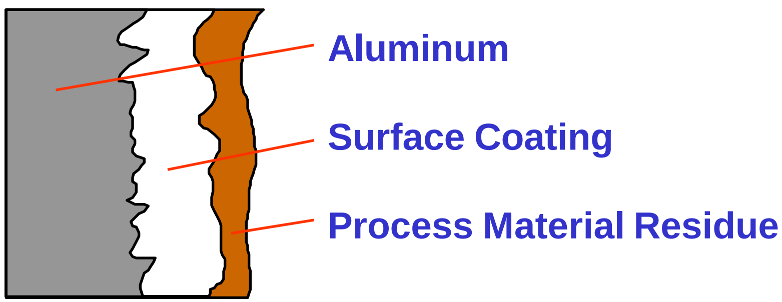
RF Power: 100 to 200 Watts

Chamber Cleaning

C_2F_6 *

NF_3

ClF_3

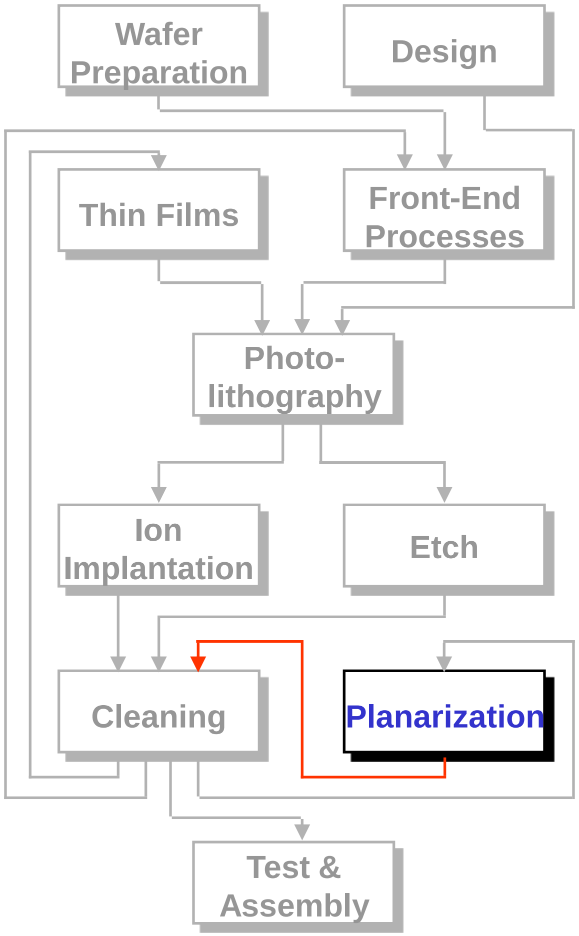


Chamber Wall Cross-Section

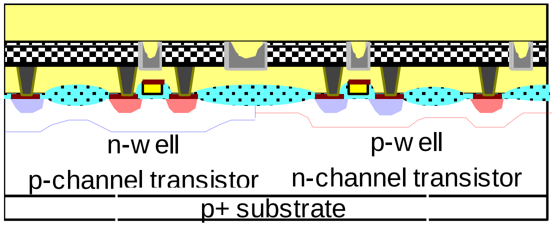
* High proportion of the total product use

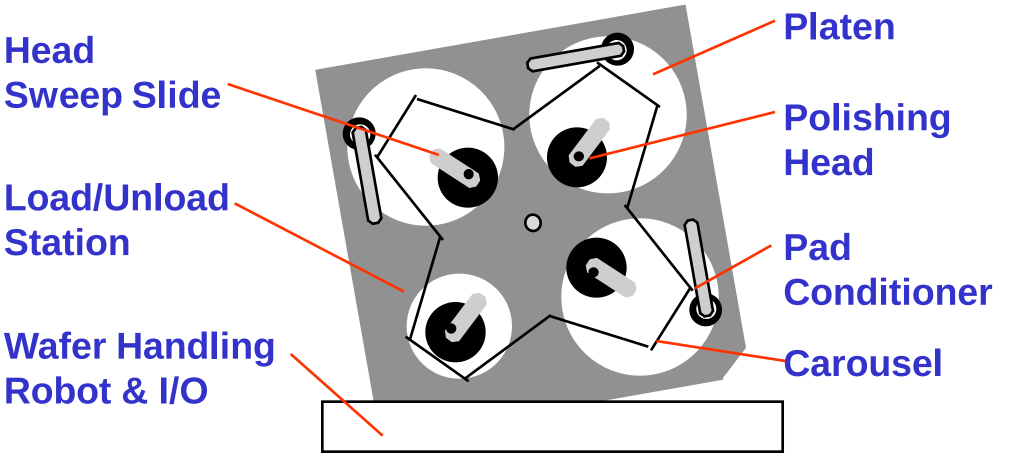
Planarization

- Oxide Planarization
- Metal Planarization



Chemical Mechanical Planarization (CMP)





Process Conditions (Oxide)

Flow: 250 to 1000 ml/min

Particle Size: 100 to 250 nm

Concentration: 10 to 15%, 10.5 to 11.3 pH

Process Conditions (Metal)

Flow: 50 to 100 ml/min

Particle Size: 180 to 280 nm

Concentration: 3 to 7%, 4.1 - 4.4 pH

Backing (Carrier) Film

Polyurethane

Pad

Polyurethane

Pad Conditioner

Abrasive

CMP (Oxide)

Silica Slurry *

KOH *

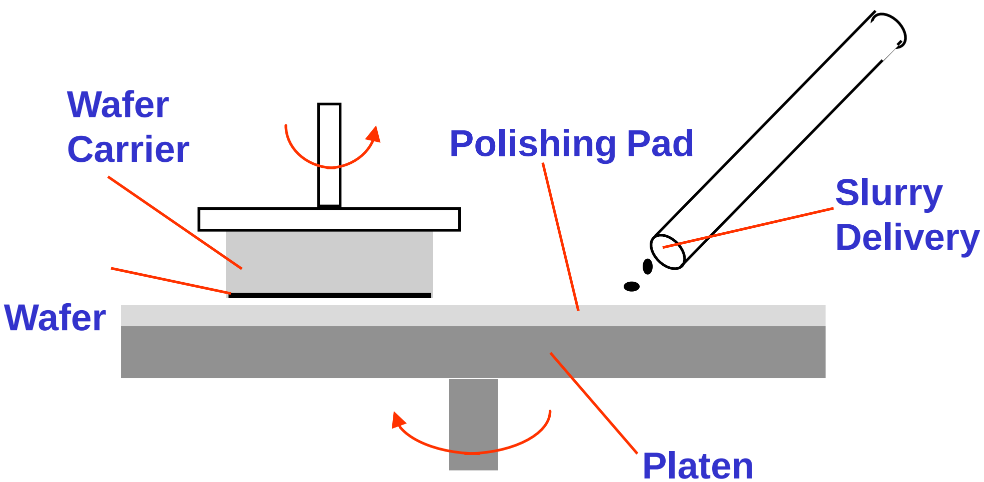
NH_4OH

H_2O

CMP (Metal)

Alumina *

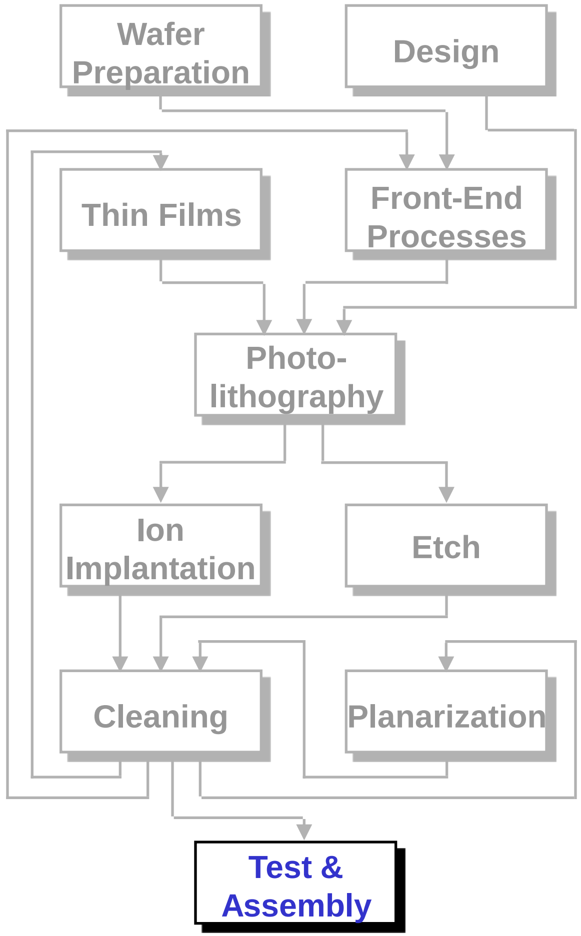
$FeNO_3$



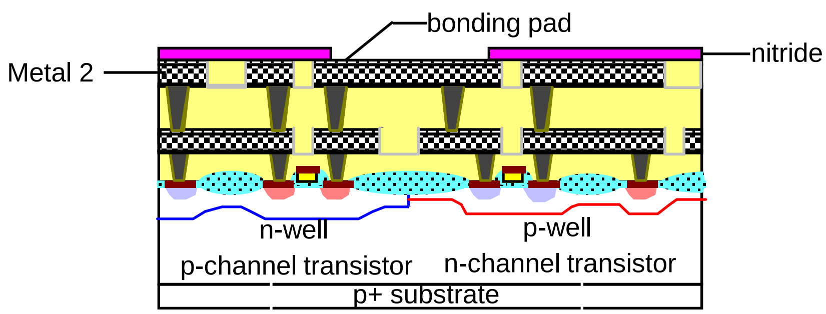
* High proportion of the total product use.

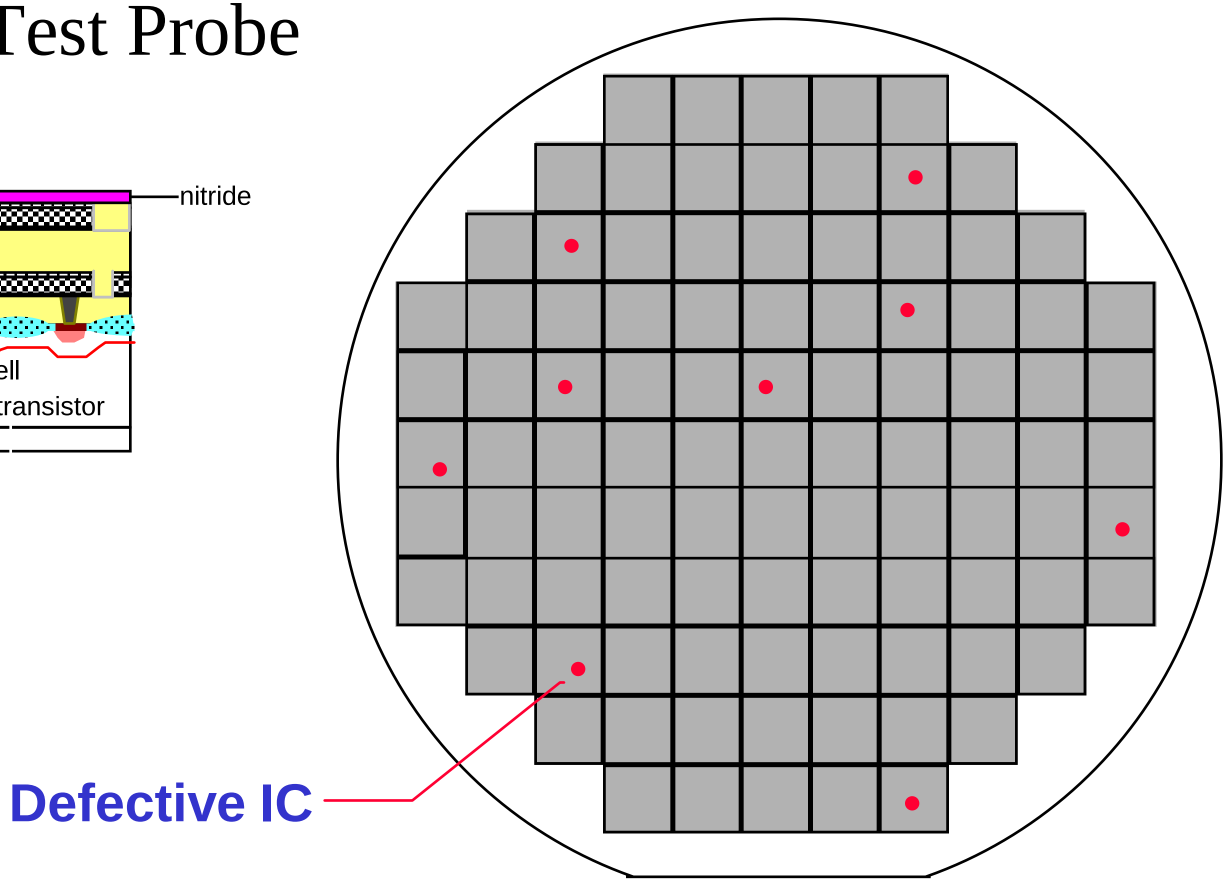
Test and Assembly

- Electrical Test Probe
- Die Cut and Assembly
- Die Attach and Wire Bonding
- Final Test



Electrical Test Probe

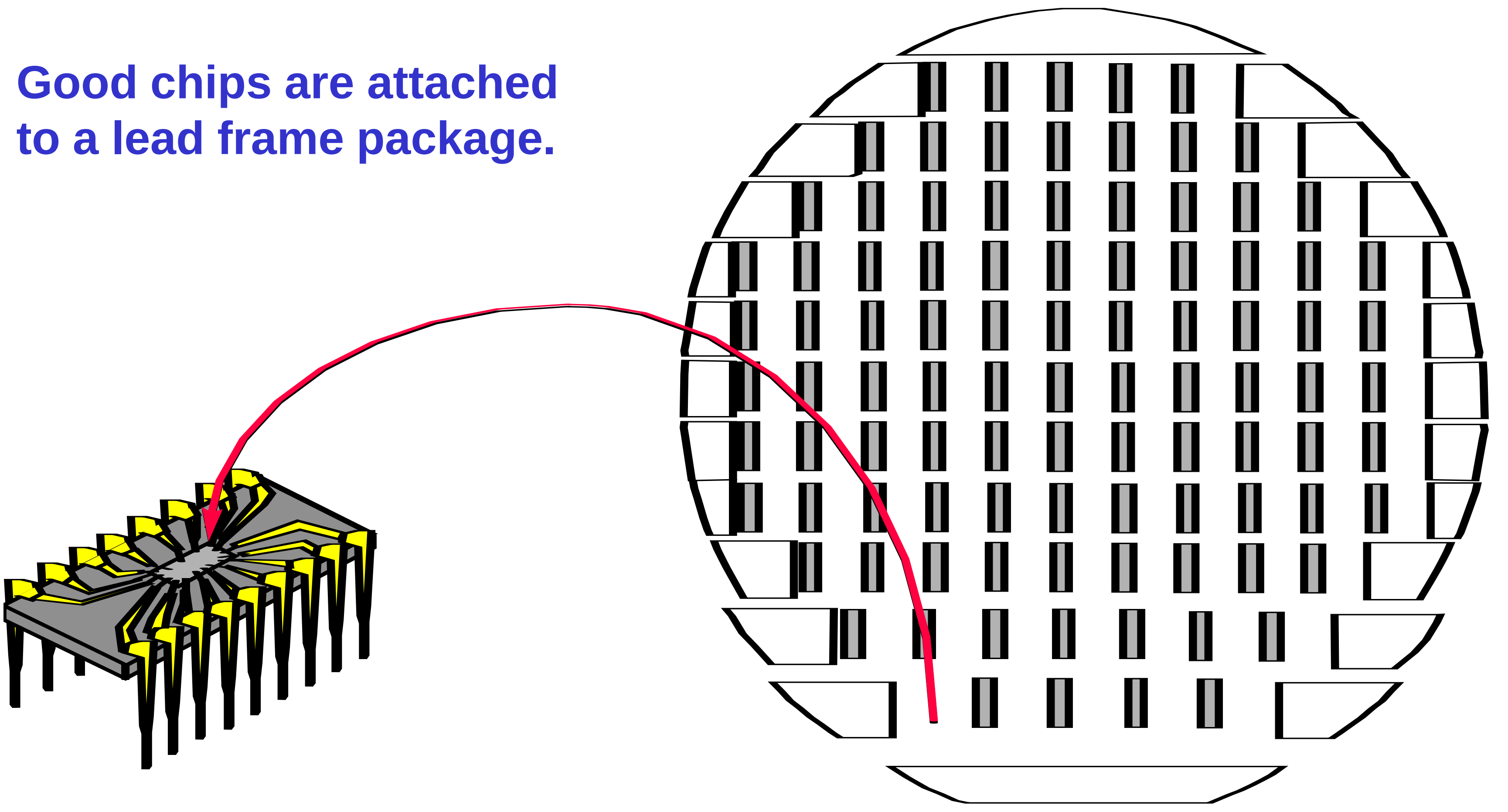




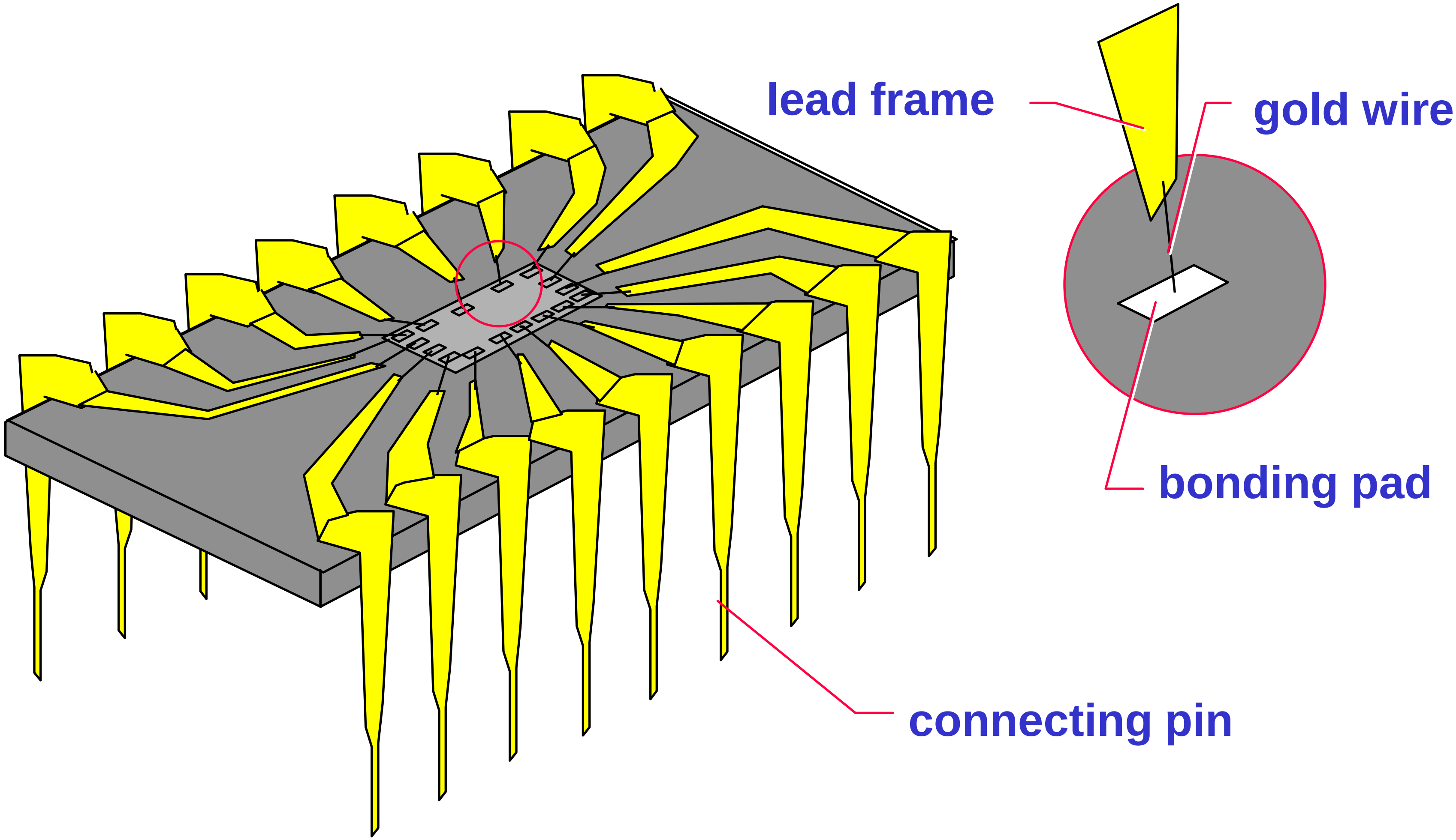
Individual integrated circuits are tested to distinguish good die from bad ones.

Die Cut and Assembly

Good chips are attached to a lead frame package.

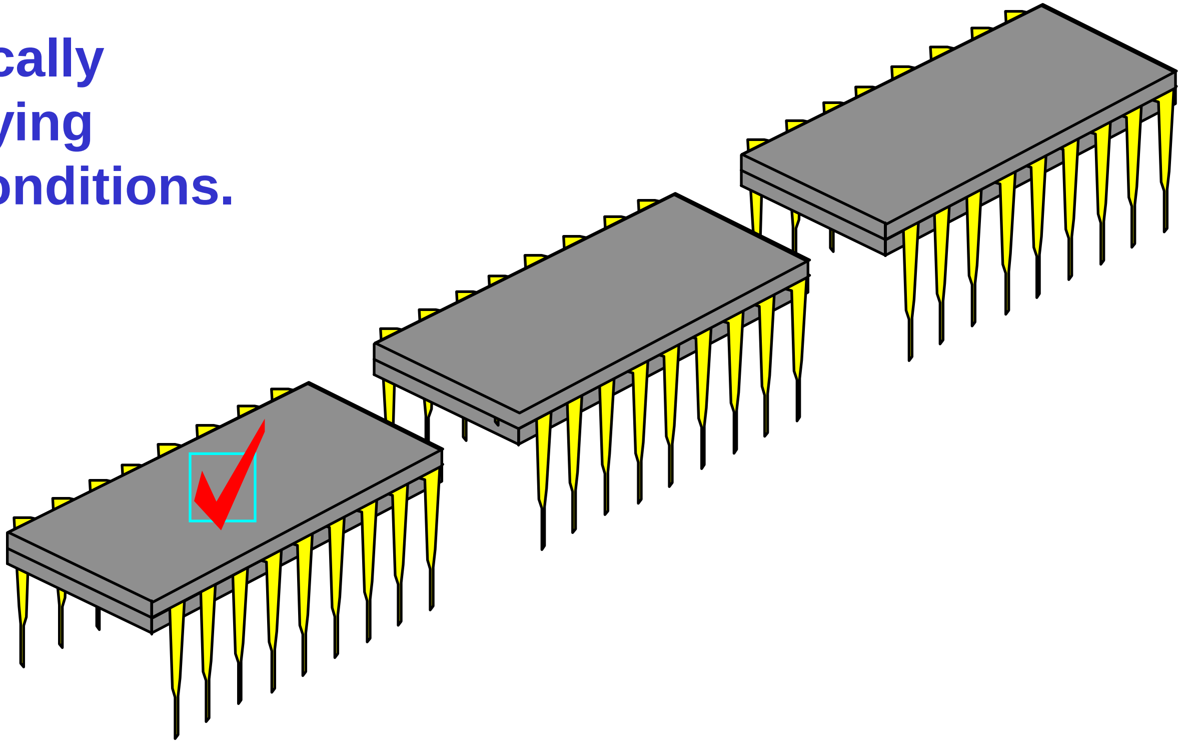


Die Attach and Wire Bonding



Final Test

Chips are electrically tested under varying environmental conditions.



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