Square Root Calculator

Nikolaos Dimou

1.12.2016

General Description

The Square Root Calculator is an area-efficient implementation of a fast converging square root algorithm. The Square root calculator is pipelined in order to provide high throughput results. The arithmetic calculation performed is:

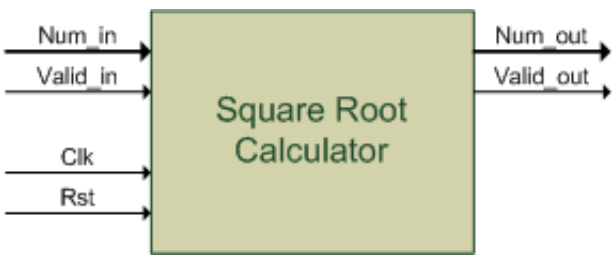
$$output = \sqrt{input}$$

Design was based on [1].The implemented algorithm is based on the bisection method presented by E. W. Dijkstra for approximating the square root of a given non-negative integer x. Result can be rounded instead of truncated with minor changes.

Features

- VHDL description
- Device - independent description.
- No DSPs, BRAMS used.
- Parametric input resolution.
- Truncated result.
- Latency: If 2N is input's resolution,then $Latency = N$ clock cycles.

Block Diagram



I/O pins

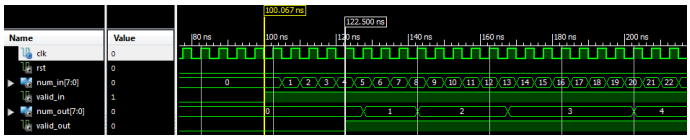
- Input Pins
  - clk: clock.
  - rst: reset.
  - num_in: non-negative integer (**parametric, must be even**).
  - valid_in= 1-bit valid signal.
- Output Pins
  - num_out: Result (**same resolution as input**.
  - valid_out: 1-bit valid signal.

Implementation

The design was sucessfully implemented in XC7K325T-2FFG900C FPGA chip.

	8-bit	16-bit	20-bit	32-bit
LUTs	48	278	489	1426
FFs	46	174	267	666
Freq.(MHz)	605.33	364.30	338.07	294.55

Testbench screenshot



References

[1] Matti T. Tommiska, *Area-efficient implementation of a fast square root alorithm*, IEEE, 2000.