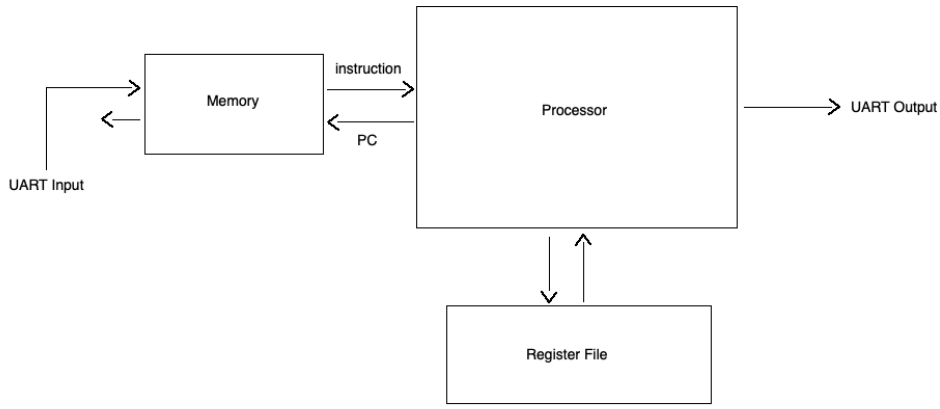
EE789: Processor
Dimple Kochar: 16D070010

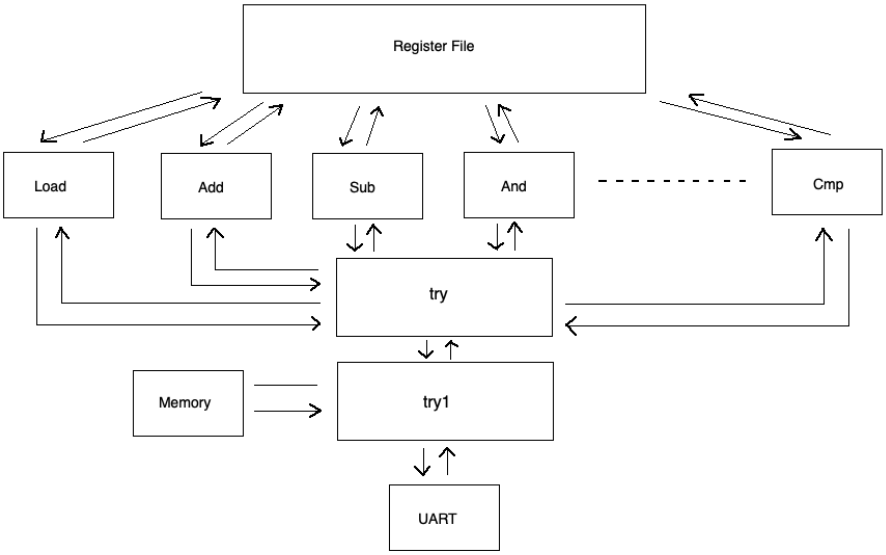
Overview:
Design a processor with the given instruction set architecture.

Implementation:
I did two implementation in Aa.
First being a single module with different statements all conditionally implemented using $guard



This processor however resulted in about 2k bits being added as buffer. On testing it worked fine, but with vivado, it just got stuck during synthesis and my laptop hanged.

So, I had to write another implementation of the processor using different modules for each instruction and reduced the buffering to 0.

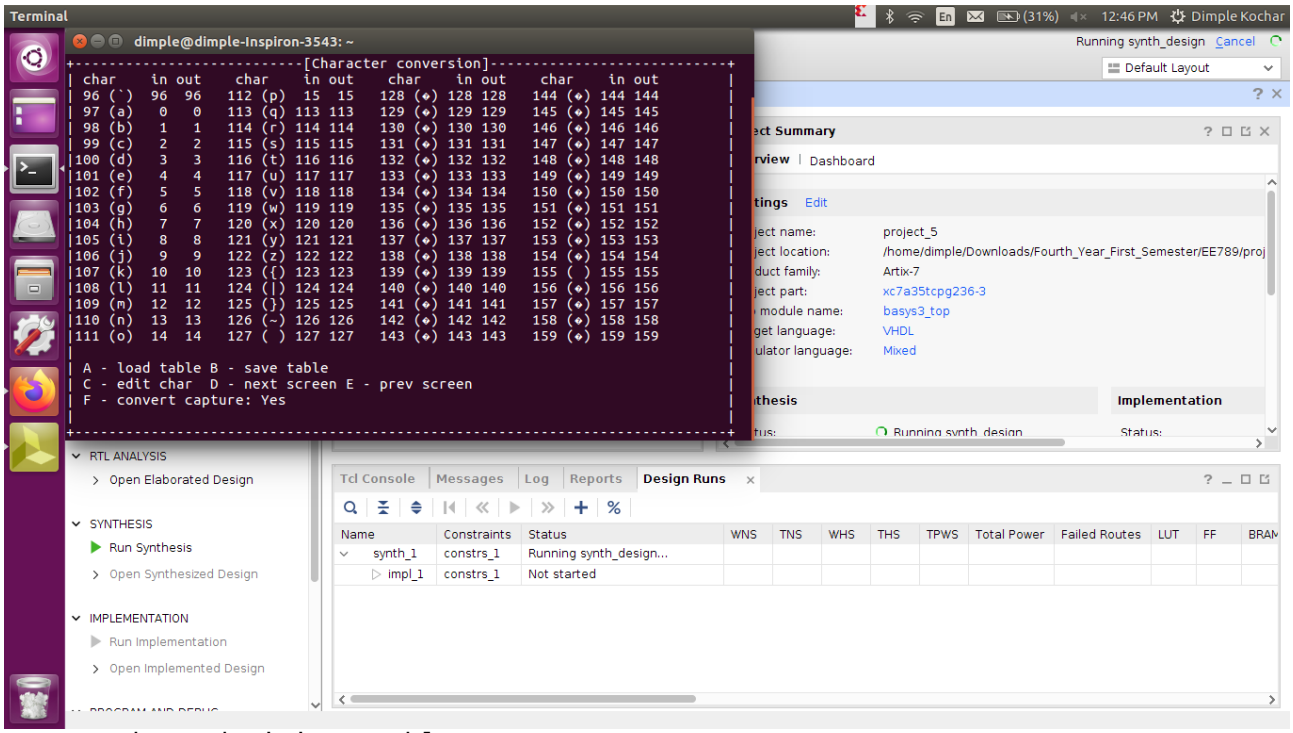


On the testing the processor with various testbenches, all the instructions seemed to work fine.

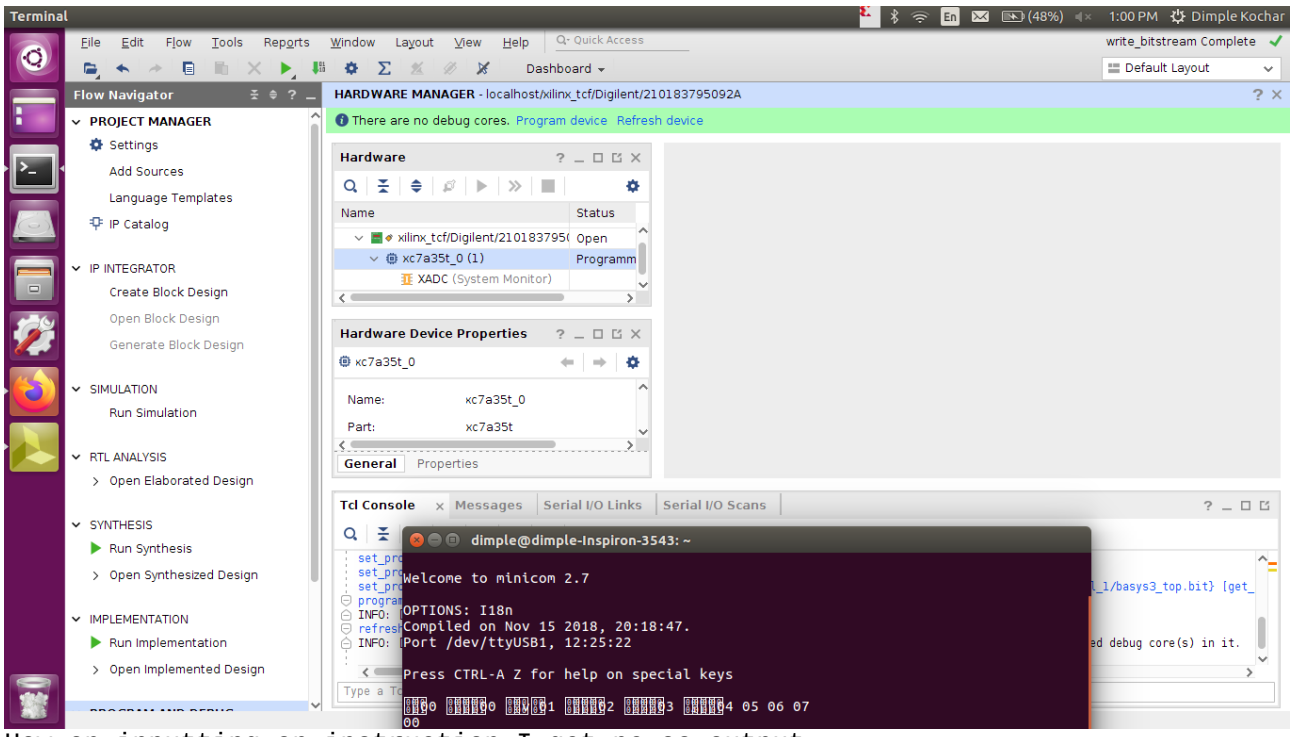
I implemented the uart and the basys3 top module.

On running vivado, I could successfully synthesize, implement and generate bitstream.

Used minicom to communicate with basys board.



How I changed minicom table



How on inputting an instruction I get pc as output

Accelerator: Dimple Kochar-16D070010

Block diagram: