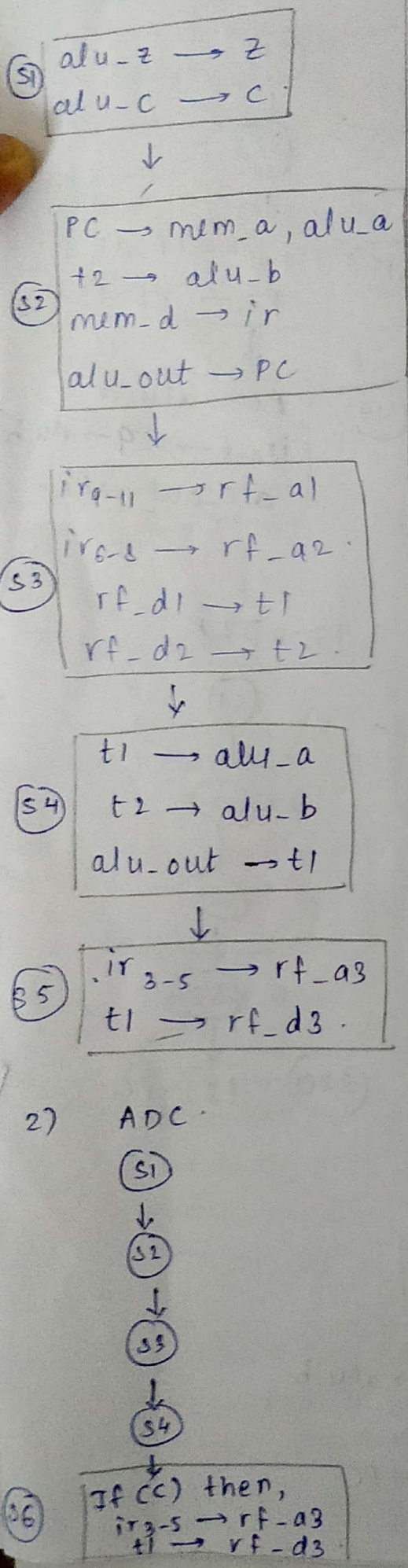
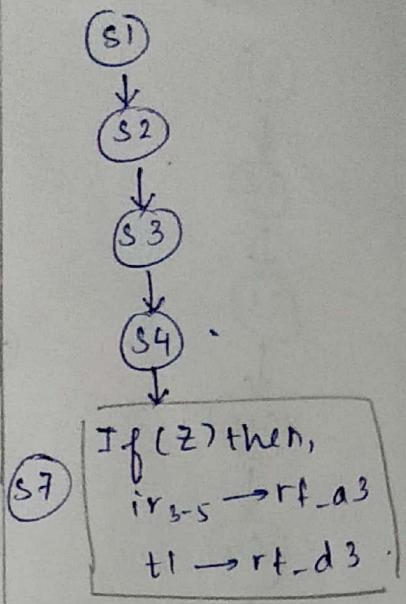
1) ADD.

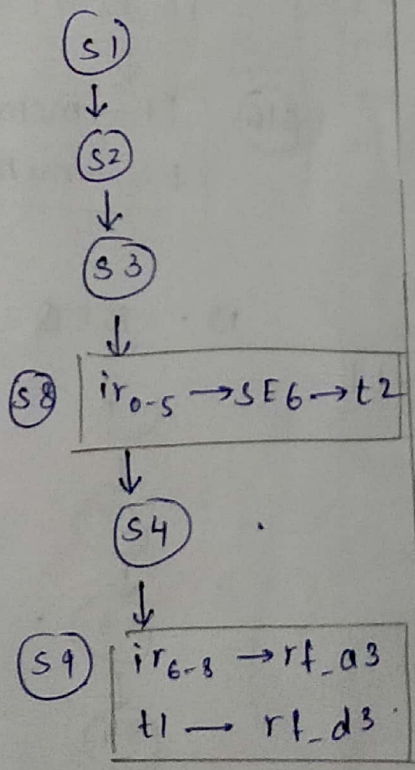


2) ADC.

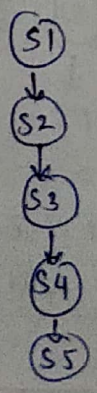
3) ADZ



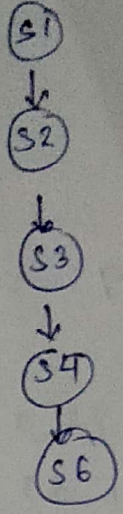
4) ADI



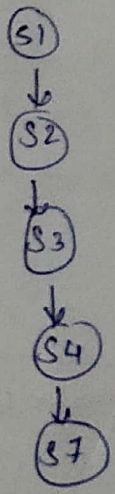
5) NAND.



6) NDC

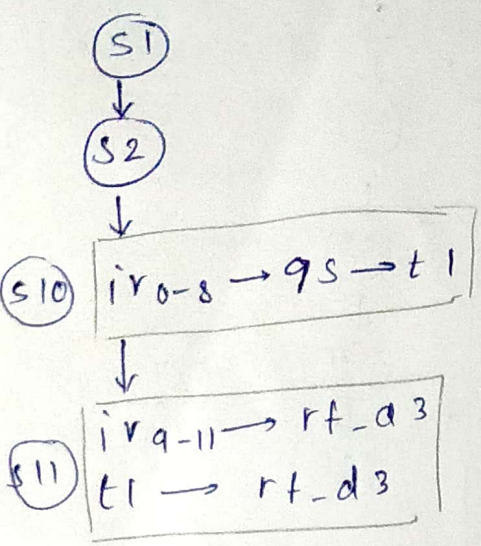


7) NDZ

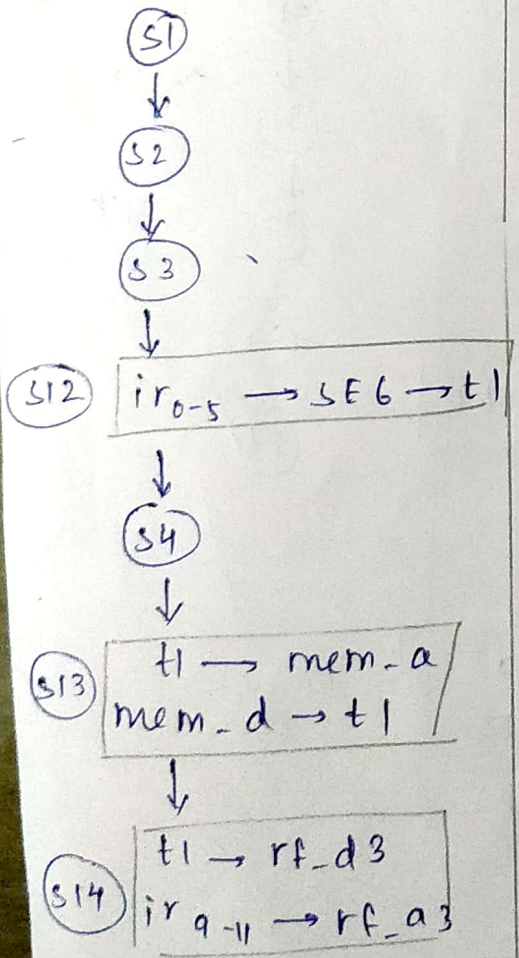


Assumption: for ADC, ADZ, NDC, NDZ: the zero and carry flags of the alu are what have been left by the previous instruction. Those flags are considered.

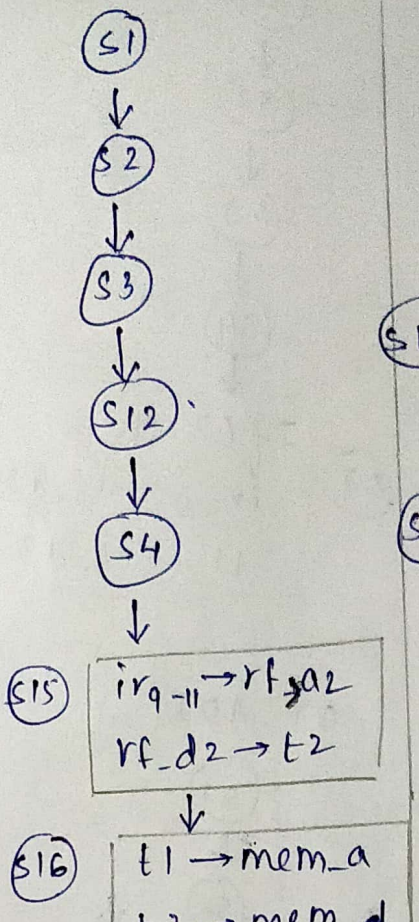
8. LHI



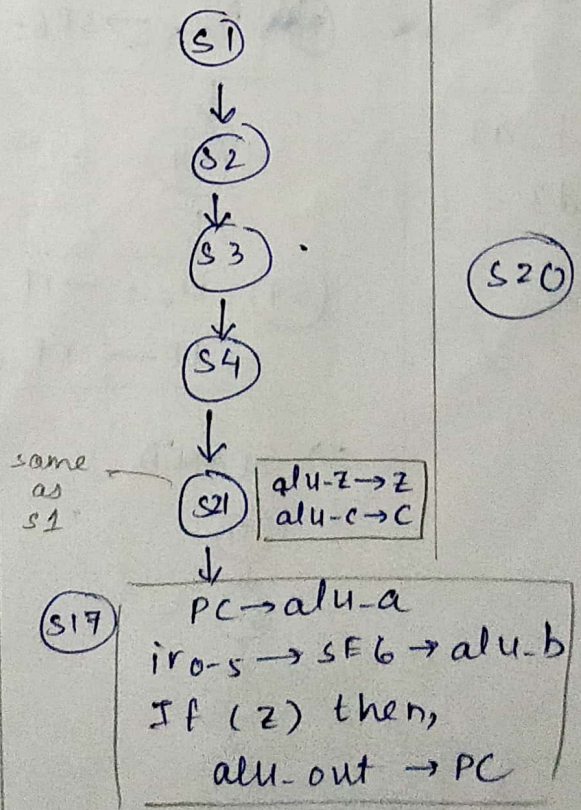
9. LW

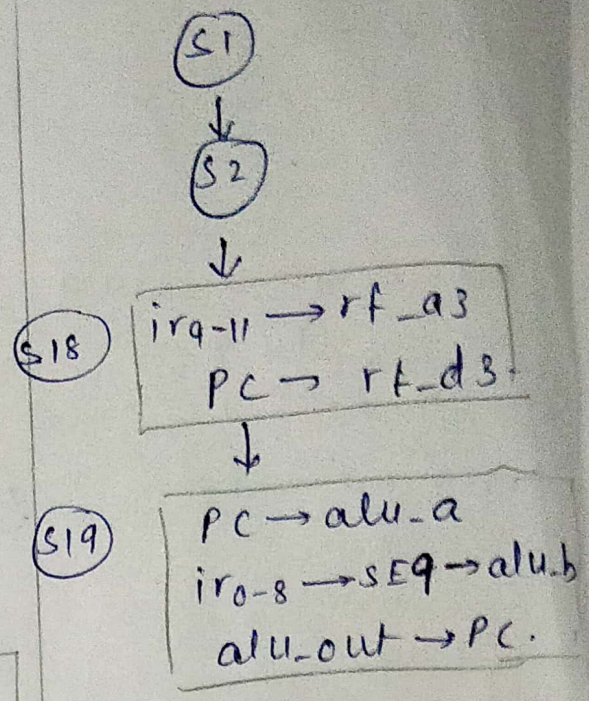


10. SW

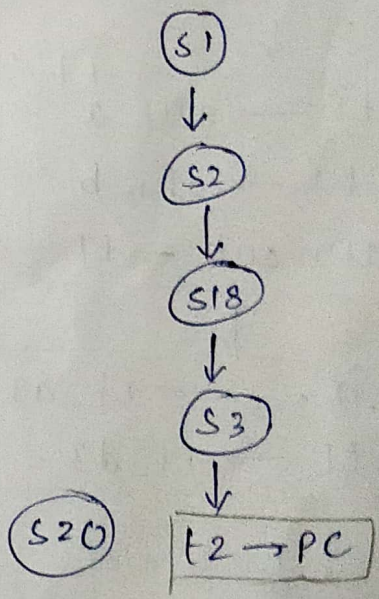


13. BEQ





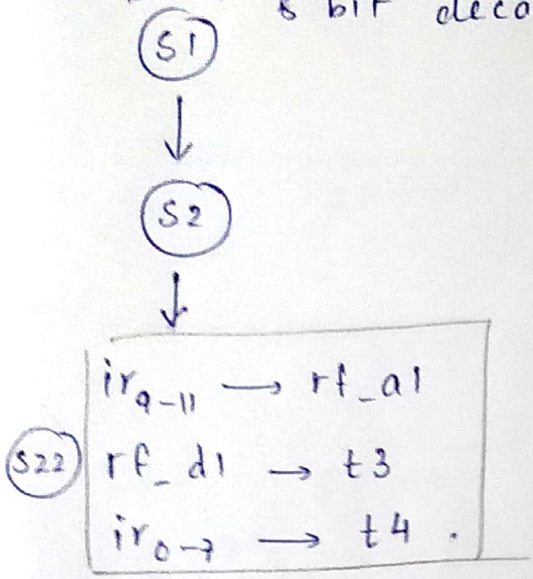
15. JLR



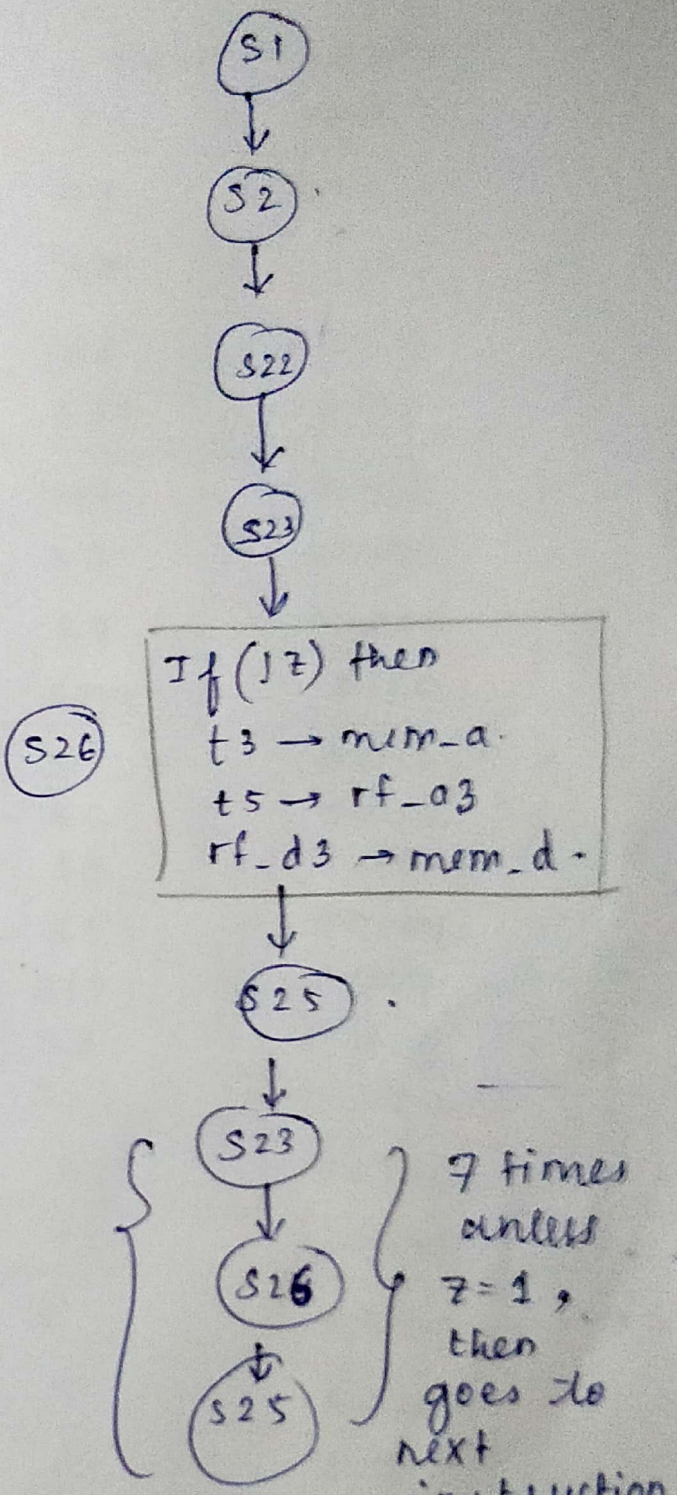
ion

11. LM

(alu1 → 8 bit alu.
t4, t6 → 8 bit registers.
t5 → 3 bit register
t3 → 16 bit register)
PE → 8 bit priority encoder.
D → 8 bit decoder.



12. SM.



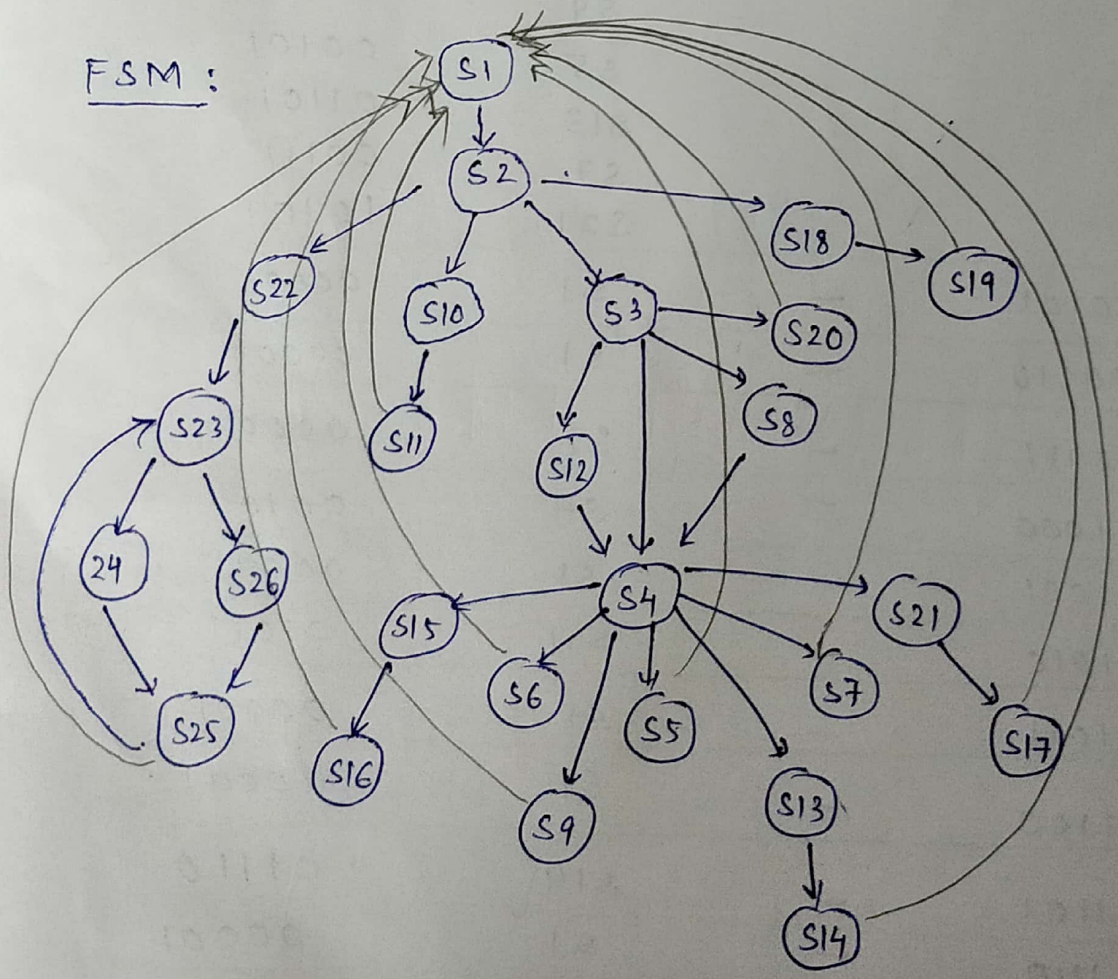
Next state decoder logic

∴ We have 26 states
∴ 5 bits required.

Current state		Decoder	Next state(s)	
S1	00001	—	S2	00010
S2	00010	D1	S3	00011
			S10	01010
			S18	10010
			S22	10110
S3	00011	D2	S12	01100
			S4	00100
			S8	01000
			S20	10100
S4	00100	D3	S15	01111
			S6	00110
			S9	01001
			S5	00101
			S13	01101
			S7	00111
			S21	10101
S5	00101	—	S1	00001
S6	00110	—	S1	00001
S7	00111	—	S1	00001
S8	01000	—	S4	00100
S9	01001	—	S1	00001
S10	01010	—	S11	01011
S11	01011	—	S1	00001
S12	01100	—	S1	00001
S13	01101	—	S14	01110
S14	01110	—	S1	00001
S15	01111	—	S16	10000
S16	10000	—	S1	00001

S17	10001	—	S1	00001
S18	10010	—	S19	10011
S19	10011	—	S1	00001
S20	10100	—	S1	00001
S21	10101	—	S17	10001
S22	10110	—	S23	10111
S23	10111	D[illegible]4	S24	11000
			S26	11010
S24	11000	—	S25	11001
S25	11001	D5	S1	00001
			S23	10110
S26	11010	—	S25	11001

FSM :



Next state decoder logic

D1

Instructions.

(2) 00010 ⟶ 00011 (3) 1, 2, 3, 4, 5, 6, 7, 9, 10, 13

01010 (10) 8

10010 (18) 14, 15

10110 (22) 11, 12.

Next State

ir_{12-15} → 0000, 0001, 0010, 0100, 0101, 1100 → 00011.

→ 0011 → 01010

→ 1000, 1001 → 10010

→ 0110, 0111 → 10110

ir: 15 14 13 12 0

a	b	c	d	

$x = \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}\bar{b}\bar{c}d + \bar{a}\bar{b}c\bar{d} + \bar{a}b\bar{c}\bar{d} + \bar{a}b\bar{c}d + ab\bar{c}\bar{d}$

$y = \bar{a}\bar{b}cd$

$z = a\bar{b}\bar{c}\bar{d} + a\bar{b}\bar{c}d$

$w = \bar{a}bc\bar{d} + \bar{a}bcd.$

Next state =

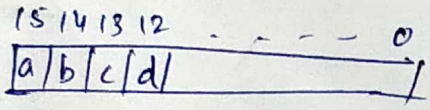
z+w	y	w	1	x

D2

(3) 00011 → 01100 (12) Instructions..
00100 (4) 9, 10
01000 (8) 1, 2, 3, 5, 6, 7, 13
10100 (20) 4
15

ir_{12-15} → 0000, 0010, 1100 → 00100 (4)
→ 0100, 0101 → 01100 (12)
→ 0001 → 01000 (8)
→ 1001 → 10100 (20)

ir



$x = \bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}\bar{b}c\bar{d} + ab\bar{c}\bar{d}$

$y = \bar{a}b\bar{c}\bar{d} + \bar{a}b\bar{c}d$

$z = \bar{a}\bar{b}\bar{c}d$

$w = a\bar{b}\bar{c}d$

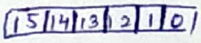
Next state =

w	y+z	x+y+w	0	0

D3

Instructions:

(4) 00100 ⟶ 01111 (15) 10
00110 (6) 2,6
01001 (9) 4
00101 (5) 1,5
01101 (13) 9
00111 (7) 3,7
10101 (21) 13



ir[15-10] ⟶ 010101 ⟶ 01111 (15)

⟶ 001010, 000010 ⟶ 00110 (6)

⟶ 0001xx ⟶ 01001 (9)

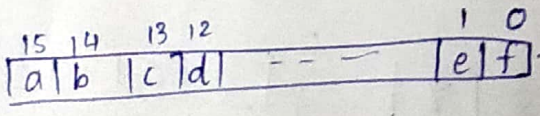
⟶ 000000, 001000 ⟶ 00101 (5)

⟶ 0100xx ⟶ 01101 (13)

⟶ 000001, 001001 ⟶ 00111 (7)

⟶ 1100xx ⟶ 10101 (21)

ir



$x = \bar{a}b\bar{c}d$

$y = \bar{a}\bar{b}cd\bar{e}\bar{f} + \bar{a}\bar{b}\bar{c}d\bar{e}\bar{f}$

$z = \bar{a}\bar{b}\bar{c}d$

$w = \bar{a}\bar{b}\bar{c}d\bar{e}\bar{f} + \bar{a}\bar{b}cd\bar{e}\bar{f}$

$r = \bar{a}b\bar{c}\bar{d}$

$s = \bar{a}\bar{b}\bar{c}d\bar{e}f + \bar{a}\bar{b}cd\bar{e}f$

$t = ab\bar{c}\bar{d}$

Next state

t	x+z+ r	x+y+ w+r+ s+t	x+y + s	x+z+ w+r+ s+t

D4

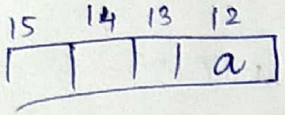
Instructions

(23) 10111 → 11000 (24) 11

11010 (26) 12

ir_{12-15} → 0110 → 11000 (24)

→ 0111 → 11010 (26)

ir. 

Next state = | 1 | 1 | 0 | a | 0 | { | 1 | 1 | 0 | a | 0 | }

D5

(25) 11001 → 00001 (1) ← z=1

10110 (23). ← z=0

z ← {the bit we'd defined which stores, when we want, alu_z}

Next state = | $\bar{z}$ | 0 | $\bar{z}$ | $\bar{z}$ | $\bar{z}$ | { | $\bar{z}$ | 0 | $\bar{z}$ | $\bar{z}$ | z | }

$\bar{z}$ 0 $\bar{z}$ $\bar{z}$ z