EE 620: Physics of Transistors
Assignment 3: Report

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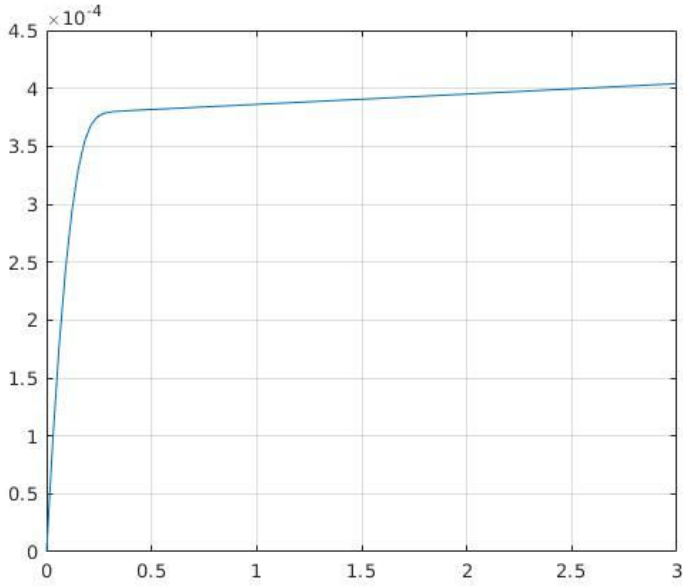
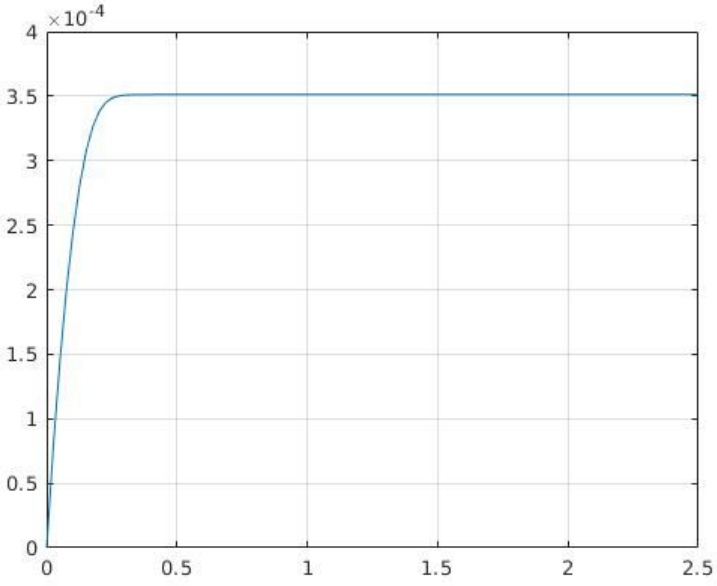
1. Pao Sah model: q1ps.m, Brews model: q1b.m

(Note the integral in pao-sah has been done using Reimann sum, so, it takes a long time to run)



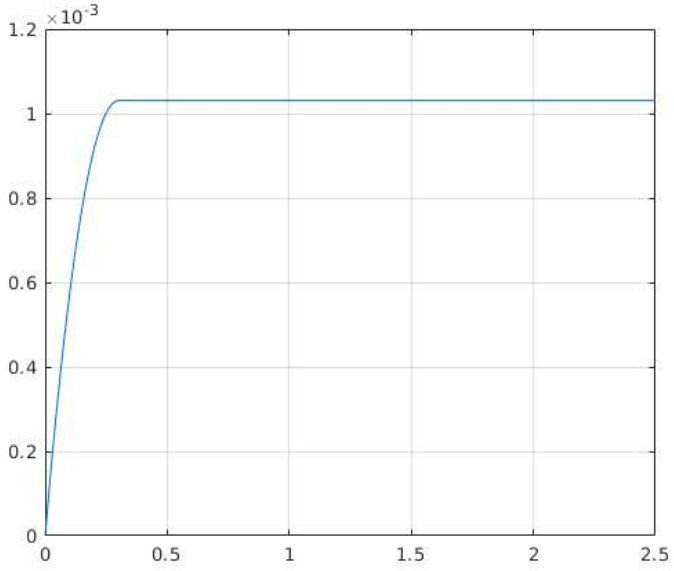
ID vs VDS @ VGS=VTH for Pao Sah



ID vs VDS @ VGS=VTH for Brews

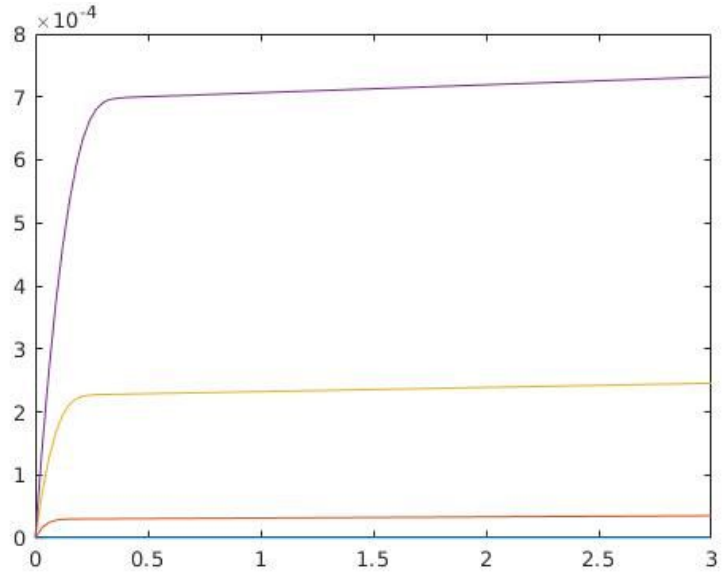
2. Since for piecewise we have two different expressions for ID, one conditioned on VG>VT and other on VG<VT, the given VG=VT+~0.3V in the question there is no expression. This is because piecewise is valid for VG significantly less or more than VT. For VG close to VT we fudge and join the VG vs IDS curve. Therefore, we get mismatched results as compared to Pao-Sah and Brews models.

Considering VG>VT piecewise expression: q2pc1.m



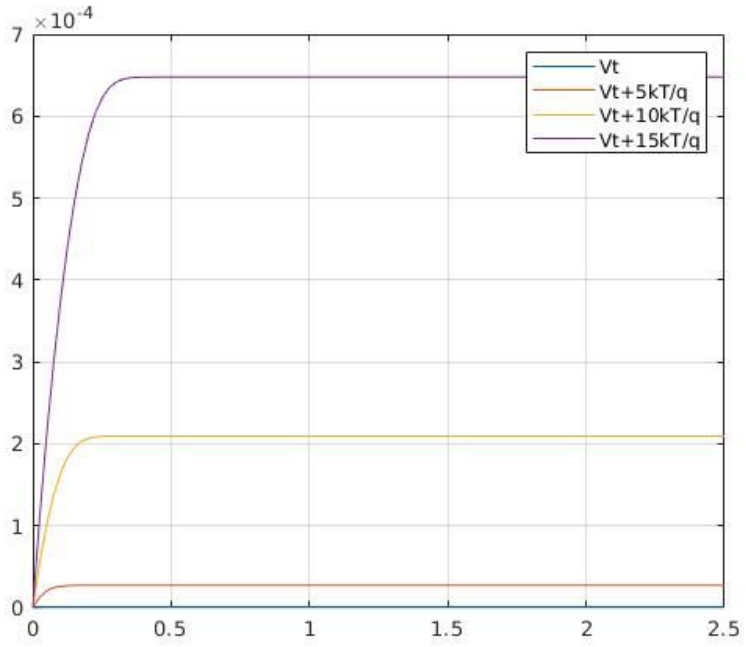
ID vs VDS @ VGS=VTH for Piecewise expression for VG>VT

3. Pao Sah model: q3ps.m, Brews model: q3b.m
(Note the integral in pao-sah has been done using Reimann sum, so, it takes a long time to run)



ID vs VDS @ VGS shown in legend for Pao Sah

Note here, the current has a slight slope, i.e., even after reaching saturation it continues to increase slightly, unlike in Brews. So, the current levels are slightly higher than Brews. For higher Vgs values, this difference is more apparent. Therefore, as Vg increases mismatch increases. Also, Brews shows a constant saturation current, whereas in Pao Sah, the current rightly increases with a small slope as VDS increases.



ID vs VDS @ VGS shown in legend for Brews