EE614 : Course Project

Mohana Madhumita Pokkuluri Dimple Kochar Bhuyashi Deka Sheetal Gupta

Supervisor : Prof. Jayanta Mukherjee With help from : Vinay Narayane

Project objective:

Design a power amplifier using AFIC901N

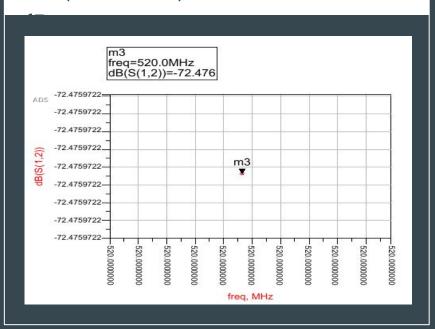
- for a gain of at least 20 dB at 520 MHz
- with appropriate matching networks and bias-tee
- with S11 and S12 values less than -10 dB and -60 dB respectively

Design Steps

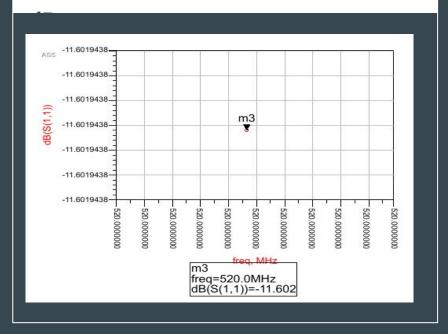
- Check for the stability (K = 17.61 >1 & $|\Delta|$ = 0.244 <1) using s-parameters
- \circ Testing the validation of unilateral assumption from U_{minus} and U_{Plus} values = 0.06
- Obesigning for fixed gain $G_T = G_S + |S_{21}|^2 + G_L = 30 dB$, where $|S_{21}|^2 = 20.15 dB$ and choosing G_S at maximum i.e. $G_S = 6.49$ And $G_L = 3.36$
- Choosing Γ_S close to S_{11}^* on constant G_S circle and Γ_L close to S_{22}^* on constant G_S circle for matching network
- Matching network for the source and load is designed using lumped elements and transmission lines
- Bias tee network (also made of lumped elements) is added to the source and load side
- Finally length of the transmission lines and lumped element parameter are adjusted to get the desired s-parameters.

Matching S constraints

S12 (-72.476 dB) < -60

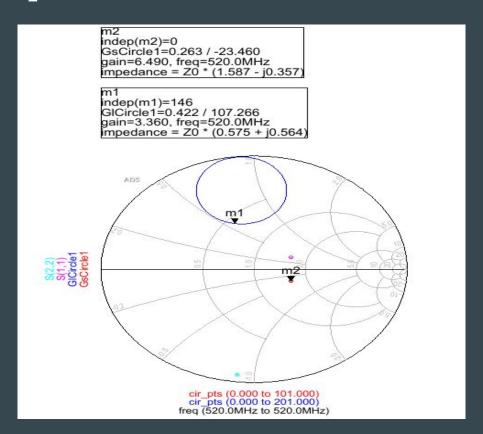


S11 (-11.602 dB) < -10

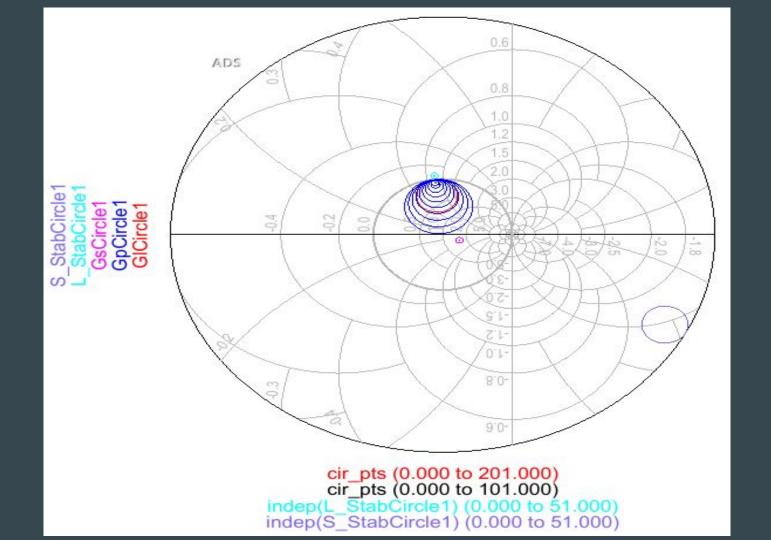


G_s and G₁ Circles

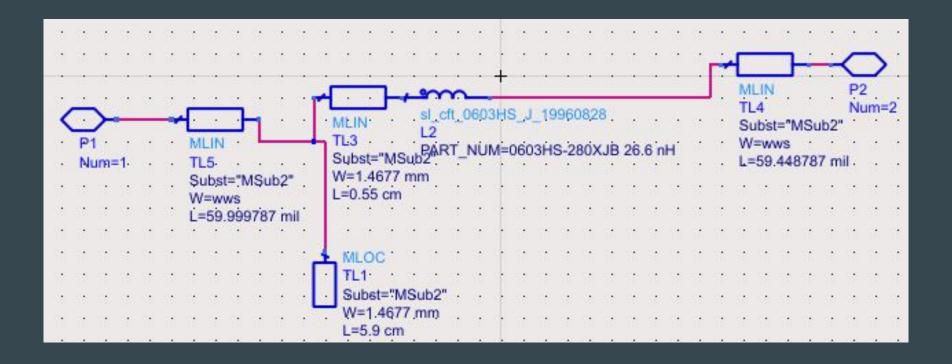
- \circ The value of of Γ_{ς} is chosen close to S₁₁* on the constant G_s circle for source matching
- \circ The value of Γ_1 is chosen close to S₂₂* on constant G₁ circle for load matching
- Total gain $G_T = G_S + |S_{21}|^2$
- $|S_{21}|^2 = 20.15 dB$
- $G_{S}^{2} = G_{S,max} = 6.49 dB$ $G_{L} = 3.36 dB$
- $G_{T} = 30dB$



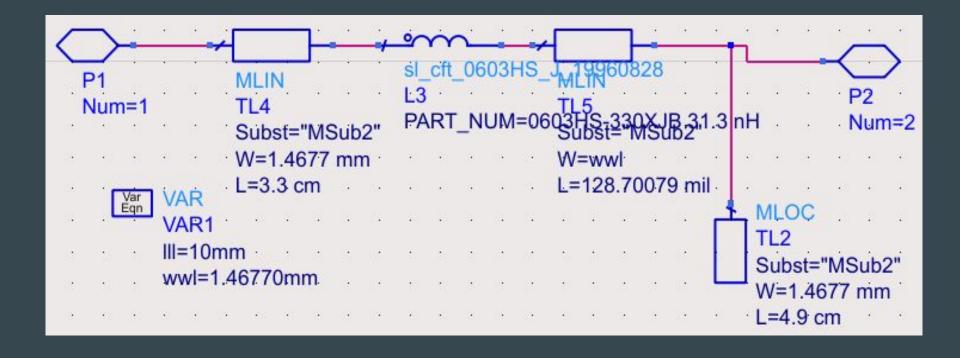
Circles Gain



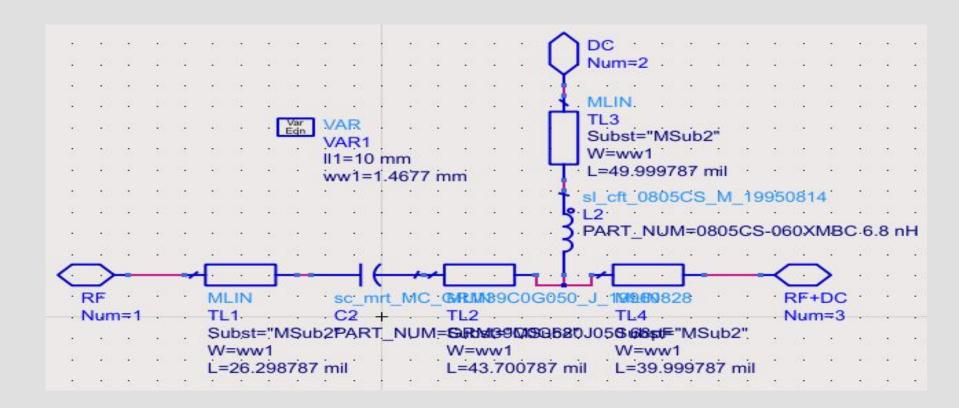
Input Matching Network



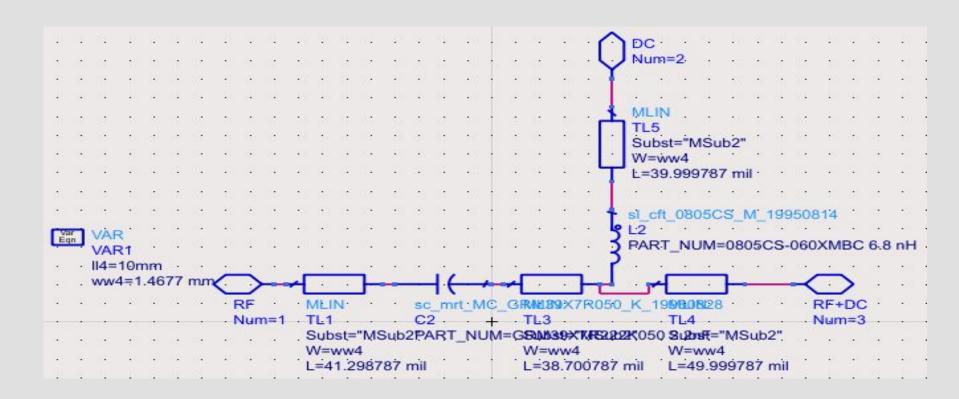
Output Matching Network



Source side bias tee



Load side bias tee

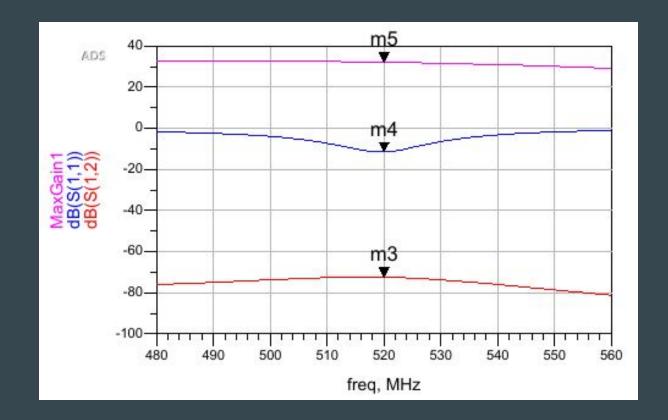


Simulation results

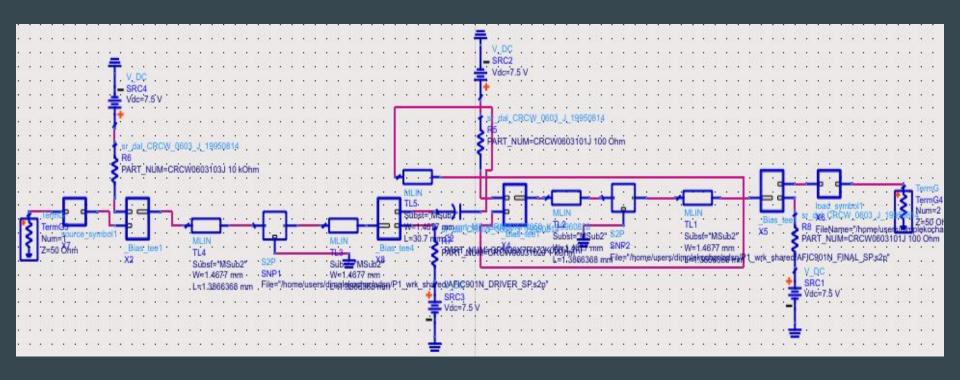
m3 freq=520.0MHz dB(S(1,2))=-72.476

m4 freq=520.0MHz dB(S(1,1))=-11.602

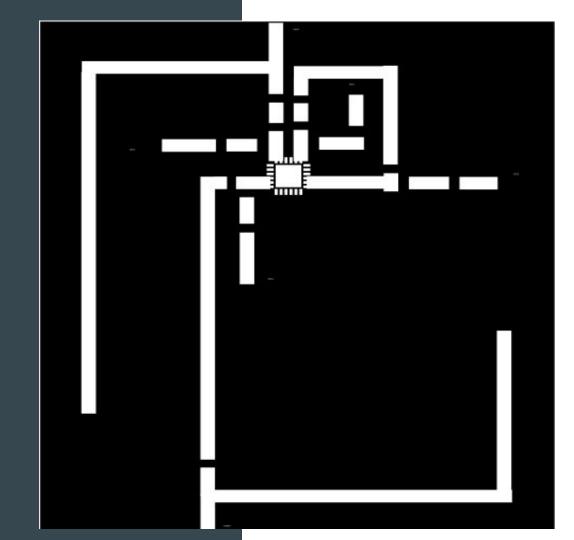
m5 freq=520.0MHz MaxGain1=32.086



Final Schematic

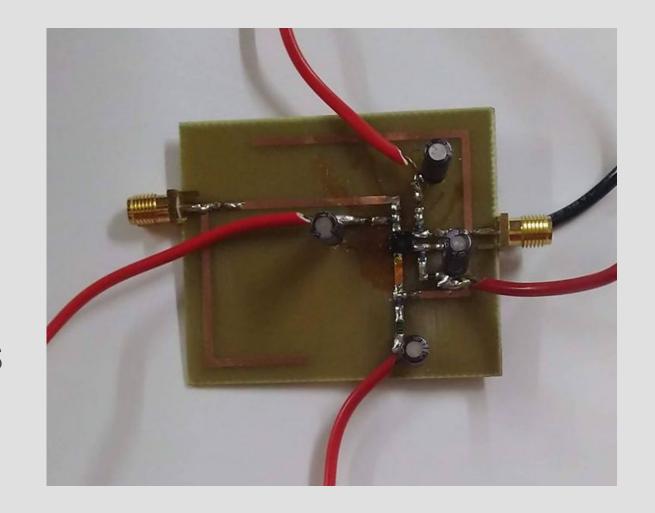


Layout

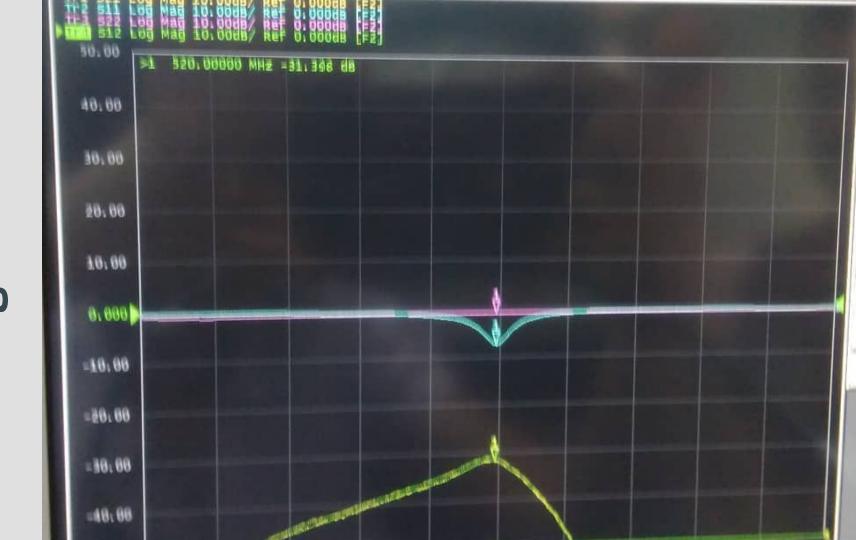


Soldered PCB

with SMD and SMA connectors



Testing results



E5071C Network Analyzer 1 Active Ch/Trace 2 Response 3 Stimulus 4 Mkr/Analysis 5 Instr State Resize Tr1 S21 Log Mag 10.00dB/ Ref 0.000dB [F2] Tr2 S11 Log Mag 10.00dB/ Ref 0.000dB [F2] Tr3 S22 Log Mag 10.00dB/ Ref 0.000dB [F2] Tr4 S12 Log Mag 10.00dB/ Ref 0.000dB [F2] System Print 50.00 >1 520.00000 MHz 2.4935 dB Abort Printing 40.00 Printer Setup... Invert Image 30.00 ON Dump 20.00 Screen Image... Multiport Test Set Setup 10.00 Misc Setup Backlight 0.000 ON Firmware -10.00Revision Service Menu -20.00 Help -30.00 Return -40.00 -50.00 IFBW 70 kHz Stop 1 GHz Cor ! 1 Start 1 MHz Meas | Stop | ExtRef | Svc | 2019-04-17 09:00