Dimple Vijay Kochar

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EDUCATION

Massachusetts Institute of Technology (MIT)
PhD - Electrical Engineering & Computer Science (EECS)
✦ **GPA: 5.00 / 5.00** | Sep 2021 - Jun 2026
Advisors: Anantha P. Chandrakasan, Prof. Hae-Seung Lee
Received the Grass Instrument Company Fellowship 2021-22
Received the MathWorks Engineering Fellowship 2025-26

Indian Institute of Technology Bombay (IITB)
Bachelor & Master of Technology - Electrical Engineering
✦ **GPA: 9.34 / 10.00** | Jul 2016 - Aug 2021
Awarded the **Sharad Maloo Memorial Gold Medal** (1 of 999)
Recipient of the Desai-Sethi Family Scholarship

RESEARCH PROJECTS

LLM-enhanced Analog Circuit Design Optimization
- Proposed using LLMs to reduce the design space for analog circuit sizing, without design annotation or training
- Achieved up to 20% improvement in low-complexity op-amps and 55% in high-complexity op-amps over the best baseline, with a speedup of 1.6x on average across nodes
- Benchmarked 22 amplifier topologies across four FinFET technology nodes, among the first to show generalization

Low Power Speech Enhancement Chip for IoT Devices
- Fabricated in TSMC 28nm CMOS process, chip consumes 407 µW or 3.24 µJ/frame with processing time under 8ms
- Achieved the highest audio quality evaluation score (PESQ) of 2.79 across a -6 to 9 dB SNR range on CHiME2
- Developed a quantized CNN to reduce computational costs; implemented hardware quantization; a complementary dataflow to decrease on-chip memory accesses by 5-9x

Machine Learning for Circuit Performance Prediction
- Created an ML-driven framework for predicting between schematic and layout simulations, multi-corners, and measured silicon data in commercial 14nm node, and migration to 5nm node with <5% MAPE with <30% data to train

Time To Failure Estimation of SRAM due to RTN
- Proposed estimation of TTF distribution of a stored bit under multi-level RTN using a current injection model
- Demonstrated via MC circuit simulations across supply voltages that process variations worsen TTF distribution

HKMG Process Impact on Gate Leakage, SILC & PBTI
- Extracted bulk trap densities from SILC measurements of differently processed NMOS using WKB tunneling model and modeled with a Reaction-Diffusion-Drift framework
- Modelled the time kinetics of traps generated from PBTI stress using the double interface H/H_2 RD framework

RESEARCH INTERESTS

GenAI for chip design and analog circuits, accelerator design, ML for circuit performance prediction

RESEARCH INTERNSHIPS

NVIDIA
PhD Research Intern: ASIC & VLSI
Austin, TX, USA | Jun 2025 - Aug 2025

Qualcomm
Making In-Memory Computing Reliable
San Diego, CA, USA | Jun 2023 - Aug 2023
- Filed a patent application for a circuit technique for an accurate and robust against process variations IMC
- Secondarily, developed a ref. circuit + ML model with 96.4% bit accuracy for IMC in TSMC N3E 8T SRAM

Kavli Institute of Nanoscience, TU Delft
Dipole-Exchange Spin Waves in Ferromagnetic Films
Delft, Netherlands | May 2019 - Jun 2019
- Calculated the wave function, magnetization and dipolar field profiles for various spin wave modes; got dispersion relation and chirality variation with thickness

SELECTED PUBLICATIONS

- S. Kim, C. Jung, **D. Kochar**, "Compute-in-Memory with Current Transition Detection," U.S. App. No. 18/403,010, 2024. ***Qualcomm***
- **D. Kochar** et *al.*, "LEDRO: LLM-Enhanced Design Space Reduction and Optimization for Analog Circuits,", *IEEE International Conference on LLM-Aided Design (ICLAD) 2025*, WIP poster at *Design Automation Conference (DAC), 2025* ***MIT***
- **D. Kochar** et *al.*, "Efficient Circuit Performance Prediction Using Machine Learning: From Schematic to Layout and Silicon Measurement with Minimal Data Input," *Int. Symposium on Circuits and Systems 2025.*, **awarded best track manuscript**, under review at *IEEE TCAS-I* ***MIT, MIT-IBM Watson AI Lab***
- **D. Kochar** et *al.*, "A 0.75mm^2 407μW real-time speech audio denoiser with quantized cascaded redundant convolutional encoder-decoder for wearable IoT devices," *Int. Conference on VLSI Design 2025.* ***MIT***
- **D. Kochar** et *al.*, "Estimation of Time to Failure Distribution in SRAM Due to Trapped Oxide Charges," *IEEE Int. Symp. on Circuits and Systems* 2021. ***IITB***
- **D. Kochar** et *al.*, "Modeling of HKMG Stack Process Impact on Gate Leakage, SILC and PBTI," *IEEE International Reliability Physics Symposium (IRPS)* 2021. ***IITB***