Dimple Kochar

CONTACT INFORMATION

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EDUCATION

Massachusetts Institute of Technology — *September, 2021 – Present*

PhD student, Department of Electrical Engineering & Computer Science
Advisor: Prof. Anantha Chandrakasan — MIT Energy-Efficient Circuits and Systems
GPA: 5.0 / 5.0

Indian Institute of Technology Bombay — *July, 2016 – August, 2021*

Bachelor & Master of Technology, Department of Electrical Engineering
Specialization: Microelectronics & VLSI
Minor Degree, Department of Computer Science & Engineering
GPA: 9.34 / 10.0
Awarded the *'Sharad Maloo Memorial Gold Medal'* for being the most outstanding student in terms of extra-curricular activities along with academic performance, among all recipients of B.Tech/DD (B.Tech+M.Tech) degree (1 in 999) at the 59th Convocation of IIT Bombay

PUBLICATIONS

- **D. Kochar**, T. Samadder, S. Mukhopadhyay and S. Mahapatra, "Modeling of HKMG Stack Process Impact on Gate Leakage, SILC and PBTI," *2021 IEEE International Reliability Physics Symposium (IRPS)*, 2021, pp. 1-7, doi: 10.1109/IRPS46558.2021.9405154. [paper]
- **D. Kochar** and A. Kumar, "Estimation of Time to Failure Distribution in SRAM Due to Trapped Oxide Charges," *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2021, pp. 1-5, doi: 10.1109/ISCAS51556.2021.9401180. [paper]
- T. Samadder, N. Choudhury, S. Kumar, **D. Kochar**, N. Parihar and S. Mahapatra, "A Physical Model for Bulk Gate Insulator Trap Generation During Bias-Temperature Stress in Differently Processed p-Channel FETs," in *IEEE Transactions on Electron Devices*, vol. 68, no. 2, pp. 485-490, Feb. 2021, doi: 10.1109/TED.2020.3045960. [paper]
- S. Kumar*, T. Samadder*, **D. Kochar**, and S. Mahapatra, "A Stochastic Simulation Framework for TDDB in MOS Gate Insulator Stacks" presented in *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2022

RESEARCH PROJECTS

Generative AI for Analog and Mixed-Signal Circuit Migration — *MIT*
Advisor: Prof. Anantha Chandrakasan, EECS Department — *Jan '24 - Present*

Introduction: The technology scaling improves the overall performances of digital circuits reducing the power delay product. However, it does not lead to the same benefits when applied to analog circuits. Additional design variables, such as transistor lengths, bias currents, or requirements, such as voltage gain, unit gain frequency, signal to noise ratio (SNR) and so on, turn this into a challenging issue. While scaling analog circuits, their overall behavior is often modified and their performances altered. This project aims to automate this process using large language models (LLMs).

- Work in progress, please contact directly for further elaboration and details

Low Power, Low Memory, CNN Accelerator for Audio Denoising — *MIT*
Advisor: Prof. Anantha Chandrakasan, EECS Department — *Nov '22 - Present*

Introduction: The growth in low-power, small area, embedded devices and advancement in the optimization of ML algorithms has resulted in tiny machine learning (TinyML). Given an input noisy signal, we aim to filter out the undesired noise without degrading the signal of interest. This is done by running a CNN on-chip with low memory & power, in real time.

- Chip taped out, work in progress, please contact directly for further elaboration

HKMG Stack Process Impact on Gate Leakage, SILC & PBTI [slides] — *IIT Bombay*
Advisor: Prof. Souvik Mahapatra, Electrical Engineering Department — *Dec '18 - Oct '20*

Introduction: The primary impediment to channel length scaling is gate leakage. PBTI and SILC also get worse at scaled EOT. Recently, RD and RDD models are used for NBTI interface and bulk trap generation in PMOS. This project aims to model direct tunneling leakage, SILC & PBTI along with the traps generated in NMOS withdeeply scaled (down to EOT∼7Å) HKMG stacks.

- Quantified impact of IL & HK thickness, channel/IL & IL/HK barriers on gate leakage & SILC
- Extracted bulk trap densities from SILC measurements of differently processed NMOS using a WKB tunneling model & used a Reaction-Diffusion-Drift (RDD) framework to model them
- Modelled the traps generated from PBTI stress using the double interface H/H_2 RD framework
- Analysed impact of gate stack process (pre-clean, IL, IL/HK interface, HK & post-HK nitridation) on gate leakage, SILC and PBTI trap generation (using DCIV) at IL/HK interface

Method for Time To Failure Estimation of SRAM due to RTN [slides] *IIT Bombay*
Advisor: Prof. Animesh Kumar, Electrical Engineering Department *Dec '18 - Nov '20*
Introduction: Trapping and detrapping of charges in the oxide interface of a MOSFET leads to a random telegraphic noise (RTN) injection & this phenomenon negatively affects the reliability of circuits. The objective of this project is to develop a reproducible strategy to obtain time to failure (TTF) distribution & related statistics for SRAM of any technology with any given RTN model.

- Proposed a method to estimate TTF distribution of a stored bit in an SRAM cell due to single or multi-level RTN by composition of Monte-Carlo simulations & circuit-level abstraction
- Showcased results of this procedure on an SRAM cell made from 45 nm technology with a single-trap RTN model at various supply voltages using Cadence, Ocean and Python scripting
- Indicated via circuit-level simulations that the TTF distribution worsens due to process variations

Model for Time Dependent Dielectric Breakdown for Thin Oxides [slides] *IIT Bombay*
Advisor: Prof. Souvik Mahapatra, Electrical Engineering Department *May '18 - Jun '21*
Introduction: Time-dependent dielectric breakdown (TDDB) is characterized by its Weibull slope. In this project, the change in the slope is explained by a percolation model with different defect generation rates in the bulk & channel/oxide and gate/oxide interfaces, also considering SILC slope changes with thickness & trap size. The model is then extended for high-k with interfacial SiO_2.

- Designed a cell based oxide percolation model which stochastically creates bulk & interface traps
- Procured time to failure distribution & analysed the relation of its Weibull slope with oxide thickness & obtained results obeying experimental data varying with voltage & temperature
- Proposed and demonstrated a hypothesis for differences in bulk trap & SILC slopes

Research Internships

Making In-Memory Computing Reliable *Qualcomm*
Memory IP Team, San Diego *Jun '23 - Aug '23*
Introduction: A major percentage of today's deep learning architecture are the MAC operations. If the weights are stored in the foundry 8-T bit-cell, and the RWL has the input coming in, current proportional to the compute output passes through the RBL. Due to process variations, this current varies in a large range. Foundry bit-cell is essential to use SRAM design rules and ensure scalability. To solve this problem, two approaches were implemented in TSMC N3E technology node.

- Further elaboration is not possible at this stage due to patent application filed on 01-03-2024, titled "Compute-in-Memory with Current Transition Detection", U.S. App. No. 18/403,010

Dipole-Exchange Spin Waves in Thin Ferromagnetic Films [slides] *TU Delft*
Advisors: Prof. Gerrit Bauer, Kavli Institute of Nanoscience *May '19 - Jul '19*
Prof. Yaroslav Blanter, Kavli Institute of Nanoscience
Introduction: Dispersion characteristics of spin waves in ferromagnetic films taking into account both the dipole-dipole and the exchange interactions are obtained by a sixth-order differential equation. The objective of this project is to solve it considering pinned and unpinned boundary conditions & study their variation with thickness in this transition region.

- Calculated the wave function, magnetization & dipolar field profiles for various modes of spin waves by solving Landau–Lifshitz & Maxwells' equations & appropriate boundary conditions
- Showed how chirality changes with thickness; obtained the dispersion relation (ω vs $\vec{k}$) for a film
- Obtained isofrequency curves & showed their change with increase in magnetic field in $\vec{k}$ space

Scholastic Achievements

- Conferred the 'Grass Instrument Company Fellowship' to support first year at MIT
- Bestowed the 'Desai-Sethi Scholarship' awarded to the top 5 girls admitted to IIT Bombay
- Achieved All India Rank 102 in JEE Main and All India Rank 295 in JEE Advanced out of 1.2 & 0.2 million candidates respectively; stood first in both in the state of Maharashtra among girls

- Awarded the 'Travel Grants for UG students by C'1992 and C'1998' for IEEE ISCAS 2021
- Selected for Indian National Chemistry Olympiad (InChO) from among 40K students

Technical Projects

Ring Oscillator Characterization *MIT-IBM AI Watson Lab*

- Taped out in 14nm Samsung technology, designed for accurate power & frequency measurements

Low Power FC-CS CMOS Operational Amplifier *Analog Circuits*

- Designed an FC-CS CMOS opamp in 22nm bsim4 with power < 1.5mW, settling times < 8ns, open loop gain > 10k, thermal noise < 300uV, phase margin $> 65^o$ at gain-of-2 frequency

Power Amplifier Design for function at 520 MHz *Solid State Microwave Devices*

- Constructed matching networks using microstrip transmission lines and fabricated it on FR4 substrate to obtain a gain of 2.5 dB at 520 MHz with S_{11} and S_{12} values -18 dB and -35 dB

Sub-100nm Gate GaN HEMT transistor fabrication *Device Fabrication*

- Fabricated a HEMT on GaN-on-Si with an $I_{ON} = 1.3$A/mm and $R_{ON} = 1.54\Omega$ at MIT.nano

Broadband 4 × 4 Butler Matrix Circuit at 5.4GHz *Microwave Integrated Circuits*

- Constructed 90° hybrids & phase delay lines using microstrip transmission lines to equally divide power, fabricated on FR4 substrate & achieved equal power division and input port isolation

Other projects:

- Implemented IITB-RISC on DE0-Nano FPGA, an 8-register, 16-bit system with 15 instructions in standard 6 stage pipelines & equipped it with control flow, data forwarding & hazard mitigation
- Awarded the best among 70+ projects for implementing an audio volume controller, motion tracker & a pattern lock by gesture detection using infrared emitters & sensors and CPLD
- Stood in the top 5 teams in the Make in India presentation organised for TEQIP-III for heart rate variability analysis by processing the ECG signal & PSD to predict risk of myocardial infarction

Relevant Courses

MIT: CMOS Analog and Circuit Design; Analysis and Design: Digital Circuit; TinyML and Efficient Deep Learning Computing; Machine Learning; Computer System Architecture; Hardware Architecture for Deep Learning; Applied Quantum and Statistical Physics

IITB: Foundation of VLSI CAD; VLSI Design; Algorithmic Design of Digital Systems; Microprocessors; Microwave Integrated Circuits; Solid State Microwave Devices & their Applications; Physics of Transistors; VLSI Technology

Teaching & Mentoring Experience

Teaching Assistant for MIT Course

6.6000 (6.775): CMOS Analog and Circuit Design, *Spring '24*

Teaching Assistant for IIT Bombay Courses

EE302: Control Systems, *Spring '21*
EE325: Probability & Random Processes, *Fall '20*
MA108: Differential Equations, *Spring '18*
PH107: Quantum Mechanics, *Fall '17*

Mentor, Graduate Application Assistance Program, EECS, MIT *2023*
Mentor, Department Academic Mentorship Program, IIT Bombay *2019-2021*

Leadership in Journalism

Recipient of the **Institute Journalism Special Mention Award** at IIT Bombay

Editor, Insight, IIT Bombay *Apr '18 - Mar '19*
Official Print Media Body | Circulated to 10K+ students & 650+ faculty | Online readership 0.4M+
Convenor, IIT Bombay Broadcasting Channel *Apr '17 - Mar '18*
Official Multimedia Journalism Body | 50K+ YouTube Subscribers | 25K+ Facebook Followers

References

Prof. Anantha Chandrakasan, EECS
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Seohee Kim, Senior Staff Engineer
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