Dimple Vijay Kochar

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RESEARCH INTERESTS

GenAI for chip design, verification and analog circuits; accelerator design; ML for performance prediction

EDUCATION

Massachusetts Institute of Technology (MIT), Cambridge, USA　　　　*Sep '21 - Jun '26*
Doctor of Philosophy (Ph.D.) in Electrical Engineering & Computer Science　　　　GPA: 5.0/5.0
Advisors: Prof. Anantha Chandrakasan and Prof. Hae-Seung Lee

Indian Institute of Technology Bombay (IITB), Mumbai, India　　　　*Jul '16 - Aug '21*
Bachelor of Technology (B.Tech.) in Electrical Engineering with Minor in Computer Science　　GPA: 9.34/10.0
Master of Technology (M.Tech.) in Electrical Engineering specialized in Microelectronics & VLSI
Advisor: Prof. Souvik Mahapatra

RESEARCH INTERNSHIPS　　　　　　　　　　　　　　(linked to publication list on next page)

NVIDIA Research | Improving LLM-based Hardware Test Plan Generation　　　*[P9]*
ASIC & VLSI Research Group, Dr. Brucek Khailany and Dr. Nathaniel Pinckney　　Summer '25, Austin, USA
• Proposed novel GRPO-SMu reinforcement learning algorithm; and a new RTL bug injection strategy
• 7B model outperforms general models (Claude-4.0-Sonnet, etc) in test generation & bug detection

Qualcomm | Making In-Memory Computing Reliable　　　*[A1]*
Memory IP Group, Chulmin Jung and Dr. Seohee Kim　　Summer '23, San Diego, USA
• Worked on circuit technique for robust against process variations IMC design with foundry 8T bit-cell

TU Delft | Dipole-Exchange Spin Waves in Ferromagnetic Films
Kavli Institute of Science, Prof. Gerrit Bauer and Prof. Yaroslav Blanter　　Summer '19, Delft, NL

ACADEMIC RESEARCH　　　　　　　　　　　　　　(linked to publication list on next page)

Automating SAR ADC Design and Generation　　　*[Ongoing]*
• Current work towards AI-driven architecture and functional verification framework for SAR ADC

LLM-enhanced Analog Circuit Design Optimization [Best Paper Candidate]　　*[P7, A2]*
• Proposed to use LLM to reduce the design space for analog circuit sizing, without annotation or training
• Achieved average ∼55% improvement for more complex op-amps, with a speedup of $1.6\times$ across nodes

Low Power Speech Enhancement Chip for IoT Devices　　　*[P5]*
• Taped out in TSMC 28nm CMOS, chip consumes 407 µW or 3.24 µJ/frame with processing time <8ms
• Achieved the highest audio quality evaluation score (PESQ) of 2.79 across a -6 to 9 dB SNR on CHiME2

Machine Learning for Circuit Performance Prediction [Best Track Manuscript]　　*[P8, P6]*
• Created an ML-driven framework for predicting between schematic, layout, and measured silicon data
 (small circuits taped out in 14nm), and migration to 5nm with <5% MAPE with <30% data to train

Time To Failure Estimation of SRAM due to RTN　　　*[P3]*
• Estimated the TTF distribution of a stored bit under multi-level RTN using a current injection model
• Demonstrated via MC circuit simulations across supply voltages that process variations worsen TTF

HKMG Process Impact on Gate Leakage, SILC & PBTI　　　*[P2, P1]*
• Extracted bulk trap densities from SILC measurements of differently processed NMOS using WKB
 tunneling model, and modeled with a Reaction-Diffusion-Drift (RDD) framework; modelled the time
 kinetics of traps generated from PBTI stress using the double interface H/H_2 RD framework

LIST OF PUBLICATIONS

[P9] **Dimple Vijay Kochar**, Nathaniel Pinckney, Guan-Ting Liu, Chia-Tung Ho, Chenhui Deng, Haoxing Ren, Brucek Khailany. **GRPO with State Mutations: Improving LLM-Based Hardware Test Plan Generation**. Accepted at *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2026.   *NVIDIA*

[P8] **Dimple Vijay Kochar**, Maitreyi Ashok, John Cohn, Xin Zhang, and Anantha P. Chandrakasan. **Efficient circuit performance prediction using machine learning: From schematic to layout and silicon measurement with minimal data input.** In *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2025, doi: 10.1109/TCSI.2025.3591557.   *MIT, MIT-IBM AI Watson Lab*

[P7] **Dimple Vijay Kochar**, Hanrui Wang, Anantha P. Chandrakasan, and Xin Zhang. **Ledro: Llm-enhanced design space reduction and optimization for analog circuits**. In *IEEE International Conference on LLM-Aided Design (ICLAD)*, 2025, doi: 10.1109/ICLAD65226.2025.00011. [Best Paper Candidate]   *MIT*

[P6] **Dimple Vijay Kochar**, Maitreyi Ashok, John Cohn, Anantha P. Chandrakasan, and Xin Zhang. **Efficient circuit performance prediction using machine learning: From schematic to layout and silicon measurement with minimal data input.** In *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2025, doi: 10.1109/ISCAS56072.2025.11044054. [Best Track Manuscript]   *MIT, MIT-IBM AI Watson Lab*

[P5] **Dimple Vijay Kochar**, Maitreyi Ashok, and Anantha P. Chandrakasan. **A 0.75 mm 2 407μW Real-Time Speech Audio Denoiser with Quantized Cascaded Redundant Convolutional Encoder-Decoder for Wearable IoT Devices**. In *2025 38th International Conference on VLSI Design and 2024 23rd International Conference on Embedded Systems (VLSID)*, 2025, doi: 10.1109/VLSID64188.2025.00044.   *MIT*

[P4] Satyam Kumar*, Tarun Samadder*, **Dimple Kochar**, and Souvik Mahapatra. **A Stochastic Simulation Framework for TDDB in MOS Gate Insulator Stacks**. In *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2022.   *IIT Bombay*

[P3] **Dimple Kochar**, and Animesh Kumar. **Estimation of Time to Failure Distribution in SRAM Due to Trapped Oxide Charges**. In *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2021, doi: 10.1109/ISCAS51556.2021.9401180.   *IIT Bombay*

[P2] **Dimple Kochar**, Tarun Samadder, Subhadeep Mukhopadhyay, and Souvik Mahapatra. **Modeling of HKMG Stack Process Impact on Gate Leakage, SILC and PBTI**. In *IEEE International Reliability Physics Symposium (IRPS)*, 2021, doi: 10.1109/IRPS46558.2021.9405154.   *IIT Bombay*

[P1] Tarun Samadder, Nilotpal Choudhury, Satyam Kumar, **Dimple Kochar**, Narendra Parihar, and Souvik Mahapatra. **A physical model for bulk gate insulator trap generation during bias-temperature stress in differently processed p-channel FETs**. In *IEEE Transactions on Electron Devices*, 2021, doi: 10.1109/TED.2020.3045960.   *IIT Bombay*

PATENT APPLICATIONS

[A2] **Dimple Kochar**, Xin Zhang, Anantha Chandrakasan, **Design Space Reduction and Optimization for Analog Circuits**, U.S. App. No. 19/247,091, 2025.   *MIT, IBM*

[A1] Seohee Kim, Chulmin Jung, **Dimple Kochar**, **Compute-in-Memory with Current Transition Detection**, U.S. App. No. 18/403,010, 2024.   *Qualcomm*

SCHOLASTIC ACHIEVEMENTS AND AWARDS

- Received the MathWorks Engineering Fellowship 2025-26, and the Grass Instrument Company Fellowship 2021-22
- Awarded the **'Sharad Maloo Memorial Gold Medal'** for being the second-most outstanding student among all B.Tech/Dual Degree graduating students (1 in 999) at the 59th Convocation of IIT Bombay
- Received the Desai-Sethi Family Scholarship 2016-20 for being among the top 5 women admitted to IIT Bombay

TEACHING SERVICES

Teaching Assistant, Massachusetts Institute of Technology (MIT)   *2024*
- CMOS Analog and Circuit Design (6.6000 / 6.775)

Teaching Assistant, Indian Institute of Technology Bombay (IITB)   *2016-2021*
- Control Systems (EE 302)
- Probability and Random Processes (EE 325)
- Differential Equations (MA 108)
- Quantum Mechanics and Applications (PH 107)