

Lecture 5 (Chapter 2)

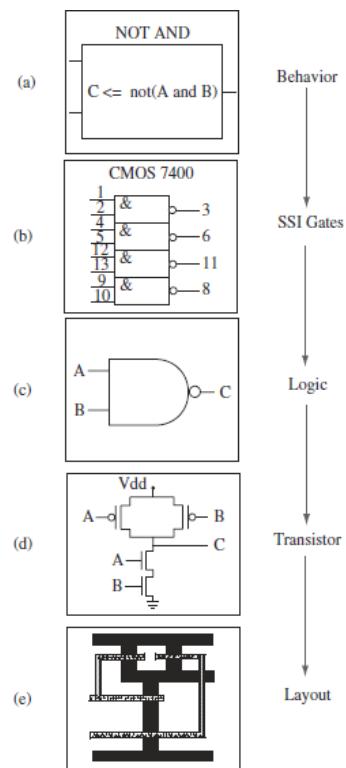
Introduction to VHDL

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ECE 4250/7250

Behavioral and Structural VHDL

- Any circuit or device can be represented in multiple forms of abstraction.
- Example:

FIGURE 2-50: Different Levels of Abstraction of a NAND Device



Behavioral and Structural VHDL (continued)

- 3 Models:

- **Behavioral:**

- Specifies only the behavior at a higher level of abstraction.
 - Does not imply any particular structure or technology.

- **Structural:**

- Specifies more details.
 - Components used and the structure of the interconnection between the components are clearly specified.
 - At a low level of abstraction.

- **Dataflow (Register Transfer Language [RTL]):**

- Data path and control signals are specified.
 - System is described in terms of the data transfer between registers.
 - At an intermediate level of abstraction.

Behavioral vs Dataflow

- Behavioral

```
if(in == 1)
    out <= 0;
elseif(in == 0)
    out <= 1;
```

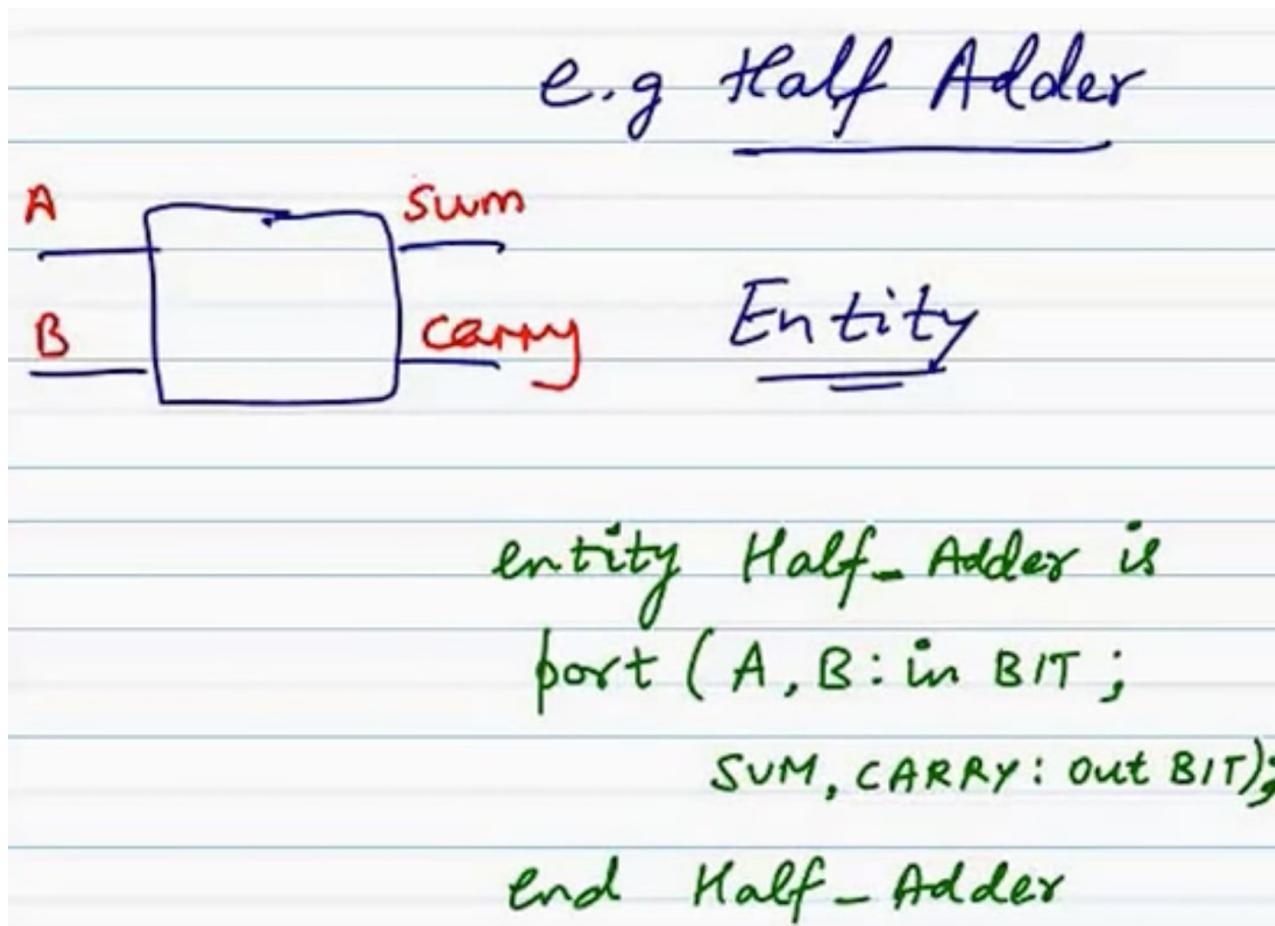
- Dataflow modeling

```
out <= ! in;
```

Behavioral and Structural VHDL

- Structural model:
 - Describes gates and flip-flops in the circuit.
 - Gates and flip-flops can be defined in a separate VHDL module.
- Behavioral design is often used for quick time-to-market.

Structural VHDL- Half Adder



Structural VHDL- Half Adder

Structural Style of Modeling

architecture Structure_HA of Half_Adder is

component XOR1

port(P, Q: in BIT ; R : out BIT);

end component;

component AND1

port(X, Y: in BIT ; Z : out BIT);

end component;

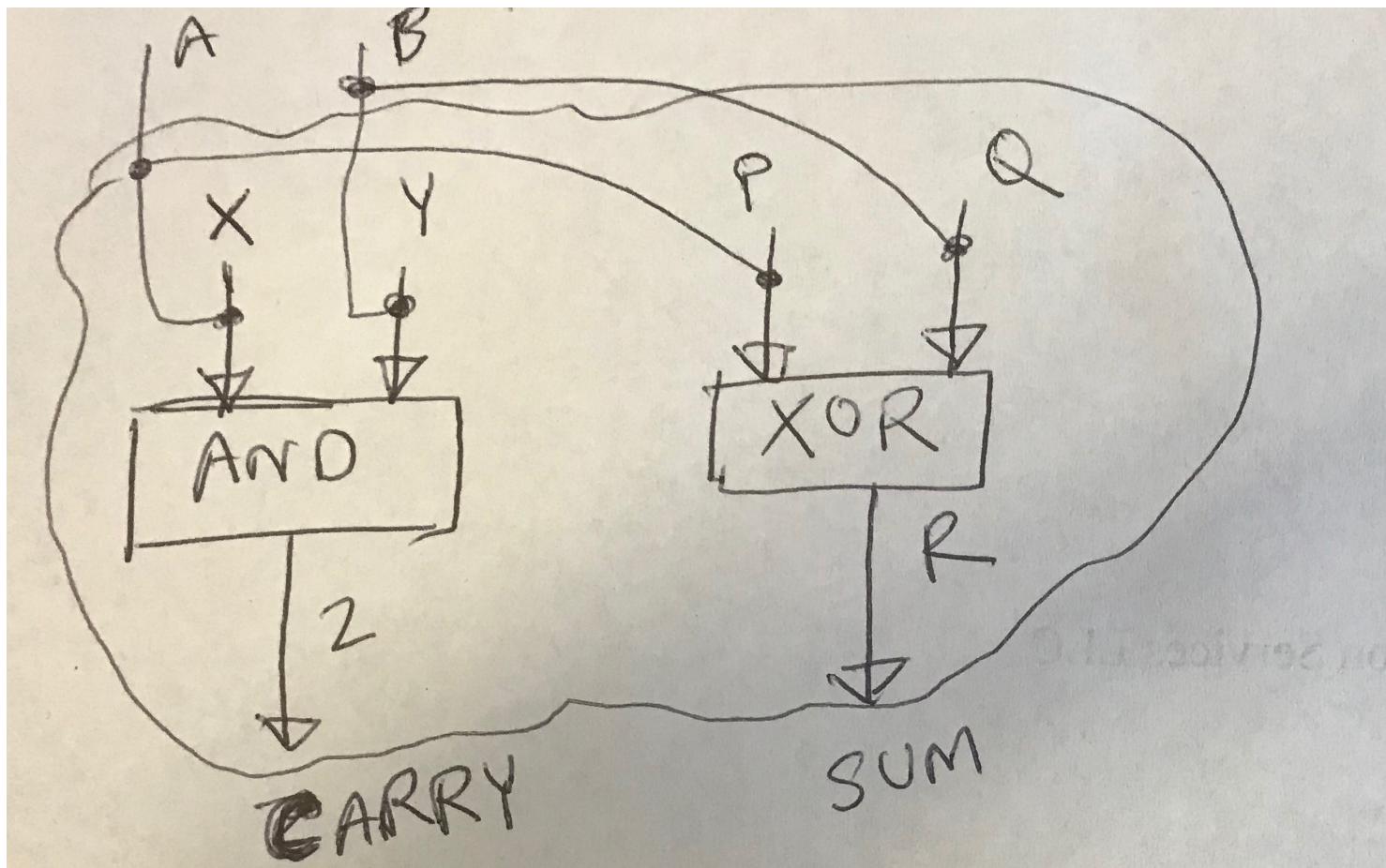
begin

X1: XOR1 port map (A, B, SUM);

A1: AND2 port map (A, B, CARRY);

end Structure_HA;

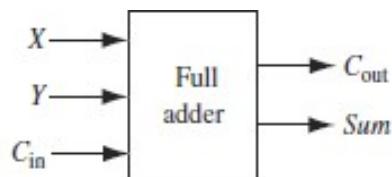
Structural VHDL- Half Adder



Structural VHDL- Full Adder

- Full adder entity:

FIGURE 2-10: Entity Declaration for a Full Adder Module

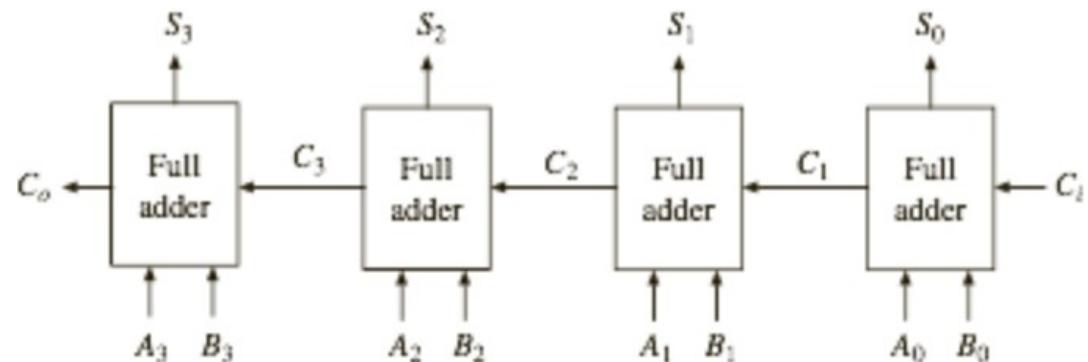


```
entity FullAdder is
  port(X, Y, Cin: in bit;      --Inputs
       Cout, Sum: out bit);   --Outputs
end FullAdder;
```

- Full adder architecture:

```
architecture Equations of FullAdder is
begin      -- concurrent assignment statements
  Sum <= X xor Y xor Cin after 10 ns;
  Cout <= (X and Y) or (X and Cin) or (Y and Cin) after 10 ns;
end Equations;
```

Structural VHDL- Full Adder



Structural VHDL- Full Adder

```
entity Adder4 is
  port(A, B: in bit_vector(3 downto 0); Ci: in bit; -- Inputs
       S: out bit_vector(3 downto 0); Co: out bit); -- Outputs
end Adder4;
architecture Structure of Adder4 is
component FullAdder
  port (X, Y, Cin: in bit;      -- Inputs
        Cout, Sum: out bit);    -- Outputs
end component;
signal C: bit_vector(3 downto 1); -- C is an internal signal
begin      --instantiate four copies of the FullAdder
  FA0: FullAdder port map (A(0), B(0), Ci, C(1), S(0));
  FA1: FullAdder port map (A(1), B(1), C(1), C(2), S(1));
  FA2: FullAdder port map (A(2), B(2), C(2), C(3), S(2));
  FA3: FullAdder port map (A(3), B(3), C(3), Co, S(3));
end Structure;
```

Transport and Inertial Delays

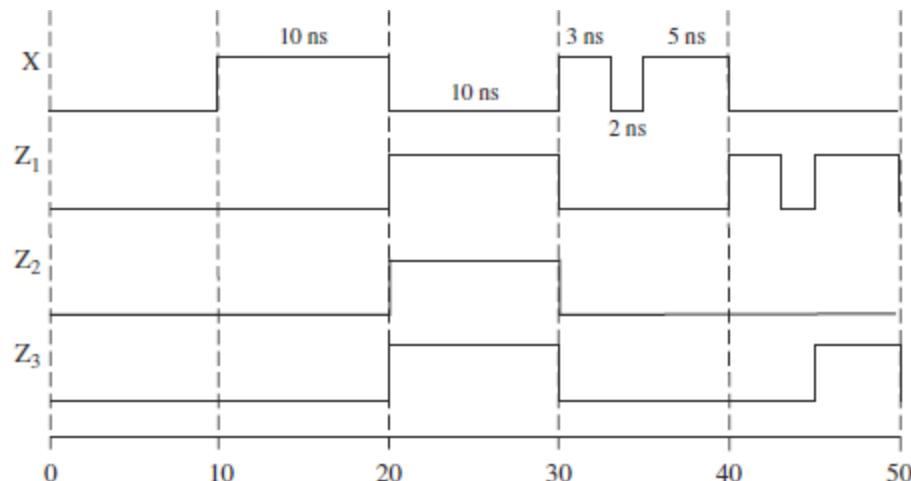
- **Inertial delay:** intended to model gates and other devices that do not propagate short pulses from the input to the output.
- **Transport delay:** intended to model the delay introduced by wiring; it simply delays an input signal by the specified delay time.

Transport and Inertial Delays (continued)

- Example of inertial and transport delays:

```
Z1 <= transport X after 10 ns; -- transport delay  
Z2 <= X after 10 ns; -- inertial delay  
Z3 <= reject 4 ns inertial X after 10 ns;  
-- inertial delay with specified rejection pulse width
```

FIGURE 2-23: Transport and Inertial Delays



ISE Project Navigator (O.87xd) - C:\VHDLDesign\Example\Example.xise - [myMUX4.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- Example
 - xc3s500e-4fg320
 - myMUX4 - Behavioral (myMUX4.vhd)

No Processes Running

Processes: myMUX4 - Behavioral

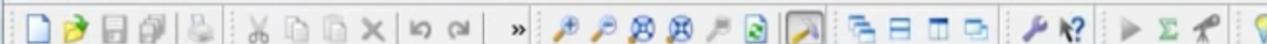
- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
 - View RTL Schematic
 - View Technology Schematic
 - Check Syntax
 - Generate Post-Synthesis Simulation...
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

myMUX2.vhd | Design Summary (out of date) | myMUX4.vhd

Console

```
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
INFO:HDLCompiler:1061 - Parsing VHDL file "C:/VHDLDesign/Example/myMUX4.vhd" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
```

```
1
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4
5 entity myMUX4 is
6     Port ( A : in STD_LOGIC;
7             B : in STD_LOGIC;
8             C : in STD_LOGIC;
9             D : in STD_LOGIC;
10            S : in STD_LOGIC_VECTOR (1 downto 0);
11            Y : out STD_LOGIC);
12 end myMUX4;
13
14 architecture Behavioral of myMUX4 is
15 -- Declare all components being used in MUX4
16 component myMUX2 is
17     Port ( A : in STD_LOGIC;
18             B : in STD_LOGIC;
19             S : in STD_LOGIC;
20             Y : out STD_LOGIC);
21 end component;
22 -- Declare all signals
23 signal t1, t2 : STD_LOGIC;
24
25 begin
26
27 U1: myMUX2 port map (A, B, S(0), t2);
28 U2: myMUX2 port map (C, D, S(0), t1);
29
30 U3: myMUX2 port map (t2, t1, S(1), Y);
31
32
33 end Behavioral;
34
35
```



Design

View: Implementation Simulation

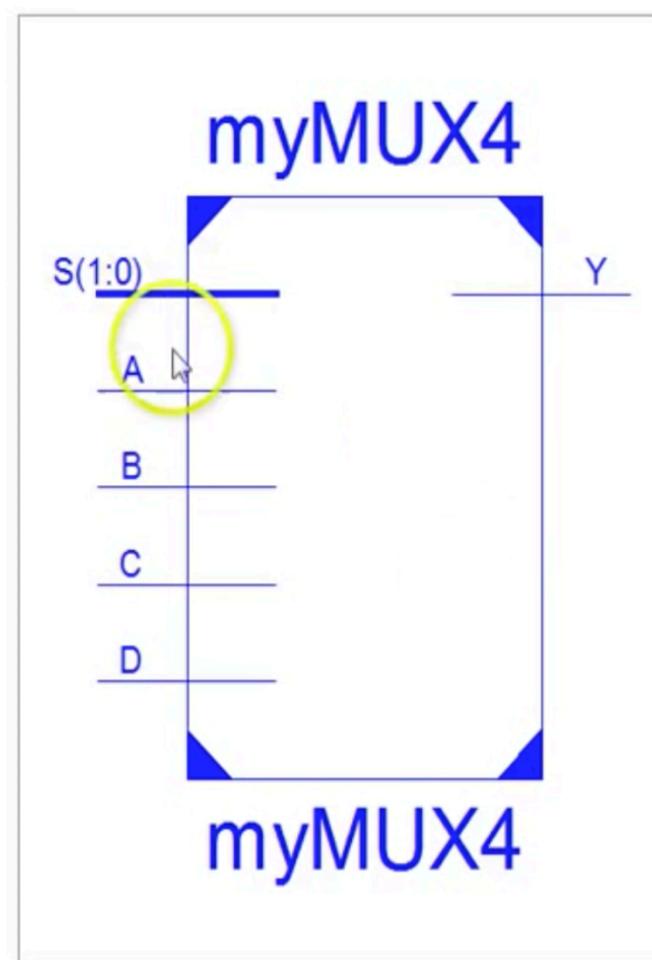
Hierarchy

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No Processes Running

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myMUX2.vhd Design Summary (Synthesized) myMUX4.vhd myMUX4 (RTL 1)

View by Category

Design Objects of Top Level Block

Properties: (No Selection)

Instances	Pins	Signals	Name	Value
myMUX4				



Design

View: Implementation Simulation

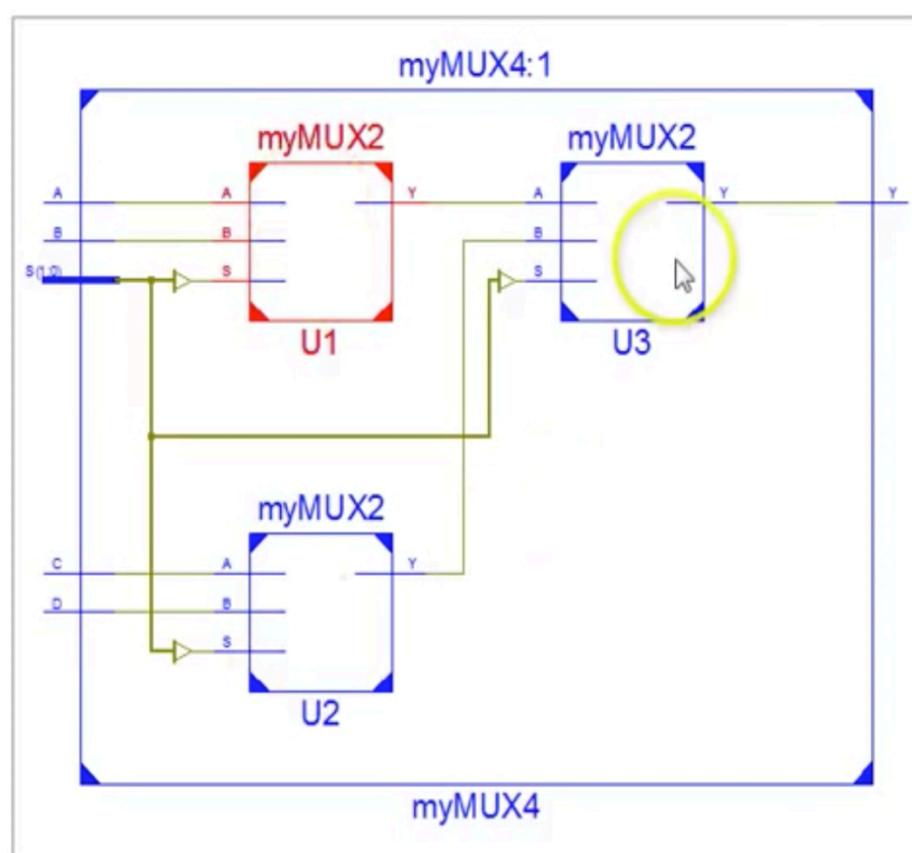
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Processes: myMUX4 - Behavioral

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Design Objects of Top Level Block

Properties of Instance: U1

Instances	Pins	Signals	Name	Type	Value
myMUX4 U1	myMUX4	myMUX4	myMUX2	Instance Name	U1