

Lecture 2 (Chapter 1)

Review of Logic Fundamentals

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ECE 4250/7250

Boolean Algebra and Algebraic Simplification

- DeMorgan's Law:
 - Complement all the terms in the expression:
 - Replace each variable by its complement.
 - Switch 1 with 0 and 0 with 1.
 - Change all ANDs to ORs and all ORs to ANDs.
 - Add parentheses to ensure proper order of operations.
 - If AND is performed before OR in F , then parentheses may be required to ensure that OR is performed before AND in F' .

Boolean Algebra and Algebraic Simplification (cont'd)

- Operations with 0 and 1:

- $\bullet X + 0 = X$

$$X \cdot 1 = X$$

- $\bullet X + 1 = 1$

$$X \cdot 0 = 0$$

- Idempotent laws

- $\bullet X + X = X$

$$X \cdot X = X$$

- Involution law:

- $\bullet (X')' = X$

- Laws of complementarity:

- $\bullet X + X' = 1$

$$X \cdot X' = 0$$

Boolean Algebra and Algebraic Simplification (cont'd)

- Commutative laws:

- $$\bullet X + Y = Y + X \quad XY = YX$$

- **Associative laws:**

- $(X + Y) + Z = X + (Y + Z) = X + Y + Z$
 - $(XY)Z = X(YZ) = XYZ$

- Distributive laws:

- $X(Y + Z) = XY + XZ$
 - $X + YZ = (X + Y)(X + Z)$

Boolean Algebra and Algebraic Simplification (cont'd)

- Simplification theorems:

- $XY + XY' = X$
 - $X + XY = X$
 - $(X + Y')Y = XY$

$$(X + Y)(X + Y') = X$$

$$X(X + Y) = X$$

$$XY' + Y = X + Y$$

- DeMorgan's laws:

- $(X + Y + Z + \dots)' = X'Y'Z'\dots$ $(XYZ\dots)' = X' + Y' + Z' + \dots$
 - $[f(X_1, X_2, \dots, X_N, 0, 1, +, \bullet)]' = f(X_1', X_2', \dots, X_N', 1, 0, \bullet, +)$

Boolean Algebra and Algebraic Simplification (cont'd)

- Duality:

- $(X + Y + Z + \dots)^D = XYZ \dots$ $(XYZ\dots)^D = X + Y + Z + \dots$
- $[f(X_1, X_2, \dots X_N, 0, 1, +, \bullet)]^D = f(X_1, X_2, \dots X_N, 1, 0, \bullet, +)$

- Theorem for multiplying out and factoring:

- $(X + Y)(X' + Z) = XZ + X'Y$
- $XY + X'Z = (X + Z)(X' + Y)$

- Consensus theorem:

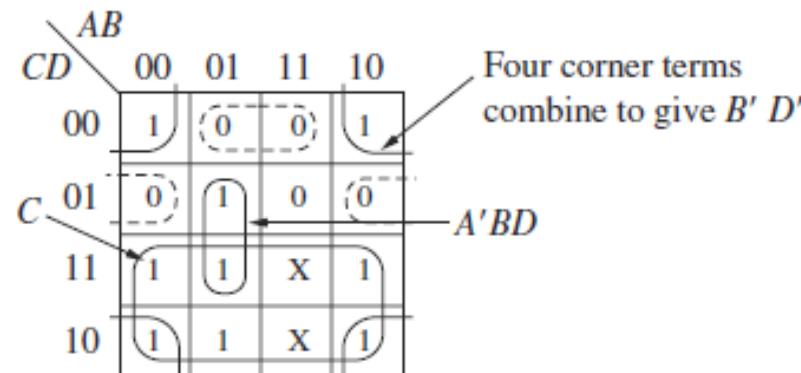
- $XY + YZ + X'Z = XY + X'Z$
- $(X + Y)(Y + Z)(X' + Z) = (X + Y)(X' + Z)$

Karnaugh Maps

- K-maps provide a convenient way to simplify logic functions of three to five variables.
- 4 variable K-maps:

		AB	00	01	11	10
		CD	00	4	12	8
		00	0	1	13	9
		01	3	7	15	11
		10	2	6	14	10

(a) Location of minterms



$$\begin{aligned}F &= \sum m (0, 2, 3, 5, 6, 7, 8, 10, 11) + \sum d (14, 15) \\&= C + B' D' + A' BD\end{aligned}$$

(b) Looping terms

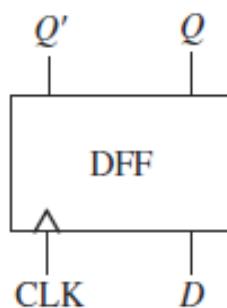
Karnaugh Maps (cont'd)

- Procedure to obtain a minimum sum of products from a Karnaugh map:
 - 1. Choose a minterm (a 1) that has not yet been covered.
 - 2. Find all 1's and X's adjacent to that minterm.
 - 3. If a single term covers the minterm and all the adjacent 1's and X's, then that term is an essential prime implicant, so select that term.
 - 4. Repeat steps 1, 2, and 3 until all essential prime implicants have been chosen.
 - 5. Find a minimum set of prime implicants that cover the remaining 1's on the map.

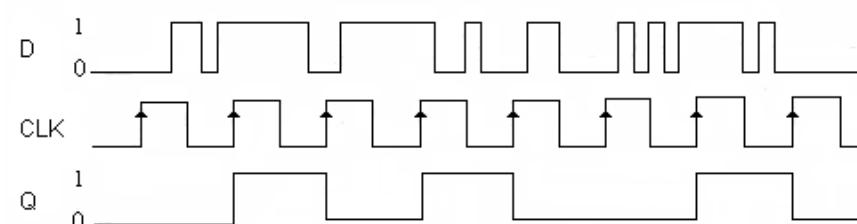
Flip-Flops and Latches

- Sequential circuits commonly use flip-flops as storage devices. Some types include:
 - Delay (D) flip-flops, J-K flip-flops, Toggle (T) flip-flops

Clocked D Flip-Flop:

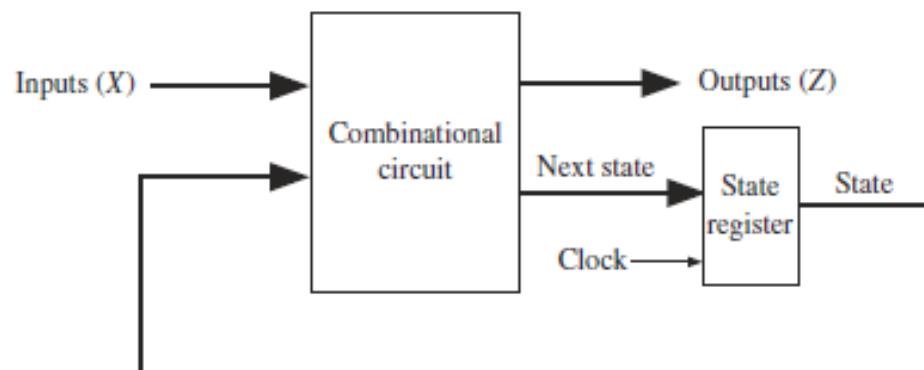


D	Q		Q ⁺
0	0		0
0	1		0
1	0		1
1	1		1



Mealy Sequential Circuit Design

- Two types of sequential circuits:
 - Moore: the outputs depend only on the present state.
 - Mealy: the outputs depend on both the present state and the present inputs.
 - Consists of a combinational circuit, which generates the outputs and the next state, and a state register, which holds the present state. The state register is usually comprised of D flip-flops.



Moore Sequential Circuit Design

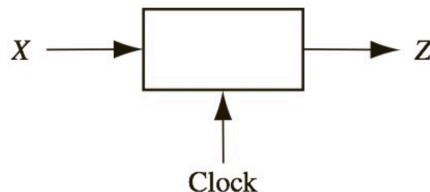
- Outputs depend only on the present state.
- Easier to design and debug than Mealy machines, but often contain more states than equivalent Mealy machines.
- No outputs occur during the transition.
- Cannot respond to an input until the active edge of the clock occurs; this is in contrast to a Mealy circuit.

Example (Mealy)

1.7.1 Mealy Machine Design Example 1: Sequence Detector

To illustrate the design of a clocked Mealy sequential circuit, a sequence detector is presented. The circuit has the form indicated in the block diagram in Figure 1-18.

FIGURE 1-18: Block Diagram of a Sequence Detector



The circuit will examine a string of 0's and 1's applied to the X input and generate an output $Z = 1$ only when the input sequence ends in 1 0 1. The input X can change only between clock pulses. The output $Z = 1$ coincides with the last 1 in 1 0 1. The circuit does not reset when a 1 output occurs. A typical input sequence and the corresponding output sequence are

$$X = 0 \ 0 \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0$$

$$Z = 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0$$

Example (cont.)

FIGURE 1-20: Mealy State Graph for Sequence Detector

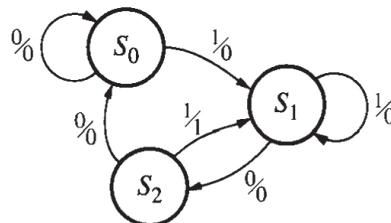


TABLE 1-3: State Table for Sequence Detector

Present State	Next State		Present Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_0	S_1	0	1

TABLE 1-4: Transition Table for Sequence Detector

AB	A^+B^+		Z	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
00	00	01	0	0
01	10	01	0	0
10	00	01	0	1

Example (cont.)

FIGURE 1-21: K-Maps for Next States and Output of Sequence Detector

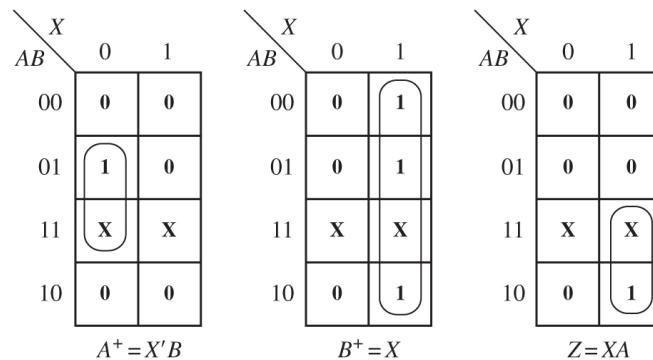
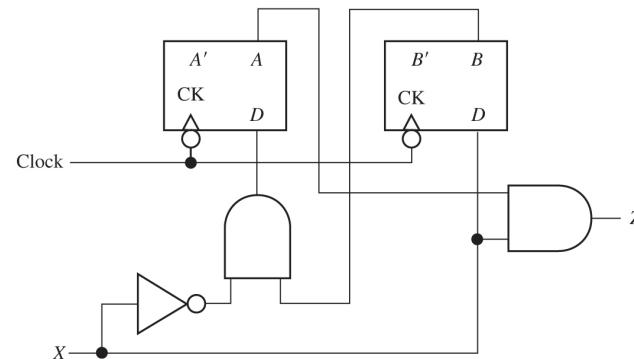


FIGURE 1-22: Circuit for Mealy Sequence Detector



Example (Moore)

FIGURE 1-28: State Graph of the Moore Sequence Detector

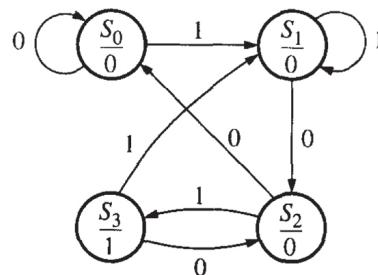


TABLE 1-7: State Table for Sequence Detector

Present State	Next State		Present Output (Z)
	$X = 0$	$X = 1$	
S_0	S_0	S_1	0
S_1	S_2	S_1	0
S_2	S_0	S_3	0
S_3	S_2	S_1	1

TABLE 1-8: Transition Table for Moore Sequence Detector

AB	A^+B^+		Z
	$X = 0$	$X = 1$	
00	00	01	0
01	11	01	0
11	00	10	0
10	11	01	1

Sequential Circuit Timing

- The correct functioning of sequential circuits involves several timing issues:
 - Propagation Delay or Clock-to-Q delay: small amount of time that elapses from the time the clock changes to the time the Q output changes.
 - Setup Time (t_{su}): the amount of time the D input is stable before the active edge of the clock.
 - Hold time (t_h): the amount of time the D input is stable after the active edge of the clock.

Summary

- This chapter serves as a review of important logic design topics such as:
 - Combinational logic
 - Sequential logic
 - Sequential circuit timing