GATE -2023 BM: 18Q

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Question: An 8 bit successive approximation Analog to Digital Converter (ADC) has a clock frequency of 1 MHz. Assume that the start conversion and end conversion signals occupy one clock cycle each. Among the following options, what is the maximum frequency that this ADC can sample without aliasing?

a) 0.9 kHz
b) 9.9 kHz
c) 49.9 kHz
d) 99.9 kHz