UNIT-3

D-A and A-D converters

→ Introduction:

→ Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc, are available in analog form.

→ Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superimposition of noise as in the case of amplitude modulation.

→ Therefore, for processing, transmission and storage purposes, it is often convenient to express these variable in digital form.

→ It gives better accuracy and reduces noise.

→ The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

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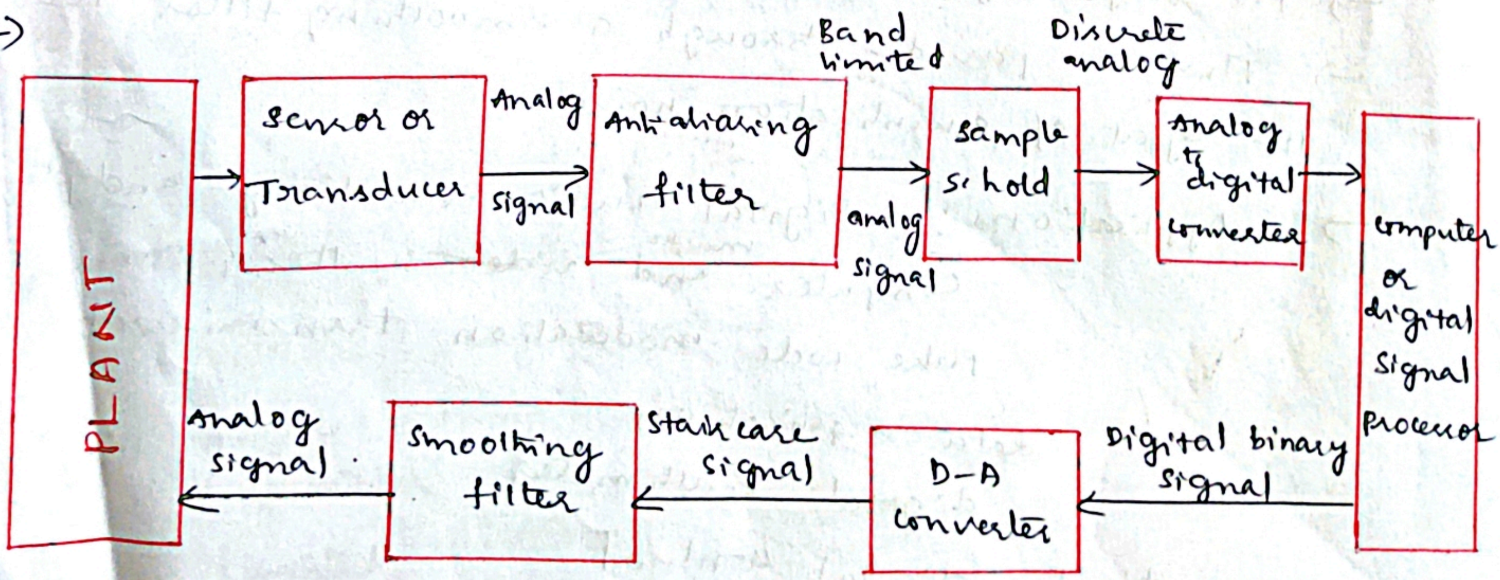


Fig: circuit showing application of A/D and D/A converter.

→ The fig. highlights a typical application within which A/D and D/A conversion is used.

→ The analog signal obtained from the transducer is band limited by antialiasing filter.

→ The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.

→ The sampled signal has to be held constant while conversion is taking place in A/D converter.

→ This requires that ADC should be preceded by a sample and hold (S/H) circuit.

→ The ADC output is a sequence in binary digit.

→ The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm.

→ The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC.

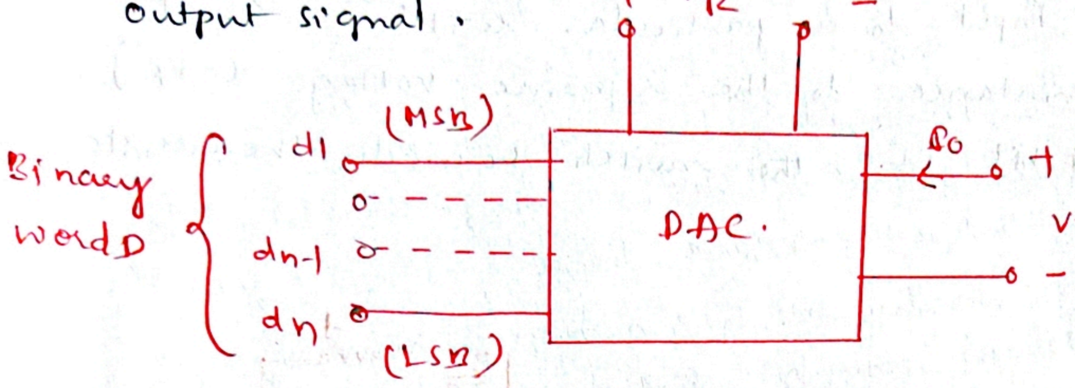
→ The output of a D/A converter is commonly a staircase.

→ This is passed through a smoothing filter to reduce the effect of quantization noise.

→ Applications: Digital audio recording and play back
computer music and video synthesis
pulse code modulation transmission
data acquisition
digital multimeter
direct digital control
digital signal processing
microprocessor based instrumentation.

→ Basic DAC techniques:-

The schematic of a DAC is shown.
→The input is an n-bit binary work and is combined with a reference voltage V_R to give an analog output signal.



→ The output of a DAC can be either a voltage or current.
→ For a voltage output DAC, the D/A converter is mathematically described as

$$V_0 = K V_{FS} (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \dots + d_n 2^{-n})$$

where, V_0 = output voltage

V_{FS} = full scale output voltage.

K = scaling factor usually adjusted to unity

$d_1 d_2 \dots d_n$ = n- bit binary fractional word with the decimal point located at the left.

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

→ The various ways to implement this is
1) weighted resistor DAC
2) R-2R ladder
3) Inverted R-2R ladder

→ Weighted resistor DAC:-
→ One of the simplest circuits shown uses a summing

amplifier with a binary weighted resistor network.

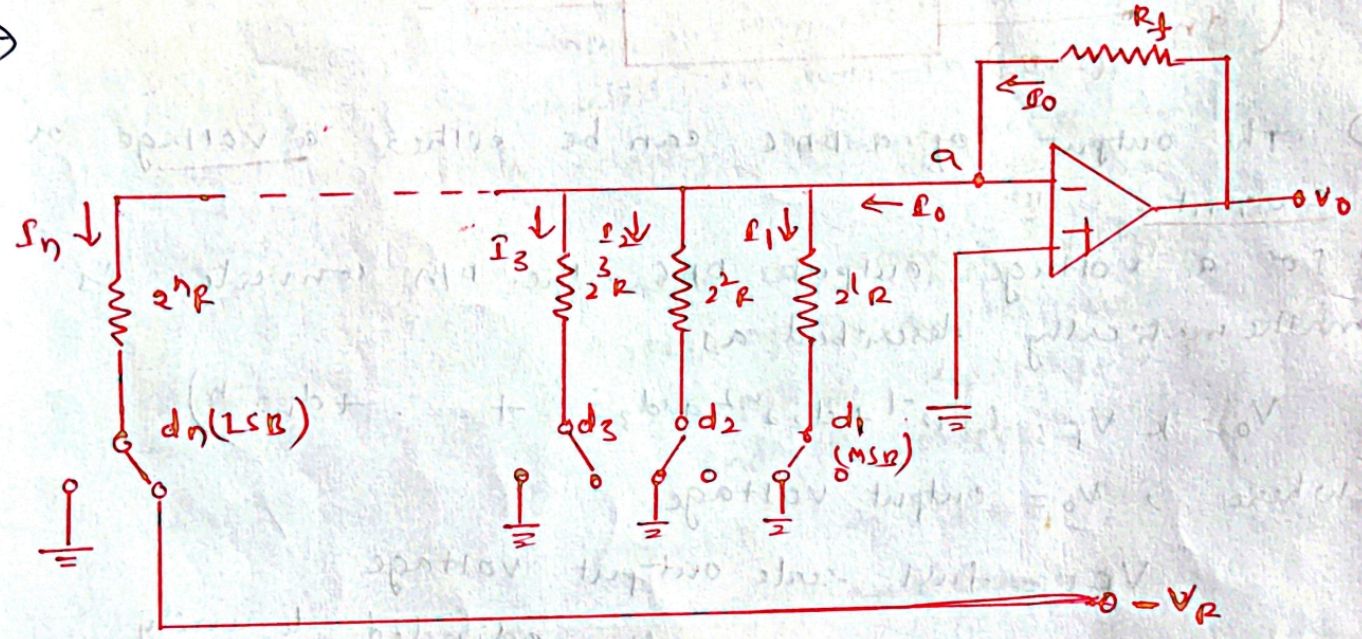
→ It has n-electronic switches $d_1, d_2, \ldots, d_n$ controlled by binary input word.

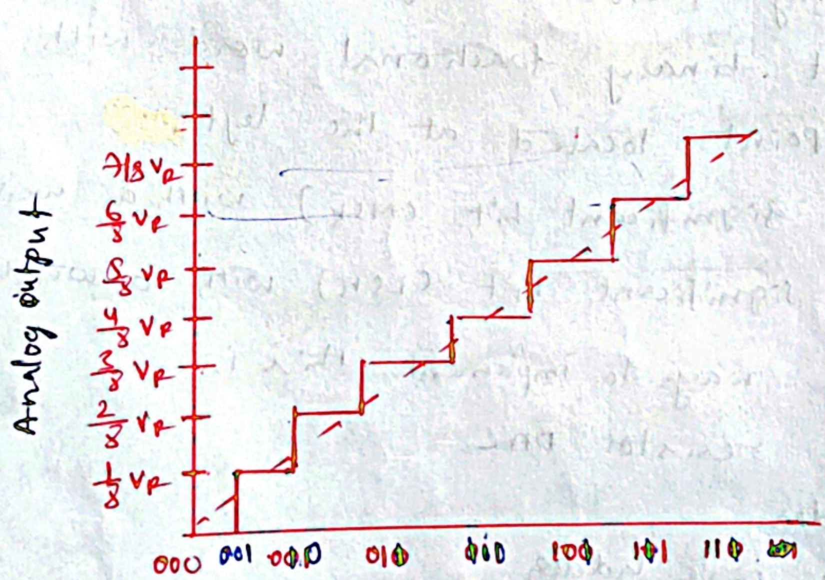
→ These switches are single pole double throw (SPDT) type.

→ If the binary input to a particular switch is 1, it connects the resistance to the reference voltage $(-V_R)$.

→ And if the input bit is 0, the switch connects the resistor to the ground.

→





→ from fig. the output current I_0 for an ideal op-amp

$$I_0 = I_1 + I_2 + I_3 + \cdots + I_n.$$

$I_1 = \frac{(0-(-V_R))d_1}{2R}$

$I_0 = \frac{V_0 - 0}{R_f}$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \cdots + \frac{V_R}{2^n R} d_n$$

$$I_0 = \frac{V_R}{R} \left(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n} \right)$$

The o/p vol $V_0 = I_0 R_f = V_R \frac{R_f}{R} \left(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n} \right)$

On comparing, $R_f = R$, then $K = 1$ and $V_{FS} = V_R$

→ The circuit shown uses a negative reference voltage.

→ The analog output voltage is therefore positive staircase for a 3-bit weighted resistor DAC.

(i) Although the op-amp is connected in inverting mode, it can also be connected in non-inverting mode.

(ii) The op-amp is simply working as a current to voltage converter.

(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be +5V and the output will be negative.

→ The accuracy and stability of a DAC depends upon the accuracy of the resistors and tracking of each other with temperature.

→ Disadvantages — The wide range of resistor values required.

→ For better resolution, the input binary word length has to be increased.

→ Thus, as the number of bit increases, the range of resistance value increases.

→ For 8-bit DAC, the resistors required are $2^0 R, 2^1 R, \ldots 2^7 R$.

→ The largest is 128 times the smallest.

→ For 12-bit DAC, the largest resistance required is 5.12MΩ if the smallest is 2.5KΩ.

→ The fabrication of such a large resistance in IC is not practical.

→ R-2R ladder DAC :-

→ Wide range of resistors are required in binary weighted resistor type DAC.

→ This can be avoided by using R-2R ladder type DAC where only two values of resistors are required.

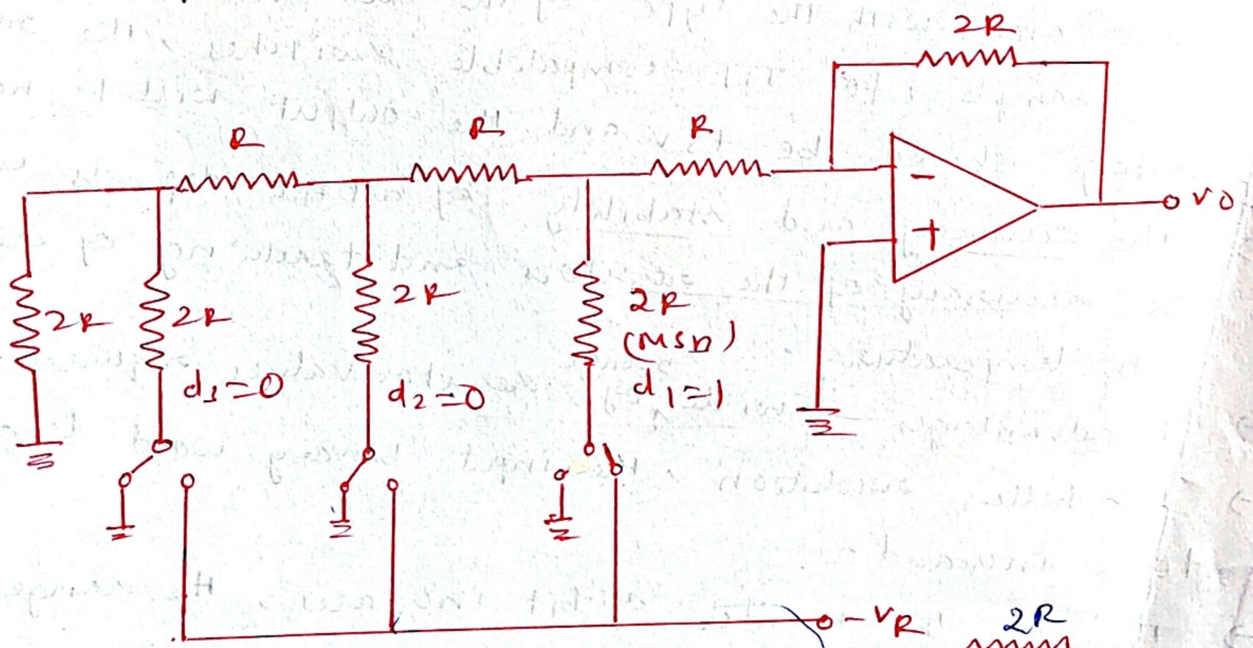
→ It is well suited for integrated circuit realization.

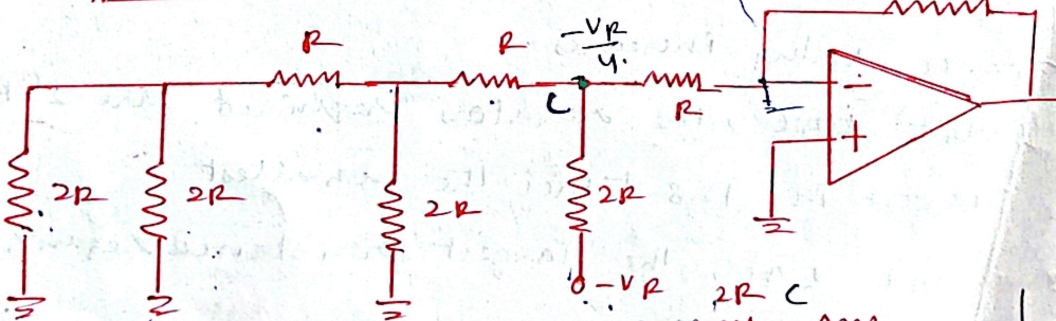
→ The typical value of R ranges from 2.5kΩ to 10kΩ.

→ For simplicity, consider a 3-bit DAC shown where the switch position $d_1 d_2 d_3$ corresponds to the binary word 100.

→ The circuit can be simplified to the equivalent form.

→ Then, voltage at node 'c' can be easily calculated by the set procedure of network analysis as,

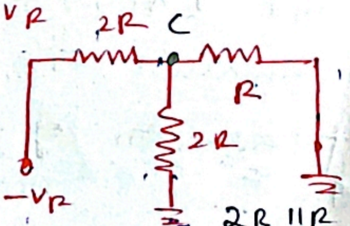




$(2R \| 2R)$ $(R+R)$ $2R \| 2R$

$\frac{2R \times 2R}{2R+2R}$ $2R$ $\simeq R$

$\frac{4R^2}{4R}$ $\simeq R$ $R+R = 2R$



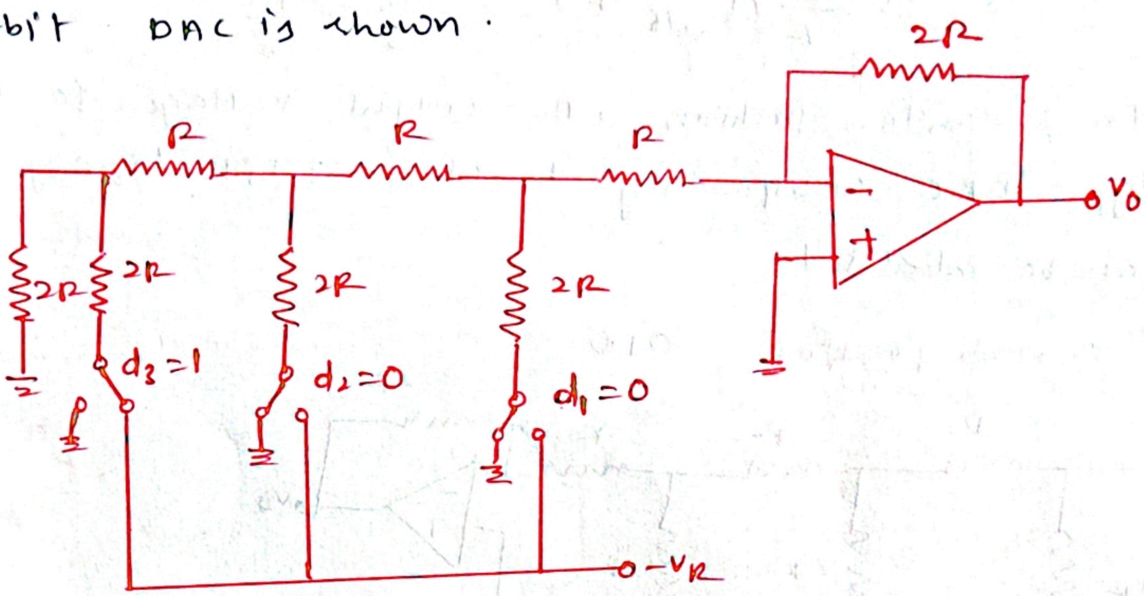
$2R \| R = \frac{2R}{3}$

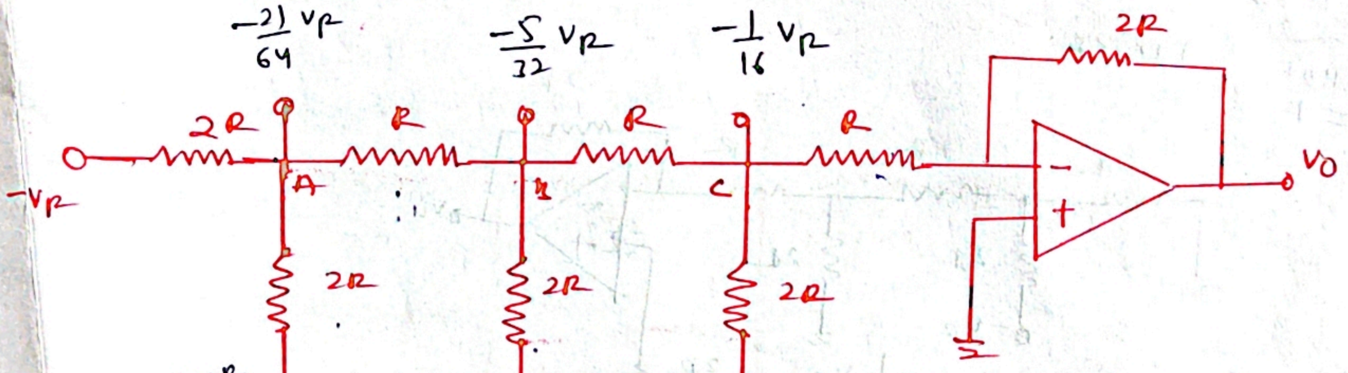
$$\left(\frac{\frac{2R}{3}}{\frac{2R}{3}+2R}\right)(-V_R) = \frac{2R}{8R}(-V_R)$$

the output voltage, $V_o = (-\frac{R_f}{R_1}) V_{in}$

$$= \left(\frac{-2R}{R}\right)\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

→ The switch position corresponding to the binary word 001 in 3-bit DAC is shown.





eq. resistance $= \frac{42R}{43}$ $\quad \frac{10R}{11}$ $\quad \frac{2}{3}R$ $\quad 2R \| R \rightarrow \frac{2}{3}R$

$\frac{21R}{11} \| 2R$

$\frac{\frac{21R}{11} \times 2R}{\frac{21R}{11} + 2R} = \left(\frac{42R}{43}\right)$

$\frac{10R}{11} + R$

$\frac{21R}{11}$

$\frac{5R}{3} \| 2R$

$\frac{\frac{5R}{3} \times 2R}{\frac{5R}{3} + 2R}$

$= \frac{10R}{11}$

$\frac{2}{3}R + R = \frac{5R}{3}$

vol. at A $= \left(\frac{\frac{42R}{43}}{\frac{42R}{43} + 2R}\right)(-V_R) = \left(\frac{42R}{42R + 86R}\right)(-V_R) = \frac{\cancel{42}^{21}\cancel{R}}{\cancel{128}_{64}\cancel{R}}(-V_R) = -V_R\frac{21}{64}$

vol. at B $= \left(\frac{\frac{10R}{11}}{\frac{10R}{11} + R}\right)\left(-\frac{21}{64}V_R\right) = \frac{\cancel{10}^{5}R}{\cancel{21}R}\left(\frac{-\cancel{21}}{\cancel{64}_{32}}V_R\right) = \frac{-5}{32}V_R$

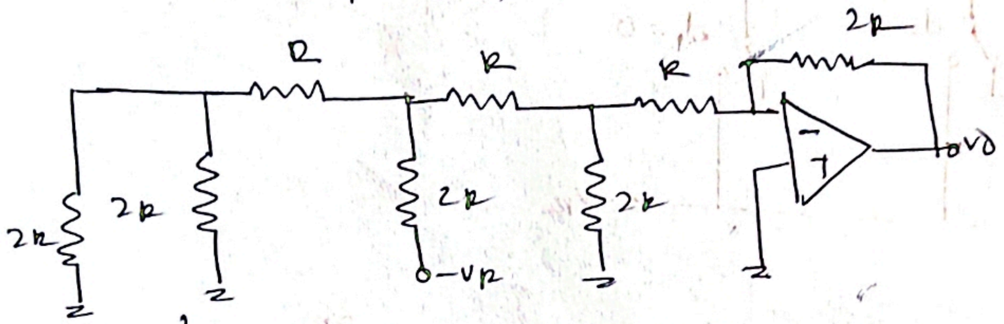
vol at c $= \left(\dfrac{\frac{2R}{3}}{\frac{2}{3}R+R}\right)\left(-\dfrac{5}{32}V_R\right) = \dfrac{2R}{5R}\left(-\dfrac{5}{32}V_R\right)$

$= -\dfrac{1}{16}V_R$

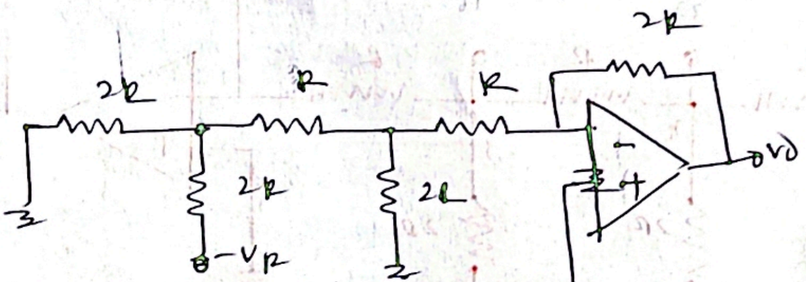
$\therefore V_0 = \left(-\dfrac{2R}{R}\right)\left(-\dfrac{1}{16}V_R\right) = \dfrac{V_R}{8} = \dfrac{V_{FS}}{8}$

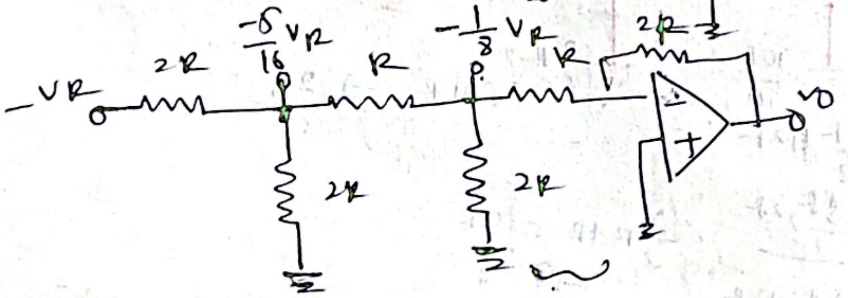
→ In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

→ switch position 010



$\underbrace{\quad}_{\substack{2R \parallel 2R \\ = R}}$ $R+R=2R$.





$\dfrac{10R}{11}$ $\qquad$ $\dfrac{2}{3}R$

$\left(\dfrac{\frac{10R}{11}}{\frac{10R}{11}+2R}\right)(-V_R)$

$= \dfrac{10R}{32R}(-V_R)$

$= -\dfrac{5}{16}V_R$

$\left(\dfrac{\frac{2}{3}R}{\frac{2}{3}R+R}\right)\left(-\dfrac{5}{16}V_R\right)$

$\left(\dfrac{\cancel{2}R}{\cancel{5}R}\right)\left(-\dfrac{\cancel{5}}{16}V_R\right)$

$V_0 = \left(-\dfrac{2R}{R}\right)\left(-\dfrac{1}{8}V_R\right)$

$= \dfrac{V_R}{4}$

→ Inverted R-2R ladder DAC

→ In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes.

→ More power dissipation causes heating, which in turn, creates non-linearity in DAC.

→ This is a serious problem and can be avoided completely in 'Inverted R-2R ladder type DAC'.

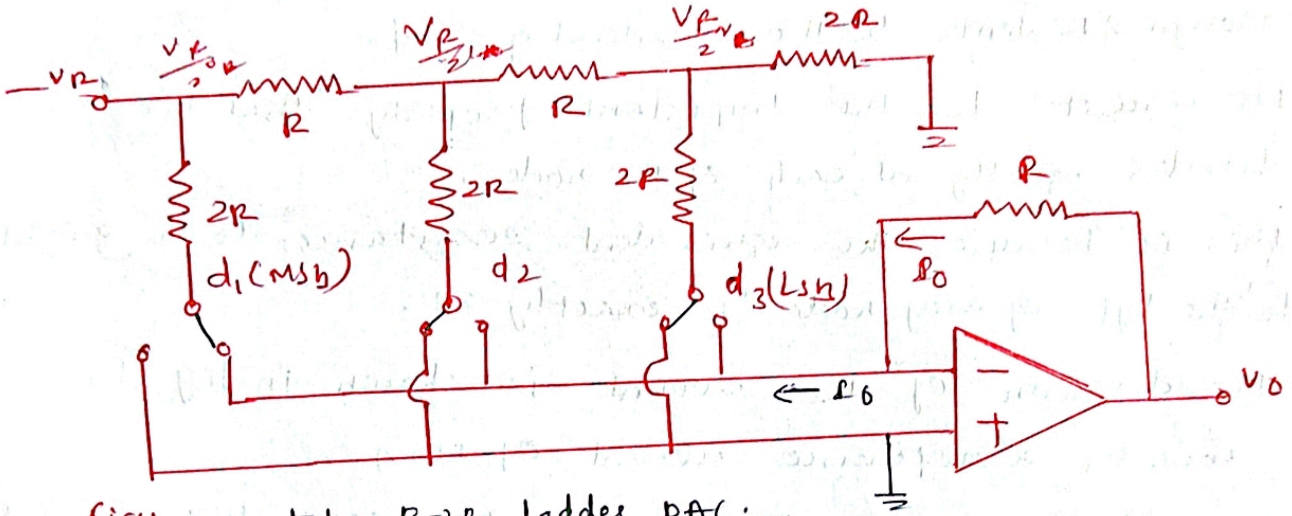


fig: Inverted R-2R ladder DAC.

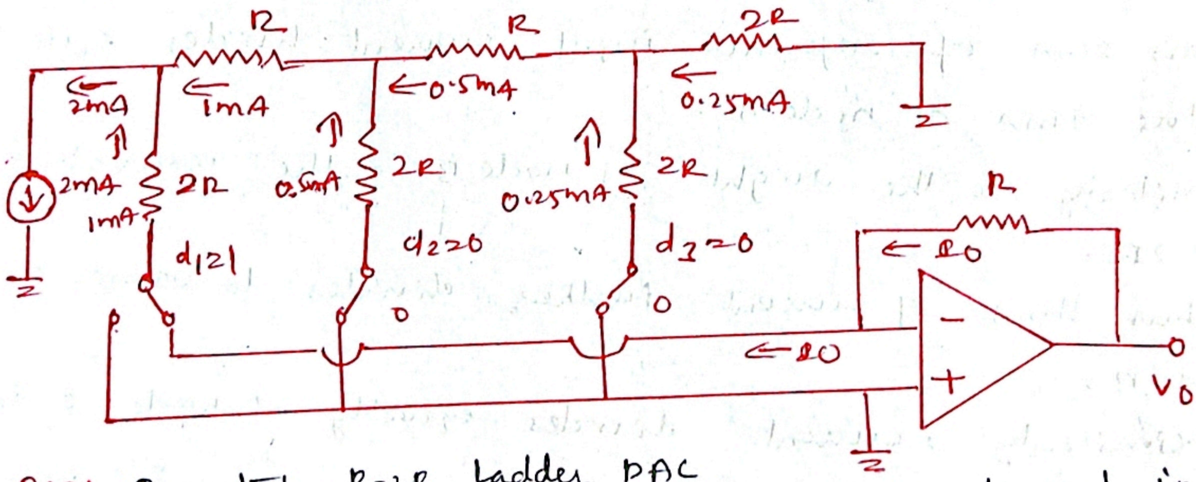


Fig: Inverted R-2R ladder DAC showing division of current for digital input word 001

→ A 3-bit inverted R-2R ladder type DAC is shown where the position of MSB and LSB is interchanged.

→ Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground.

→ Since both the terminals of switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e, independent of input binary word.

→ In fig.(a) when switch d_i at logical '0' i.e, to the left, the current through 2R resistor flows to the ground and. When the switch d_i at logical '1' i.e, to the right, the current through 2R sinks to the virtual ground.

→ The circuit has the important property that the currents divides equally at each of the nodes.

→ This is because the equivalent resistance to the right or to the left of any node is exactly 2R.

→ The division of the current is shown in fig (b).

→ consider a reference current of 2mA.

→ Just to the right of node A, the equivalent resistor is 2R.

→ Thus 2mA of reference input current divides equally to value 1mA at node A.

→ Similarly to the right of node B, the equivalent resistor is 2R.

→ Thus 1mA of current further divides to value 0.5mA at node B.

→ similarly, current divides equally at node C to 0.25mA.

→ The equal division of current in successive nodes remains the same in the 'inverted R-2R ladder' irrespective of the input binary word.

→ Thus the currents remain constant in each branch of the ladder.

→ since constant current implies constant voltage, the ladder node voltage remains constant at $V_R/2^0$, $V_R/2^1$, $V_R/2^2$.

→ The circuit works on the principle of summing currents and is also said to operate in the current mode.

→ The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes).