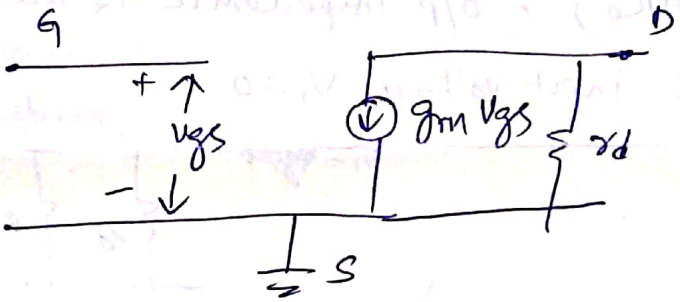
FET Amplifiers

FET is a voltage controlled device as o/p current is controlled by the i/p voltage.

Advantages over BJT

1) FET is a more temperature stable
2) FET has very high i/p impedance & they are preferred in Amplifiers
3) FET require less space than that for BJT hence they are preferred in IC's.

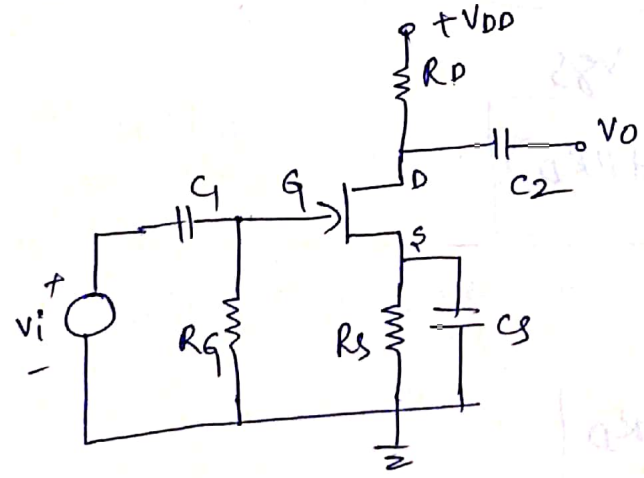
JFET Low frequency Small Signal model



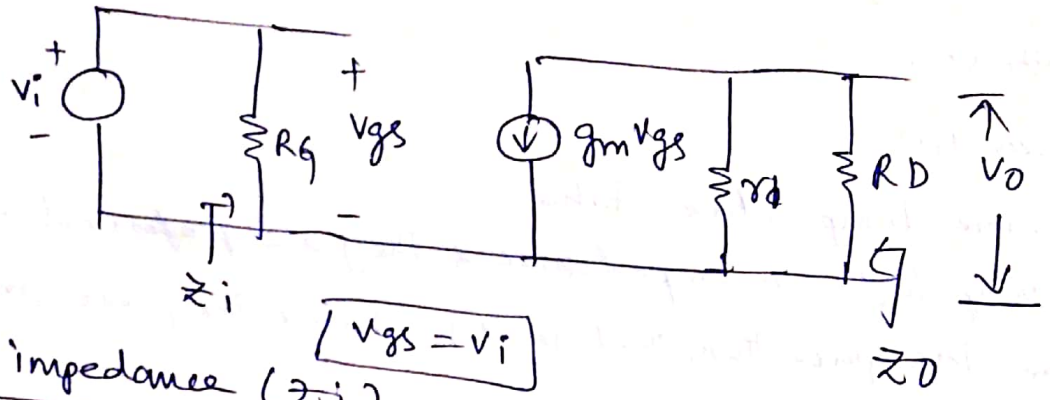
common source

Analysis of JFET Amplifiers

1) common source Amplifier (CS):-



FET Amplifiers provide an excellent voltage gain with added f... in the ... Find ...
high i/p Resistance.



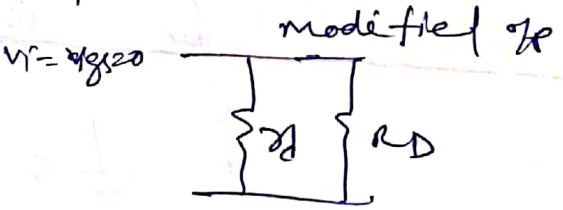
$V_{gs} = V_i$

1) I/p impedance (Z_i)

$$Z_i = R_G$$

2) O/p impedance (Z_o or R_o) :- O/p impedance is measured at the o/p terminals with input voltage $V_i = 0$

$$Z_o = r_d \| R_D$$



3) Voltage Gain (A_V) :-

$$A_V = \frac{V_o}{V_i} = \frac{V_o}{V_{gs}}$$

$$V_o = -g_m V_{gs} \cdot (r_d \| R_D)$$

$$\therefore A_V = -g_m V_{gs} (r_d \| R_D)$$

$$\frac{}{V_{gs}}$$

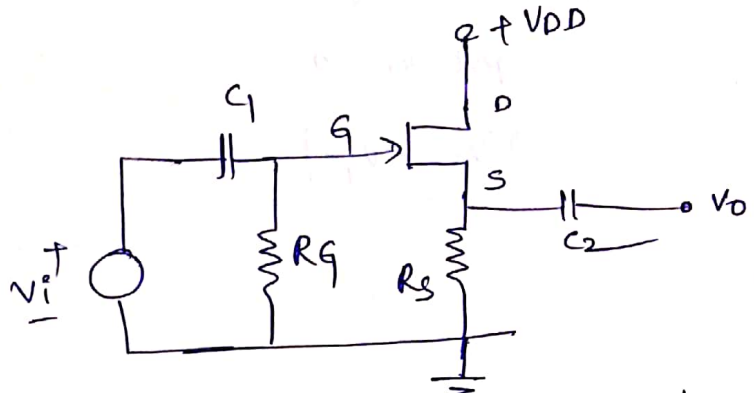
$$\boxed{A_V = -g_m (r_d \| R_D)}$$

if $r_d >> R_D$

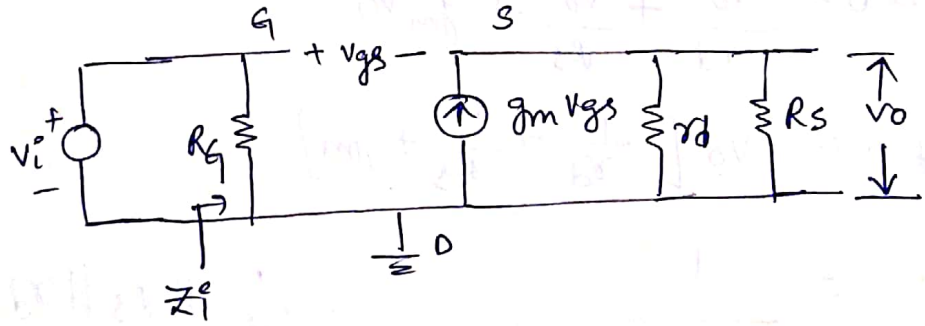
$$\boxed{A_V = -g_m R_D}$$

In the CS Amp let $R_D = 5k\Omega$, $R_G = 10M\Omega$, $\mu = 50$, $r_d = 35k\Omega$.
Find Av, Zi & Zo

) Common Drain (or) source follower

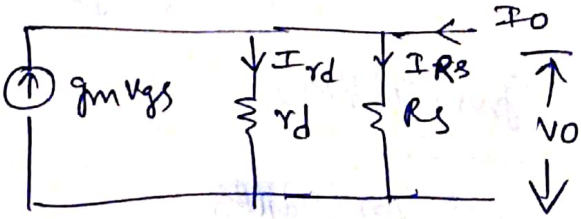


It is also called as buffer Amp because o/p voltage is almost equal to i/p voltage.



1) i/p impedance (Zi) :- $Z_i = R_G$

2) o/p impedance (Zo) :- $Z_O = \frac{V_O}{I_O}$ where $V_i = 0$



Apply KCL

$$g_m V_{gs} + I_o = I_{rd} + I_{Rs}$$

$$g_m V_{gs} + I_o = \frac{V_o}{r_d} + \frac{V_o}{R_s} \longrightarrow (1)$$

Applying KVL to outer loop $V_i = V_{gs} + V_o$

put $V_i = 0$

$$\boxed{V_o = -V_{gs}}$$

Substitute in eq (1)

$$-g_m V_o + I_o = \frac{V_o}{r_d} + \frac{V_o}{R_s}$$

$$I_o = \frac{V_o}{r_d} + \frac{V_o}{R_s} + g_m V_o$$

$$I_o = V_o \left[\frac{1}{r_d} + \frac{1}{R_s} + g_m \right]$$

$$Z_o = \frac{V_o}{I_o} = \frac{1}{1/r_d + 1/R_s + g_m} = \frac{1}{g_m} \| R_s \| r_d$$

Voltage Gain (A_V)

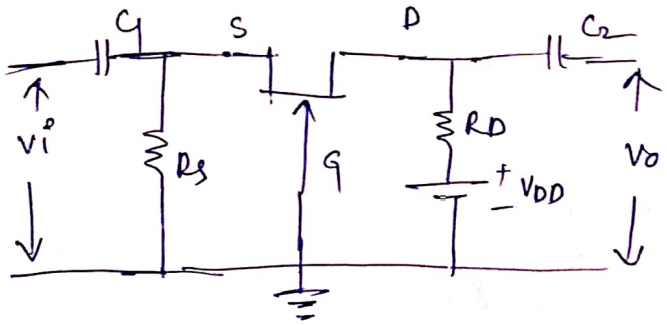
$$A_V = \frac{V_o}{V_i} = \frac{+ g_m V_{gs} (r_d \| R_s)}{V_{gs} + g_m V_{gs} (r_d \| R_s)}$$

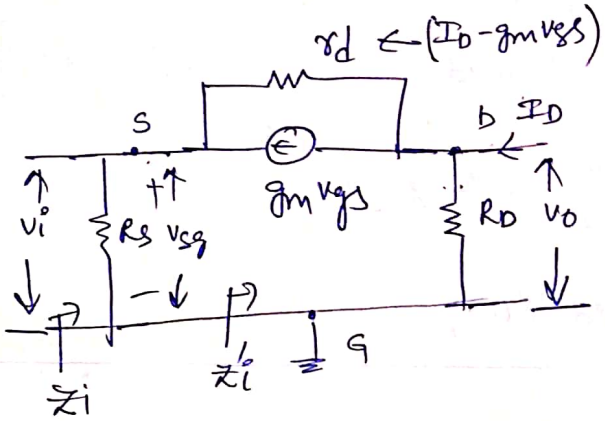
$$A_V = \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)}$$

$\boxed{A_V \simeq 1}$

① In CD $g_m = 2.5\ mo/V$, $r_d = 25\ k$, $R_s = 3.3$ $R_G = 1M\Omega$ calculate Z_i, Z_o, A_V.

common Gate (CG) Amplifier

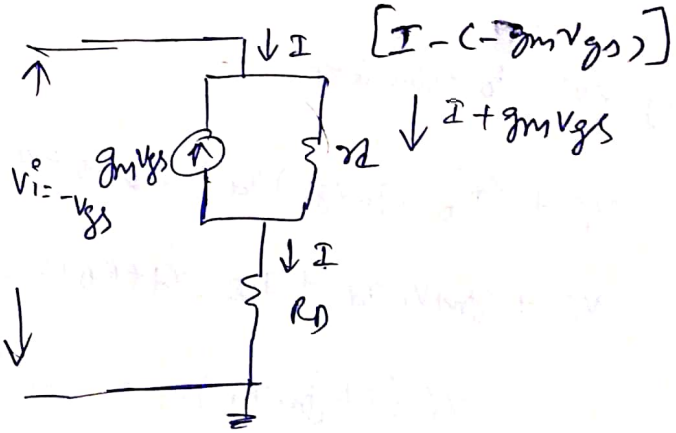




input impedance (Z_i)

$Z_i = R_S \| Z_i'$

$Z_i' = \frac{V_i}{I}$



Apply KVL

$$V_i^o = (I + g_m V_{gs}) r_d + I R_D$$

$$V_i^o = I r_d + g_m V_{gs} r_d + I R_D$$

$V_i = I(r_d + R_D) - g_m V_i r_d \quad \because V_{gs} = -V_i$

$V_i(1 + g_m r_d) = I(r_d + R_D)$

$$\frac{V_i}{I} = \frac{r_d + R_D}{1 + g_m r_d}$$

$$\therefore Z_i = R_S \parallel \frac{r_d + R_D}{1 + g_m r_d}$$

if $r_d >> R_D$, $g_m r_d >> 1$

$$\boxed{Z_i = R_S \parallel \frac{1}{g_m}}$$

o/p impedance (Z_o)

$Z_o = \frac{V_o}{I_o}$ with $V_{gs} = 0$

$$\boxed{Z_o = r_d \parallel R_D}$$

voltage Gain (A_V)

$A_V = \frac{V_o}{V_i} =$

$V_o = -I_D R_D$

Apply KVL to outer loop

$V_i - (I_D - g_m V_{gs}) r_d - I_D R_D = 0$

$V_i = I_D (r_d + R_D) + g_m$

$V_i + g_m V_{gs} r_d$

$V_i (1 - g_m r_d)$

$V_i + (I_D - g_m V_{gs}) r_d + I_D R_D = 0$

$V_i + g_m V_i r_d + I_D (r_d + R_D) = 0$

$V_i (1 + g_m r_d) = -I_D (r_d + R_D)$

$$V_i = -\frac{I_D (r_d + R_D)}{1 + g_m r_d}$$

$$\therefore A_V = \frac{R_D (1 + g_m r_d)}{r_d + R_D}$$

if $r_d >> R_D$, $g_m r_d >> 1$

$$\boxed{A_V = R_D g_m}$$

Metal Oxide Semi-Conductor Filed Effect Transistor (Moss FET (or) Insulated Grate Field Effect Transistor [IGFET]):-

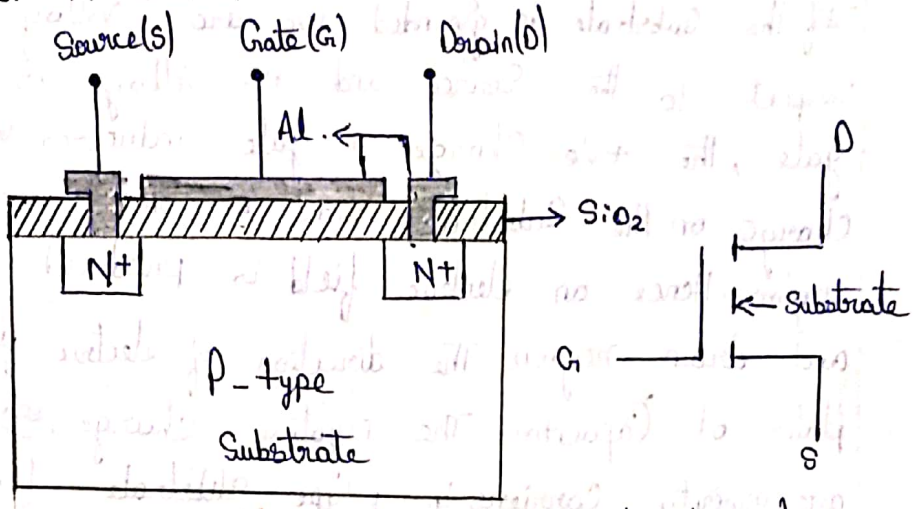
There are two Basic Forms of Moss FET.

(1) Enhancement Moss FET

(2) Depletion MOSSFET.

(1) Enhancement MOSSFET:-

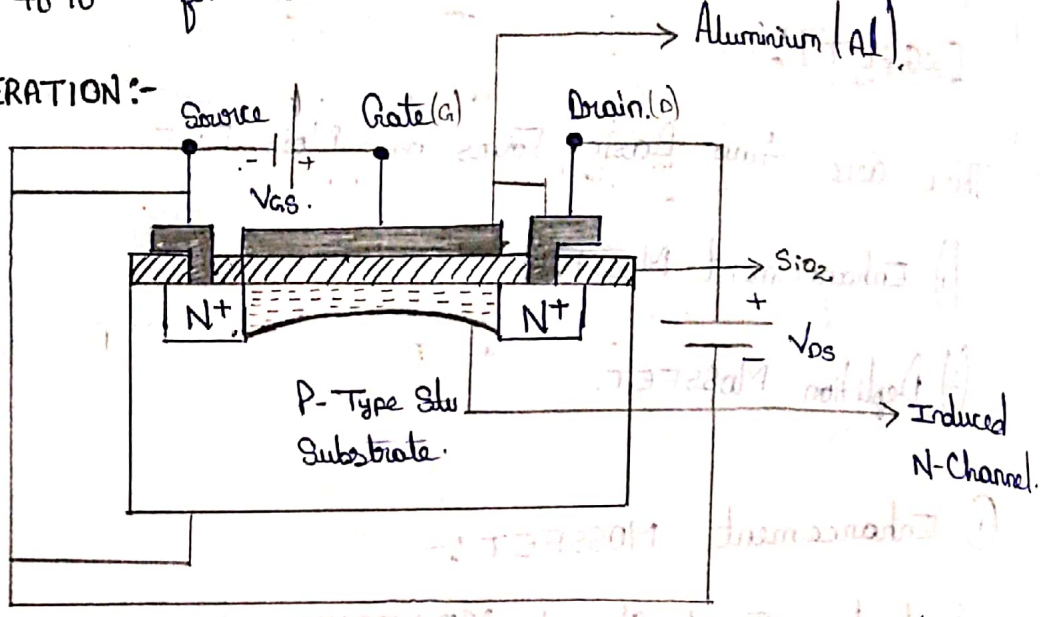
Construction of N-Channel MOSFET:-



N-Channel MOSFET Consist of a lightly doped P-type Substrate into which two highly doped N+ regions are diffused. These N+ Sections which will act as the Source and drain & are seperated by 5-10 micro meter. A Thin layer of Insulating Silicon dioxide [SiO_2] is grown over the Surface of the structure and holes are cut into in the oxide layer allowing Contact with the Source and drain metal Contacts are made into the drain and Source. Then the gate metal area is over laid on the oxide, Covering entire Channel oregion the Contact to the metal over the Channel area is the gate terminal the metal area of the gate in Conjunction with the insulating dielectric oxide layer and the Semi-Conductor Channel form a Parallel plate Capacitor. The insulating layer of SiO_2 is the

region ~~by~~ reason ~~by~~ why this device is called as the insulting gate FET. This layer results in high input resistance 10^{10} to 10^{15} for the MOSFET.

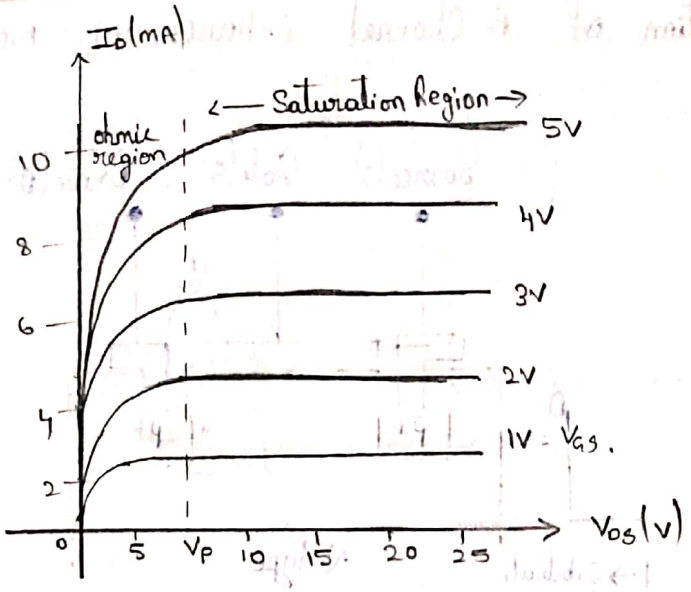
OPERATION:-



If the Substrate is grounded +ve drain voltage is applied with respect to the Source and +ve Voltage is applied at the gate, the +Ve Charge on gate induces ~~on~~ a equal -ve Charge on the Substrate side b/w the Source and the Drain region. Hence an electric field is produced b/w the Source and drain region. The direction of electric field is ⊥er to the plates of Capacitor. The negative Charge ~~(-ve)~~ electrons which are minority Carriers in p-type Substrate forms an inversion layer. as the +ve Voltage on gate increases, the induced negative Charge in the Semi-Conductor increases. Hence the Conductivity increases and the Current flows from Source to drain through the induced Channel.

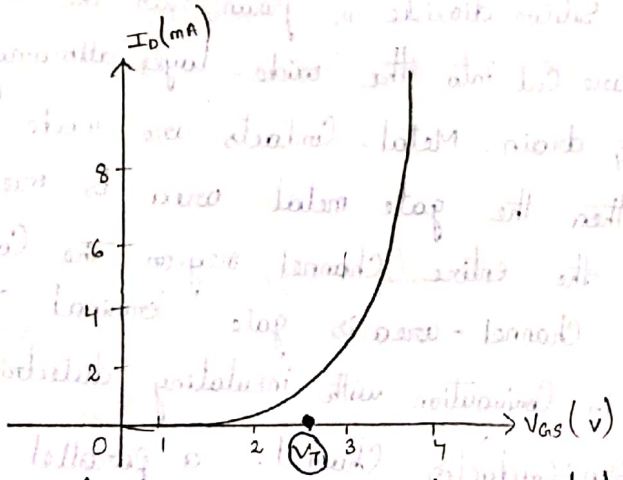
Drain Characteristics :-

Drain Characteristics are drawn b/w Drain Voltage VDS and Drain Current (I_D) where. gate Voltage VGS is Constant



Transfer Characteristics :-

Transfer Characteristics are drawn b/w Gate Voltage V_{GS} and drain Current (I_D) where drain Voltage V_{DS} is Constant.



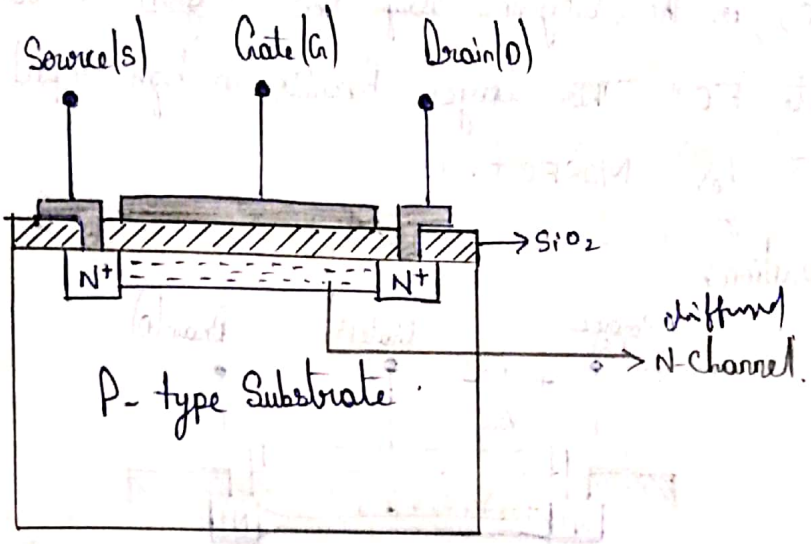
Threshold Voltage (V_T) :- If we increase the magnitude of V_{GS} in the positive direction, I_D increases at a particular value of V_{GS} there is a measurable Current flows b/w Drain and Source. This Value of V_{GS} is Called Threshold Voltage (V_T).

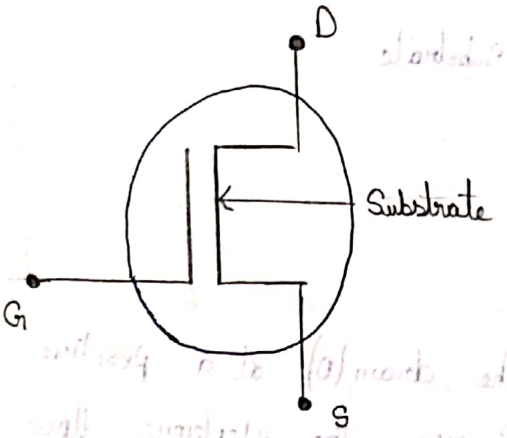
(or)

The minimum gate to Source Voltage required to turn on the MOSFET is Called Threshold Voltage V_T.

Depletion MOSFET :

Construction of Depletion N-Channel MOSFET.

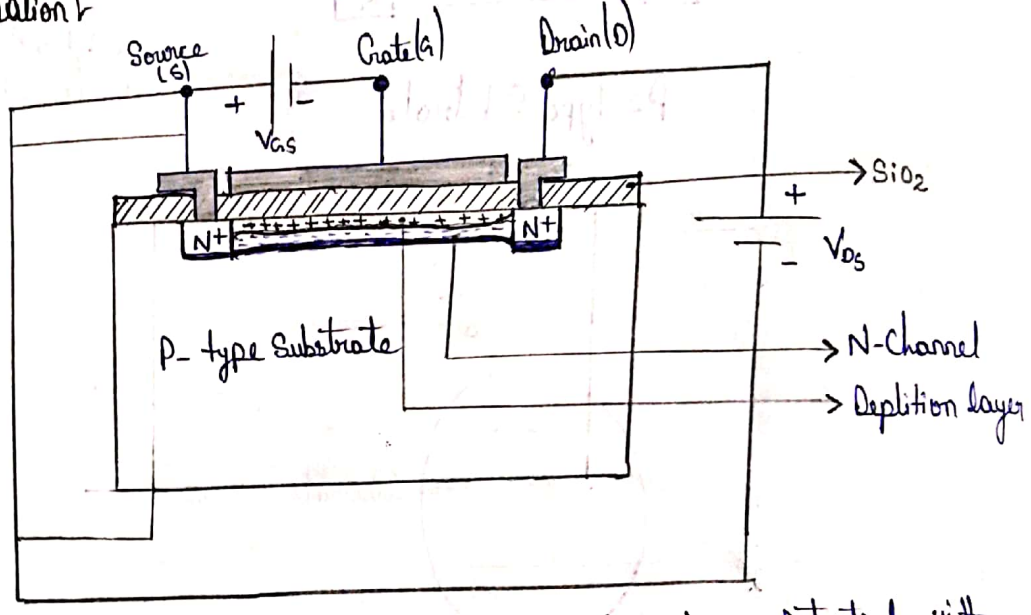




N-Channel MOSFET Consist of a lightly doped P-type Substrate into which two highly doped N^+ regions are diffused these N^+ Sections which will act as the Source and drain are Seperated by 5 to 10 micro meters. Diffuse N-Channel b/w the Source and drain. A Thin layer of insulating SiO_2 is grown over the surface of the Structrure and holes are Cut into the Oxide layer allowing Contact with the Source and drain. Metal Contacts are made into the drain and Source. Then the gate Metal area is over laid on the oxide Covering the entire Channel region. The Contact to the metal over the Channel area is the gate terminal. Metal area of the gate in Conjunction with the

dielectric oxide layer and the Semi-Conductor Channel Form a parallel plate Capacitor. The insulating layer of SiO_2, is the region why this region is Called the insulated Gate FET. This layer Results in high input Resistance 10^{10} to 10^{15} for MOSFET.

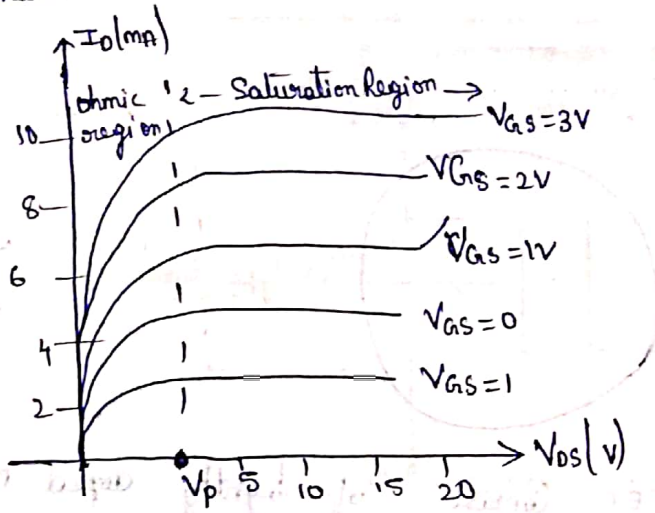
Operation:



When $V_{GS} = 0$ and the drain(D) at a positive potential with respect to the Source, the electrons flow through N-Channel from Source to drain Therefore Conventional Current I_D flows through the Channel from drain to Source. If the gate Voltage is made negative, positive Charge Consisting of holes is induced in the Chanel through SiO_2 of the gate to Channel Capacitor. The introduction of the positive Charge Causes deplition of Mobile electron in the Channel Hence a deplition region is produced in the Channel. The Shape of the deplition region depends on V_{GS} and V_{DS} hence the Channel will be "wedge Shaped". When V_{DS} is increased I_D increases and it becomes Constant at a Value of V_{DS} Called the pinch of Voltage. The Charges make the Chanel less Conductive

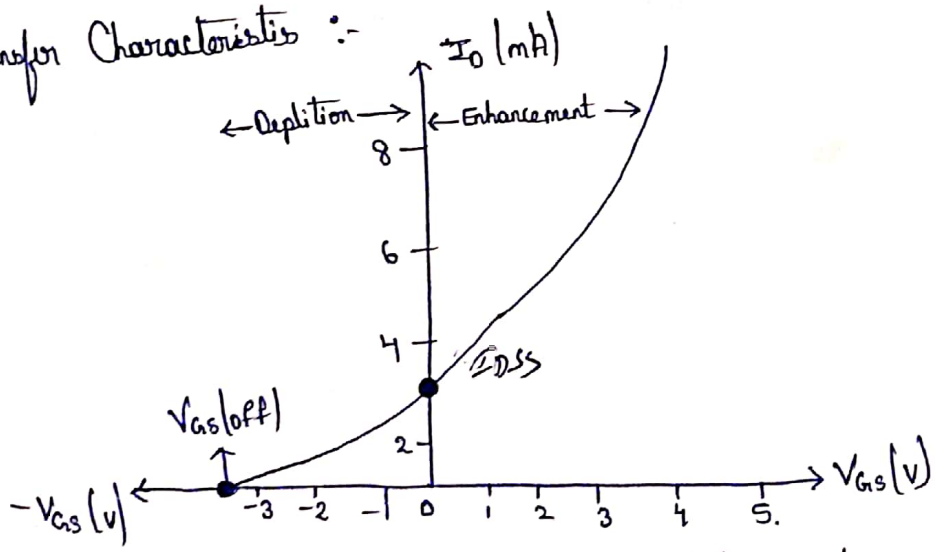
and I_d drops as V_{GS} is made negative. The depletion MOSFET may also be operated in an enhancement mode. It is only necessary to apply a positive gate voltage. So that the negative charge induced into the n-type channel. Hence I_D increases as it can be operated with bipolar input signals it is also called as Dual Mode MOSFET.

Drain Characteristics :-



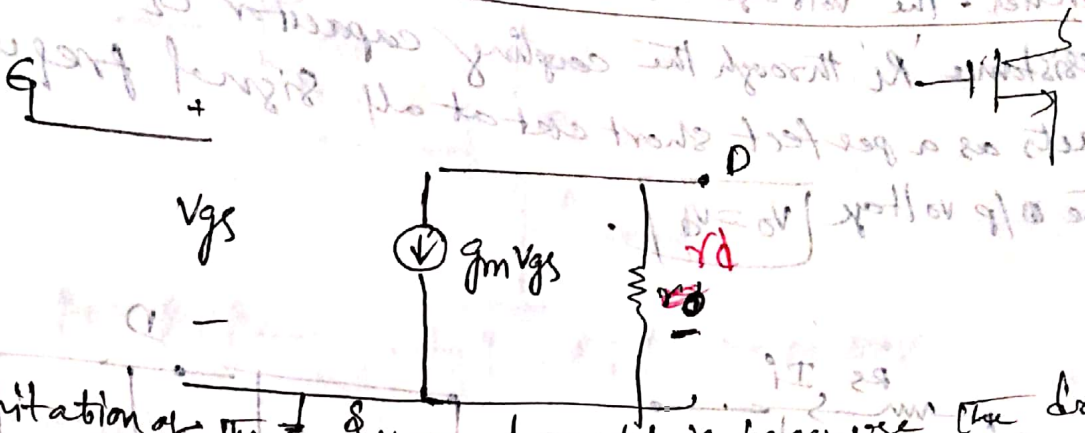
These are drawn b/w drain-Voltage (V_{DS}) & drain-Current (I_D) where gate-Voltage (V_{GS}) is Constant

Transfer Characteristics :-



These are drawn b/w gate Voltage (V_{GS}) & drain-Current (I_D) where drain-Voltage (V_{DS}) is Constant.

MOS small signal equivalent ckt model



The limitation of the small signal model is because the drain current in saturation is assumed to be independent of the drain voltage.

The finite resistance b/w drain & source is given by

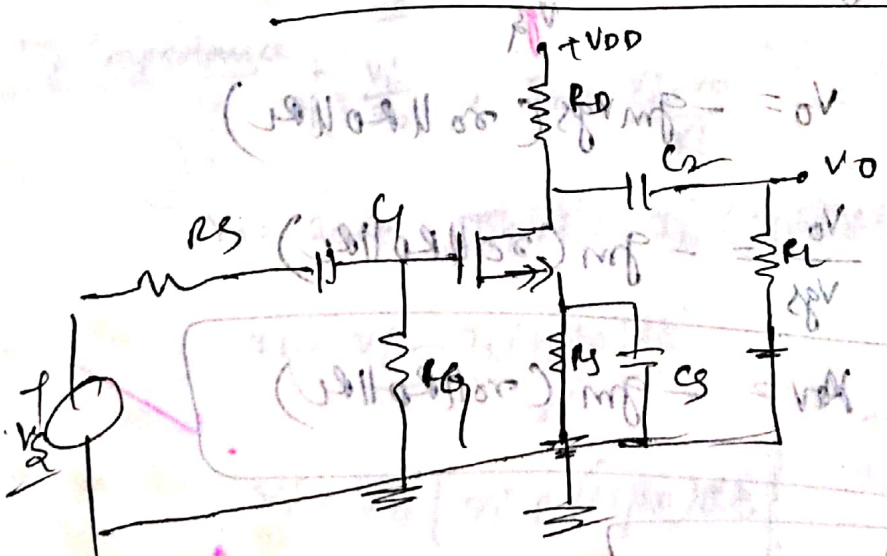
$$r_d = \frac{|V_A|}{I_D}$$

Here $V_A = V_A$ is the MOSFET parameter that is proportional to the MOSFET channel length. Typically, r_d is in the range of 10k to 100k.

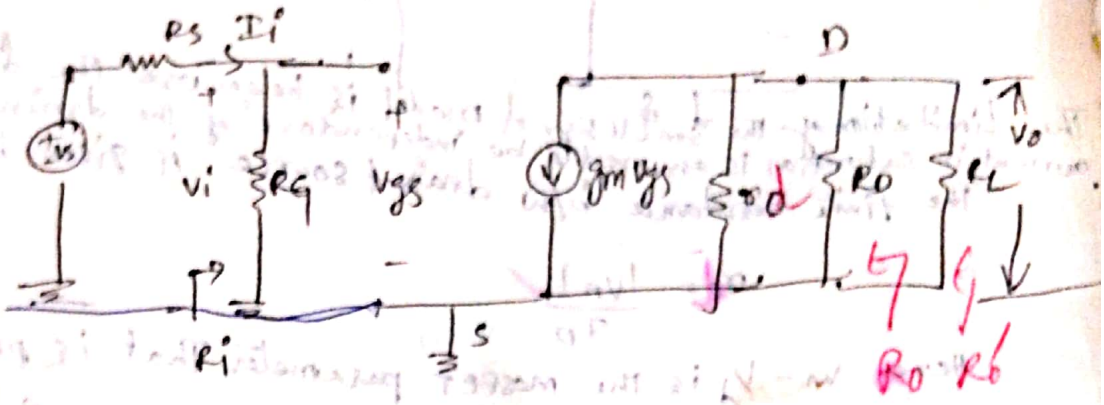
Transconductance of the MOSFET is given by

$$g_m = K_n' \left(\frac{W}{L}\right)(V_{GS} - V_t) \qquad K_n' = \mu_n C_{ox}$$

common-source (CS) amplifier with resistive load



The voltage signal to be amplified v_s with an internal resistance R_s is connected to the gate through a large capacitor 'C_1' called coupling capacitor this acts as a perfect short ckt at all freq consider. The voltage at the drain is coupled to the load resistance 'R_L' through the coupling capacitor 'C_2' and it acts as a perfect short ckt at all signal frequencies The o/p voltage $\boxed{V_o = V_d}$.



D/p resistance $R_i = R_G$

overall voltage gain $A_{VS} = \frac{V_o}{V_s} = \frac{V_o}{V_i'} \times \frac{V_i'}{V_s} = A_V \cdot \frac{V_i'}{V_s}$

$$V_i' = V_s \cdot \frac{R_G}{R_G + R_s}$$

Voltage gain $A_V = \frac{V_o}{V_{gs}}$

$$V_o = -g_m V_{gs} (r_o \| R_D \| R_L)$$

$$\frac{V_o}{V_{gs}} = -g_m (r_o \| R_D \| R_L)$$

$$\boxed{A_V = -g_m (r_o \| R_D \| R_L)}$$

$$\boxed{A_{VS} = \frac{R_G}{R_G + R_s} \cdot A_V}$$

o/p resistance $R_O = (r_d \| R_D)$