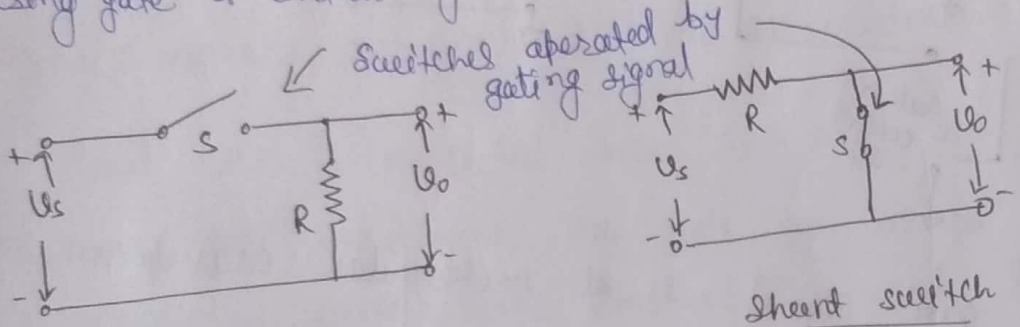
Sampling gates and Realization of Logic gates

* Basic operating principles of sampling gates:

Def"
An ideal sampling gate is transmission ckt in which o/p is exact reproduction of an i/p waveform during selected time interval else zero. The time interval is selected by using gate or control signal. It is refers as linear gate.



In series switch, normally it is open but it will be closed during transmission. whereas in shunt switch it will be open only during transmission.

In practical use, switch will be replaced by Semiconductor diode. Ideally, switch has zero resistance when closed and infinite resistance when open. But in practice we can't achieve this. So, resistance of (R_{sw}) has range from several hundred to several thousand ohms. It is required $R >> R_{sw}$.

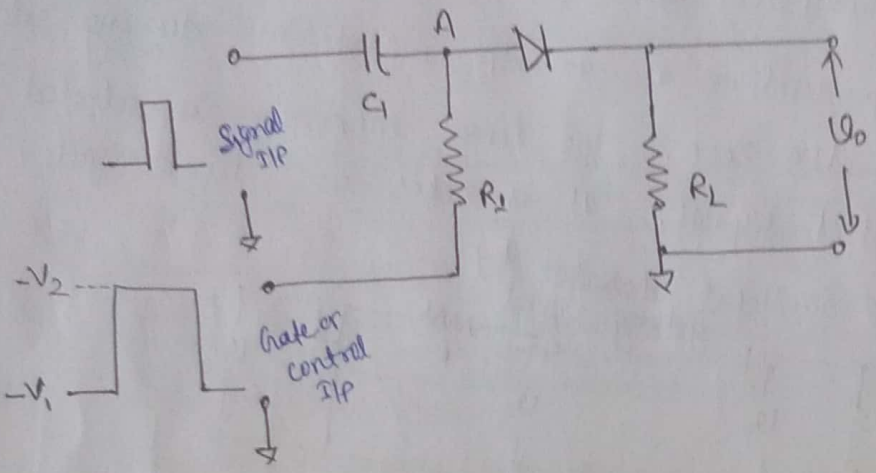
During transmission, i/p & o/p will be separated by large resistance R. If there is stray capacitance, shunting the o/p then it is not possible to transmit fast wave without deterioration.

→ Difference b/w series & shunt switch

(i) In series switch, stray capacitance will permit some signal transmission even switch is open.

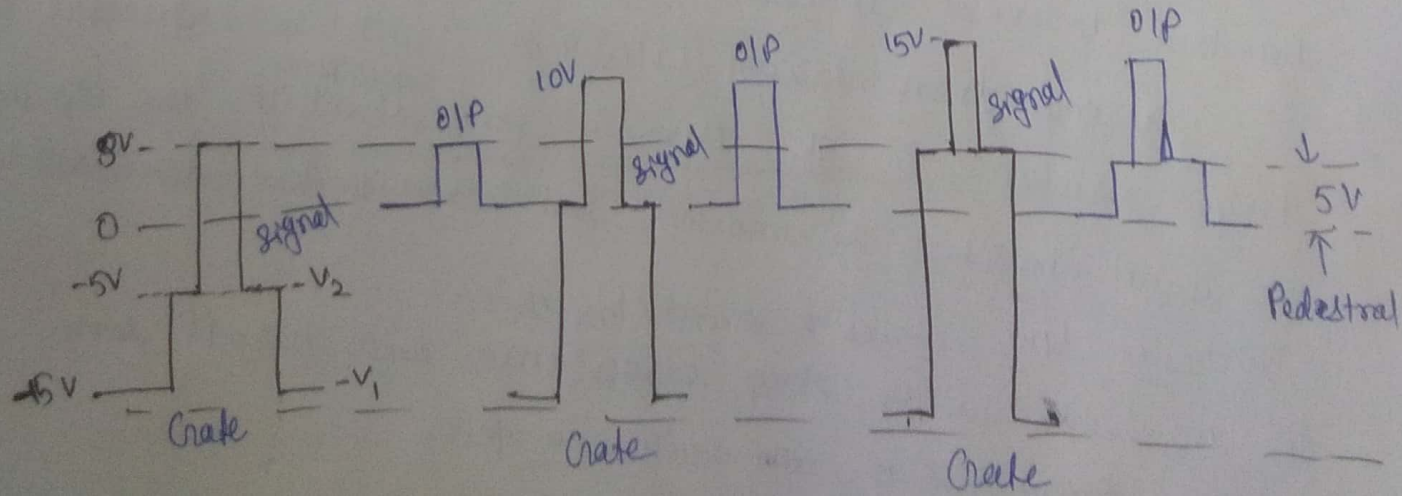
(ii) Signal is transmitted through the switch, so some attenuation and distortion will be produced due to nonlinearity.

* Unidirectional sampling gate



The gate signal is a rectangular waveform, which makes transition b/w $-V_1$ & $-V_2$. It is also known as control pulse, a selector pulse or an enabling pulse.

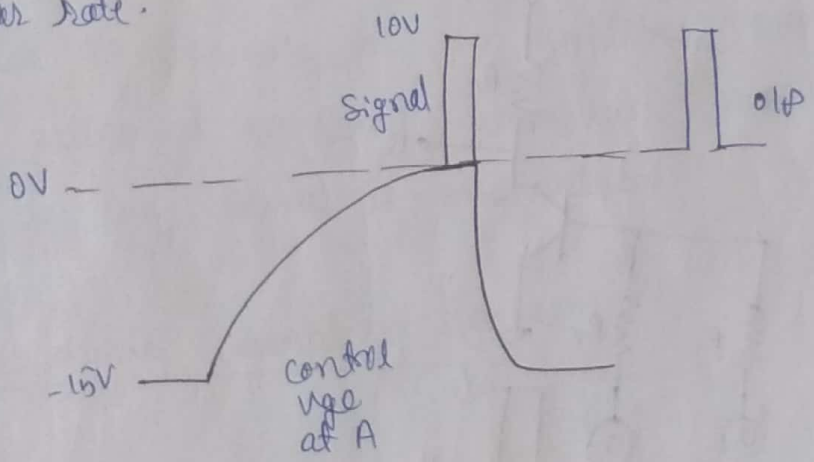
When gate vge is at $-V_1$, the diode is heavily reverse biased & there will be no o/p unless peak amplitude of i/p signal is larger than reverse biasing vge. The duty cycle of I/p signal is very less. When gate vge rises to $-V_2$ then signal i/p pulse will be transmitted to o/p.



The i/p signal is of 10V. For first case 5V o/p pulse appears. If baseline of i/p signal has noise then it is not transmitted.

But if level $-V_2$ may be adjusted so that only part of signal above noise threshold appears at the o/p. Then circuit is known as threshold gate. When $-V_2=0$, then entire i/p pulse is transmitted. When $-V_2$ is positive then signal appears superimposed on a 5V pedestal.

But R_1C_1 is neglected here. This now act as integrating n/w for gate waveform. So, gate vge at pt A will rise exponentially with time constant R_1C_1 and fall with similar rate.



Adv. of gate :

(i) It is extremely simple

(ii) There is little delay through the gate since i/p is coupled directly to o/p through C_1 & diode.

(iii) Gate draws no current in stand by condition.

Disadv:

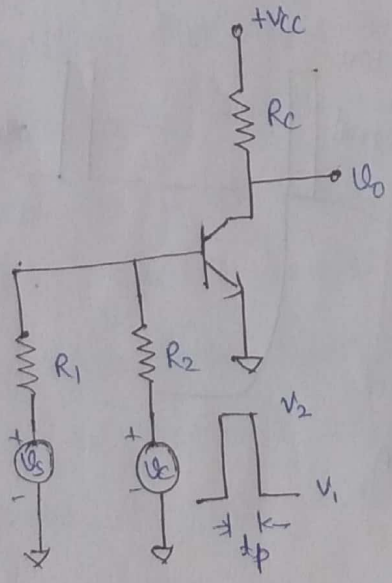
(i) There will be interaction b/w the signal source and control vge source

(ii) The gate has limited use because of slow rise of control vge at diode.

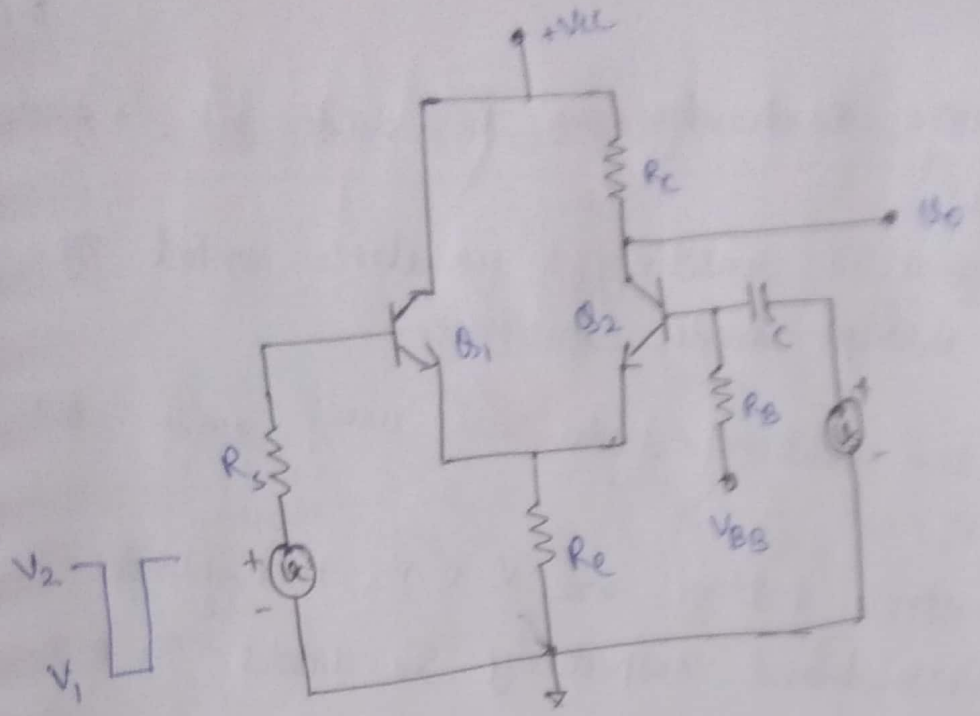
The rise time of control vge at pt. A may be improved by reducing R_1 but it will increase coupling b/w I/P signal & control signal. It can be done by reducing C_1 but other issue will rise.

So, rise time issue can be eliminated by replacing C_1 by resistor R_2. But signal will be attenuated. Eg. $R_1 = R_2$ then amplification will be half & d.c. coupling of signal will be required.

* Bidirectional sampling gates by using Transistor

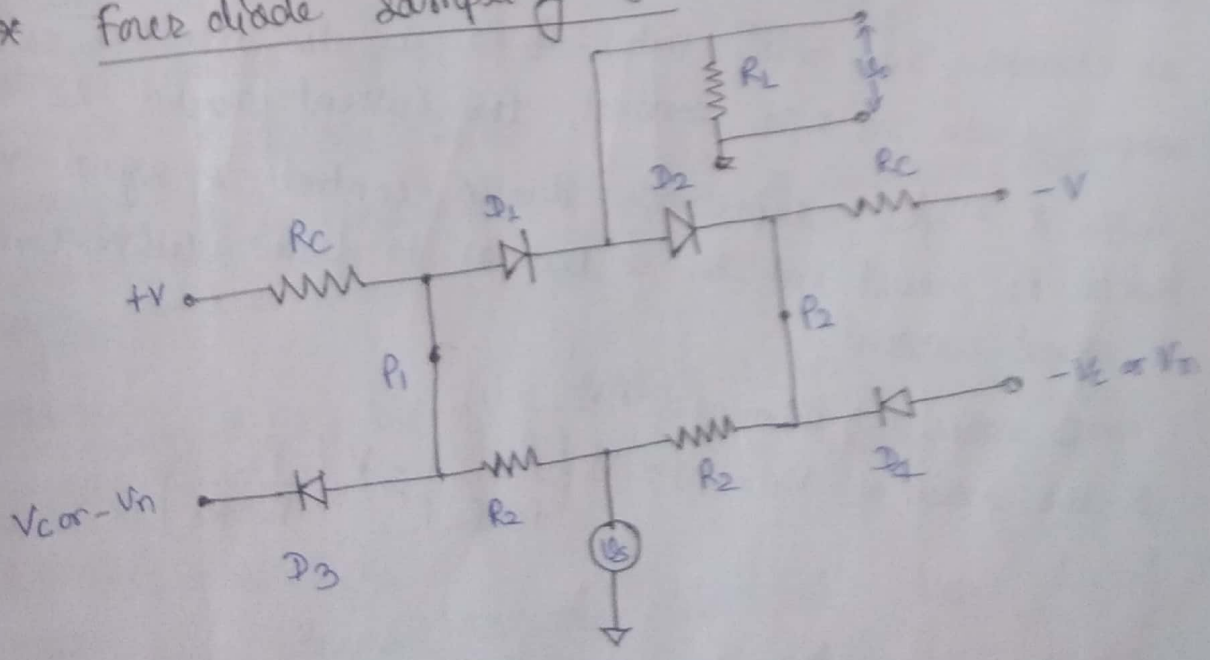


It is linear bidirectional sampling gate. The signal vge Vs(t) and control voltage Vc(t) are applied through resistors R_1 & R_2 to base of transistor. The gate vge has V_1 & V_2 levels in pulse. when gate vge is at lower level V_1, the transistor is biased in cut-off. At upper level V_2, the transistor will enter in to active region. So, transistor will sample the signal vge & amplified will appear at O/P.



Here separate bases are available for signal & gating ckt. when $V_1(t)$ is at upper level, the current through R_e is large enough to raise the emitter voltage to the point to make Q_2 in cut-off. At level V_1, Q_1 is in cut-off & Q_2 is free to operate as an amplifier stage. During this interval gating & o/p signal uncoupled from each other. Loading to the signal is also reduced.

* Four diode sampling gate:



Due to following disadvantages of two diode gate, 4 diode gate is required:

(i) Low gain, (ii) sensitivity to unbalance control vge.
(iii) Leakage through diode capacitance.

So, here two additional diodes are used with fixed voltage +V & -V.

when control voltages are V_c & $-V_c$, then diodes D_3 and D_4 are reverse biased respectively. The diodes D_1 & D_2 are conducting because of +V & -V. The signal source is coupled to load through R_2 and conducting diodes. The control voltages are disconnected and an imbalance in control signals can't result in pedestral at the o/p.

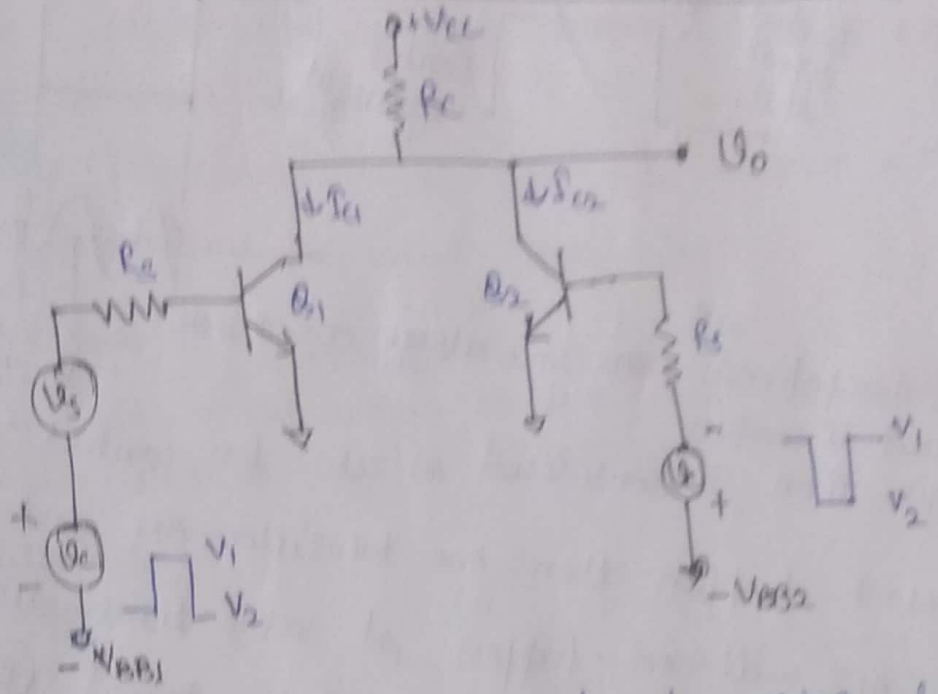
when control voltages are V_n and $-V_n$, then D_1 & D_2 clamped to these levels, so diodes D_1 & D_2 are reverse-biased. Hence o/p is zero.

The value of R_2 to be large in comparision to the diode-conducting resistance, so that diode may be effectives as clamps. The min^m value of R_2 is also limited, so that when diodes D_3 & D_4 conduct, the current should be V_n/R_2 & $2V_s/R_2$ respectively due to control & signal vge. Hence R_2 must not be so low as to draw excessive control or signal current.

The value of $V_c(min) = AV_s$.

& the value of $V_n(min) = V_s\left(\frac{R_c}{R_c+R_2}\right) - V\left(\frac{R_2}{R_2+R_c}\right)$.

* Reduction of Pedestal in a gate circuit:



The pedestal can be removed by using symmetrical arrangement. Here source signal & control signal both are given in series to transistor Q_1 whereas transistor Q_2 is given only control signal, which is opposite of Q_1.

Case-I

when $V_c(Q_1) = V_1$ (+ve) & $V_c(Q_2) = V_2$ (-ve).

then Q_1 will be ON & Q_2 will be OFF. So, o/p voltage without source signal i.e $V_s = 0$ is given as

$$V_o = V_{cc} - I_{c_1} R_c$$

when V_s is considered then it is superimposed on this with phase shift of 180°.

Case-II

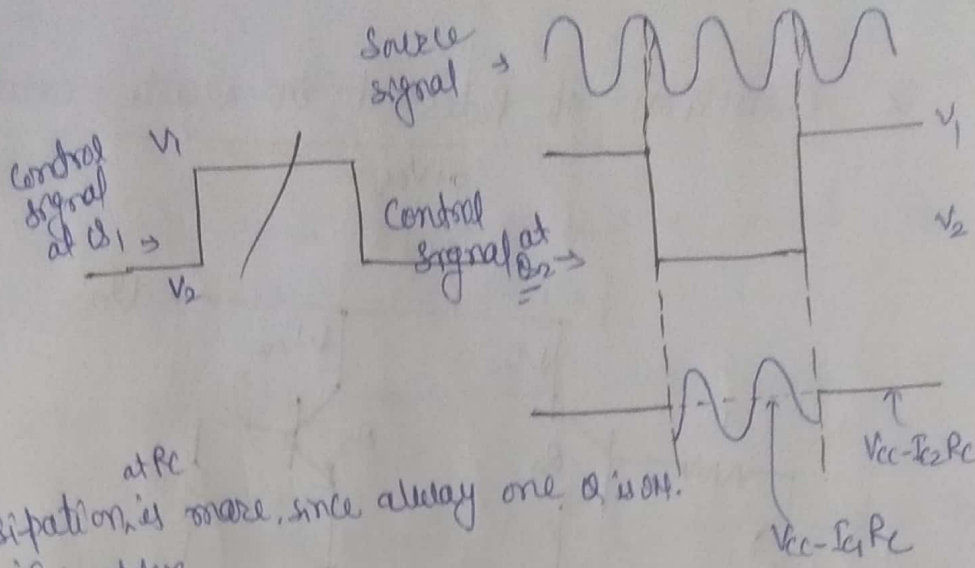
when $V_c(Q_1) = V_2$ (-ve) & $V_c(Q_2) = V_1$ (+ve)

then Q_1 is off & Q_2 is ON. So, o/p voltage is given as

$$V_o = V_{cc} - I_{c_2} R_c.$$

If both transistors are identical then $I_{c_1} = I_{c_2}$.

So, o/p vge will be same in both cases when $V_s = 0$.

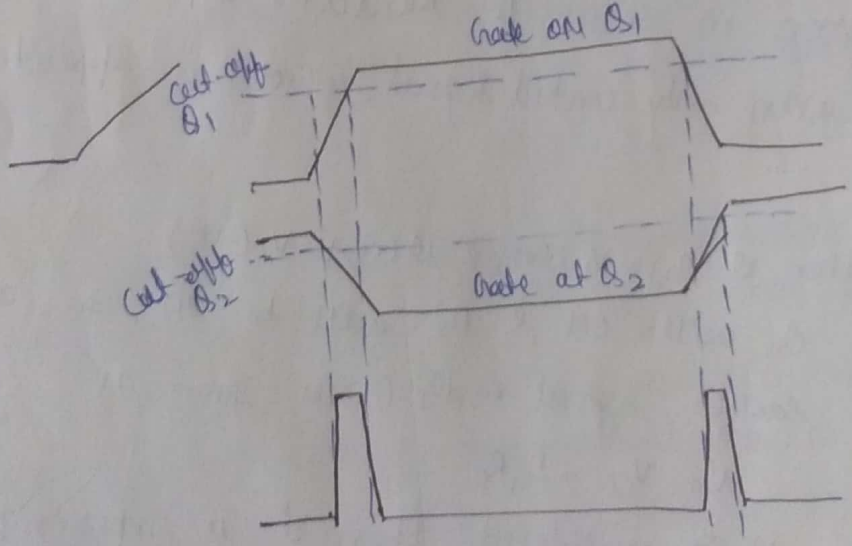


Disadv: at R_C

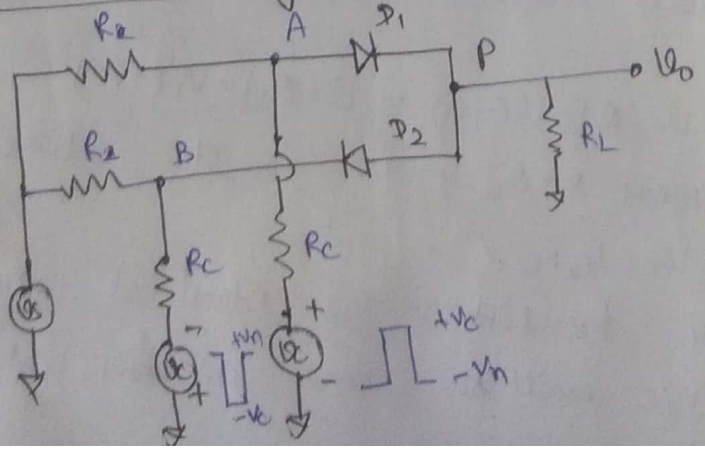
(i) Power dissipation is more, since always one Q_1 is ON.

(ii) Circuit is complex

(iii) Here rise time is considered as zero for control signal. If it doesn't happen then one transistor ON and another transistor OFF will not happen at same time due to finite rise time. During this period V_{cc} will appear as spikes at O/P.



* Bidirectional diode sampling gate:



Case-I

$D_1 \to +V_c$, $D_2 \to -V_c$: $V_o = 0$ if $V_s = 0$; $V_o = V_s$ if $V_s \neq 0$

Case-II

$D_1 \to -V_n$, $D_2 \to +V_n$: Both diodes OFF, so $V_o = 0$

$V_{e\,min}$ → min^m the V_{ge} at D_1 that keep both diodes FB

$V_{n\,min}$ → min^m the V_{ge} at D_2 that keep both diode RB.

* Logic gates:

It is fundamental building blocks of digital system, which has ability to make decision.

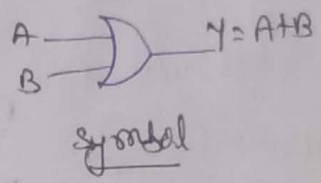
The interconnection of gates to perform a variety of logical operations is called logic design.

* OR Gate : (IC 7432) 2→I/P

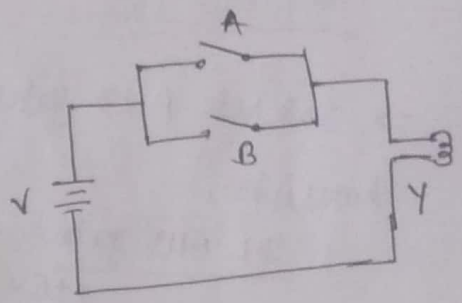
It is device or ckt, whose O/P is 1 even one of its I/P is 1.
It is also called as any or all gate.

Truth table

I/P		O/P
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

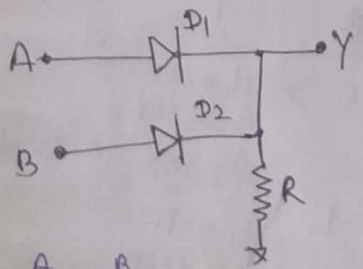


symbol



→ The discrete OR gates may be realized by using diodes or transistors.

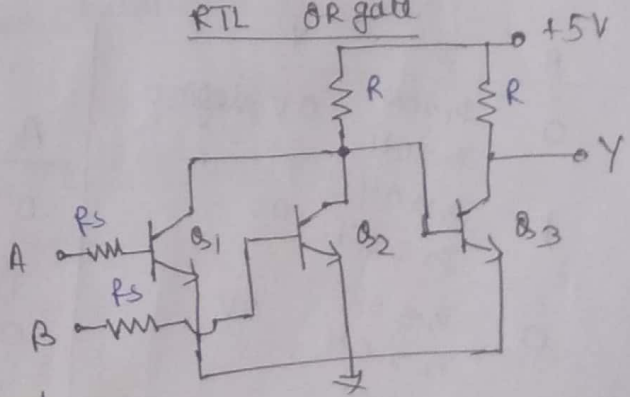
DL OR gate



A	B		Y
0	0	D_1→OFF & D_2→OFF	0V
0	1	D_1→OFF, D_2→ON	+5V
1	0	D_1→ON, D_2→OFF	+5V
1	1	D_1→ON, D_2→ON	+5V

0 → 0V
1 → +5V

RTL OR gate



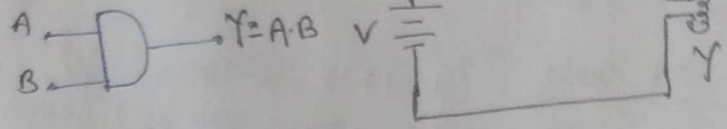
A	B	I	Y
0	0	Q_1→OFF, Q_2→OFF, Q_3→ON	+0.3V → logic 0
0	1	Q_1→OFF, Q_2→ON, Q_3→OFF	+5V → logic 1
1	0	Q_1→ON, Q_2→OFF, Q_3→OFF	+5V → logic 1
1	1	Q_1→ON, Q_2→ON, Q_3→OFF	+5V → logic 1.

* AND gate (IC 7408 → 2 I/P, IC 7411 → 3 I/P & IC 7421 → 4 I/P)

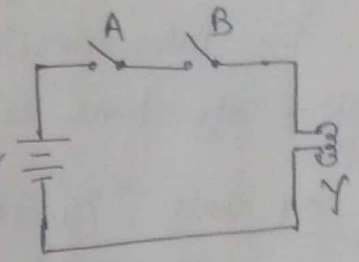
It is device or circuit whose O/P is 1, if and only if all its I/Ps are 1. So it is called as all or nothing gate.

Truth table

I/P		O/P
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

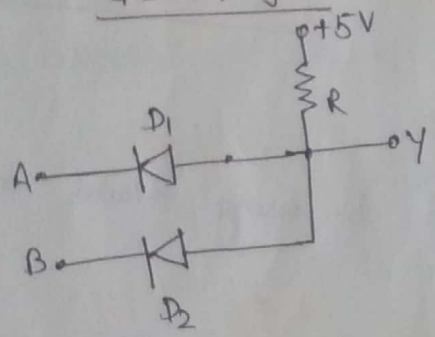


Symbol



→ Discrete AND gates may be realized by using diodes or transistor.

DL AND gate

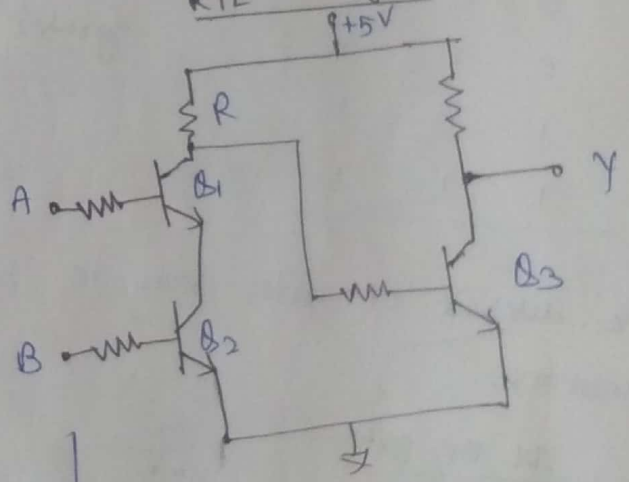


A	B	D	Y
0	0	D_1 → ON, D_2 → ON	0V → logic 0
0	1	D_1 → ON, D_2 → OFF	0V
1	0	D_1 → OFF, D_2 → ON	0V
1	1	D_1 → OFF, D_2 → OFF	5V → logic 1

0 → 0V
1 → 5V

* logic 0 → all supply voltage drop across R
* logic 1 → No supply drop across R

RTL AND gate



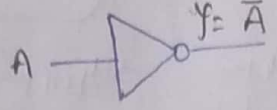
A	B	T	Y
0	0	Q_1 → OFF, Q_2 → OFF, Q_3 → ON	0.3V → logic 0
0	1	Q_1 → OFF, Q_2 → OFF, Q_3 → ON	0.3V
1	0	Q_1 → OFF, Q_2 → OFF, Q_3 → ON	0.3V
1	1	Q_1 → ON, Q_2 → ON, Q_3 → OFF	5V logic 1

* NOT gate (Inverter) (IC 7404):

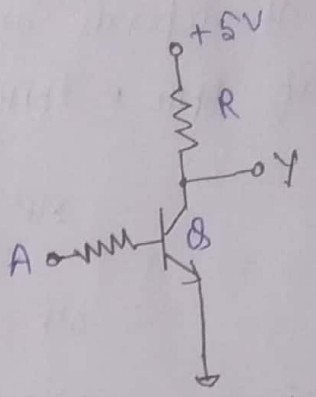
It is device (ckt), whose O/P is always the complement of its i/p.

Truth table

I/P A	O/P Y
0	1
1	0



Symbol



RTL NOT gate

I/P A	T	Y
0	Q-OFF	V_{cc} = +5V (logic 1)
1	Q-ON	$V_{cc} - I_c R = V_{ce(sat)} \approx 0.3$ V (logic 0)

* Logic families:

A group of ICs with same logic levels & supply voltage perform various logic fns with the help of unipolar & bipolar technologies & they are fabricated.

Bipolar LF:

1. Saturated: RTL, DCTL, I^2L, DTL, HTL, TTL
2. Unsaturated: Schottky TTL, ECL

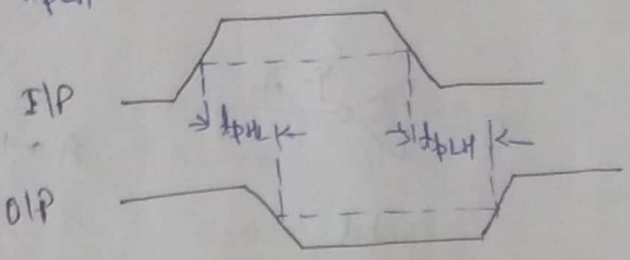
Unipolar LF:

1. PMOS
2. NMOS
3. CMOS

* Characteristics of Digital ICs :

(i) Speed of operation :

It depends on propagation delay. It is taken as average of t_{pHL} & t_{pLH}.



(ii) Power dissipation :

It is amount of power dissipated in an IC. which is given as $V_{cc} \times I_{cc}$. where I_{cc} is avg. value of $I_{cc}(0)$ & $I_{cc}(1)$.

(iii) Figure of merit :

It is product of speed & power.

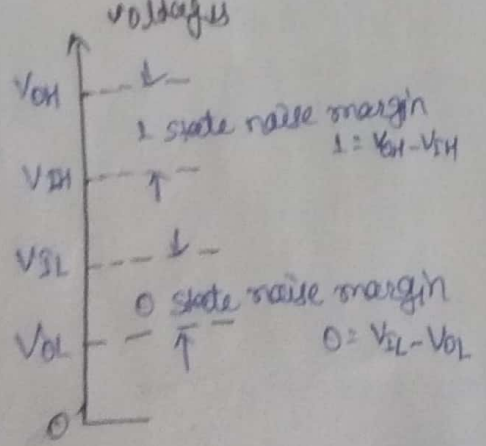
F.M = propagation delay (ns) x power (mW)
(pJ)

Its low product is desirable.

(iv) Fan-out :

It is number of similar gates which can be driven by a gate. High fan out is advantageous.

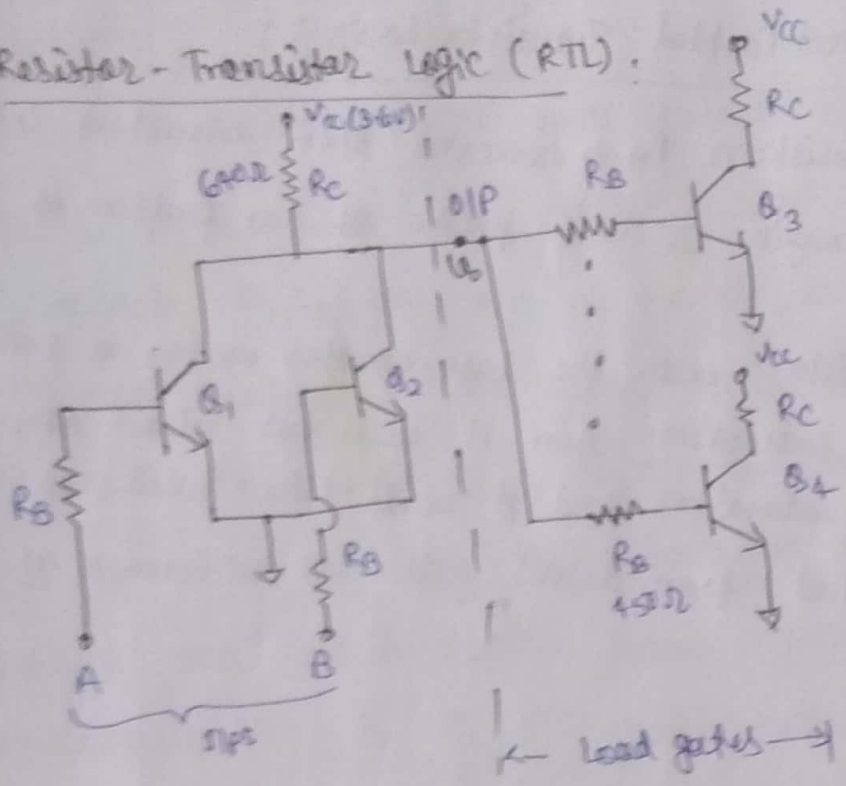
(v) Noise immunity :



The circuit's ability to tolerate noise signal is called as noise immunity. Its quantitative measure is called as noise margin.

→ DC noise margin
→ AC noise margin
It is greater than dc noise margin.

* Resistor - Transistor Logic (RTL):



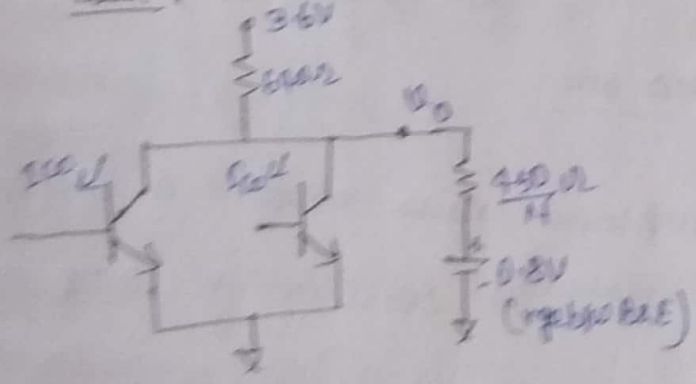
RTL NOR gate

It is earliest logic family, but now it is not used because of its simplicity. It consist of 2 I/Ps NOR gate. which is basing of similar gates.

operation:

When both A & B has low level voltage as i/p than transistors B_1 & B_2 are off. So, O/P is maximum slightly less than Vcc. This high O/P will drive any transistor into saturation. Hence o/p will be $V_{out} = 0.2V$.

Load:



$$I_B = \frac{3.6 - 0.8}{640 + \frac{450}{N}} = \frac{2.8}{640N + 450}$$

$$I_{C,sat} = \frac{3.6 - 0.2}{640} = 5.31\,mA$$

$h_{fe} \cdot I_B \geq I_{C,sat}$.

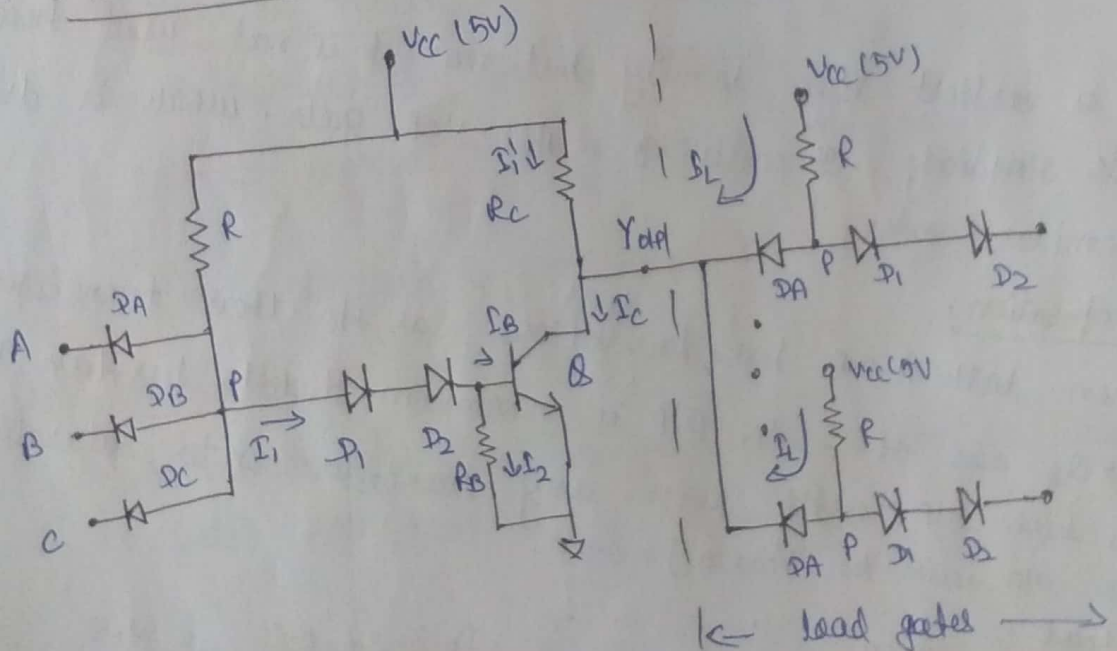
⇒ RTL has low noise margin, poor fan out capabilities, low speed & high power dissipation.

* DCTL : (Direct Coupled Transistor Logic) :

In RTL, base resistance R_B is removed then circuit is called as DCTL. Noise margin is very poor. It has problem of current hogging.

The transistor with the base-emitter voltage of 0.7V, when its enter into saturation then it will not allow other transistors to enter into saturation and it will take whole of the current supplied from driver gate. It is known as current hogging.

* DTL (Diode - Transistor Logic) :



3 I/Ps DTL NAND gate

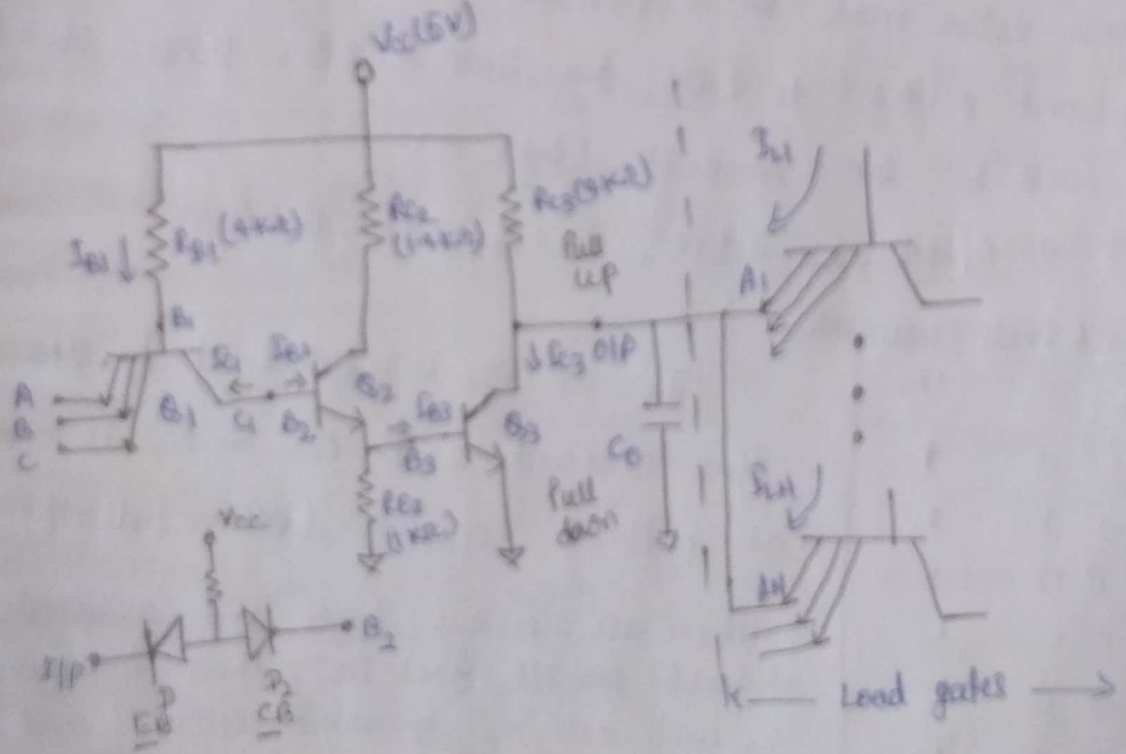
It has more fan-out & improved noise margins in compare to RTL. But its speed is less. which is overcome in TTL.

operation:

The I/p diodes in DTL will conduct through the resistor R. If I/P is in the low state while in high state, diode will not conduct. So, if any one of the I/P is low then that diode will conduct. The voltage Vp at I/P will keep transistor Q_1 in to cut-off. So, O/P of transistor is Vcc.

But if all I/ps are high then transistor will enter in to Saturation and o/p is low i.e Vcesat. Logic 1 & logic 0 here corresponding to Vcc & Vcesat) respectively.

* TTL (Transistor - Transistor Logic):



It is most successful bipolar logic, which was evolved in 1960 It perform logic functions and it has high drive capability.

The 3 I/P TTL NAND gate is driving N similar gates. It has multiple emitter transistor Q_1.

Case- I

When any I/P or all I/Ps are low then transistor Q_1 will work in forward active mode. The voltage at base B_1 will be (0.2V to 0.7) 0.9V. [EB→FB & BC→RB]
(I/P, diode FB.)

So, there is no sufficient voltage to turn Q_2 ON. Hence Q_3 is also OFF. Finally O/P voltage will be equal to V_{cc}. (logic 1)
i.e. Q_1 → Forward active, Q_2 & Q_3 → OFF & $V_o = V_{cc}$.

Case II

When all I/Ps are high then transistor Q_1 will act as reverse active mode. i.e (EB→RB & BC→FB). So, there is sufficient voltage to ON transistor Q_2 & Q_3. Hence O/P vge V_o will be low i.e. 0.3V. (logic 0)

→ Q_1 → Reverse active, Q_2 & Q_3 → ON, $V_o = 0.3V$.

Truth table (NAND gate)

A	B	C	V_o
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

The O/P vge is pulled up by the time constant. $\tau = R_3 \cdot C_0$. So, R_3 is known as pull-up resistor. (passive pull-up)

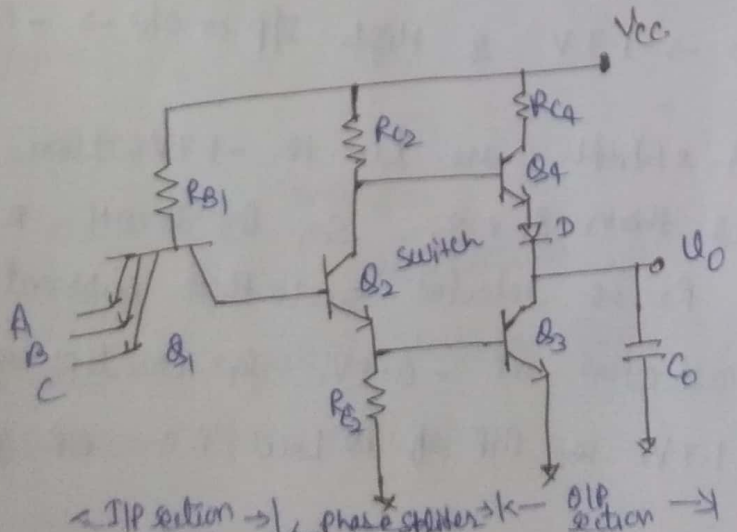
→ When all I/Ps are high and suddenly at least one I/P goes low then transistor Q_1 will act as forward active and it has more collector current. It will remove base storage charge of transistors Q_2 & Q_3, so, speed is more in TTL.

when O/P is high then leakage current drives load gates, which is very small in comparision to the sinking current so, TTL is known as current sink logic.

→ It is required that time constant $R_{C3} \cdot C_0$ should be less. which is possible by reducing R_{C3}. when Q_3 is off then capacitor C_0 will charge through resistance R_{C3} due to V_{CC}. while R_{C3} will be reduced then flow of more collector current will occur. So, Power dissipation will be more.

when Q_3 is ON then collector current will be more, so, saturation current will increase. Hence R_{C3} should have large value.

Finally R_{C3}, we can't change. So, it is replaced by transistors. Due to this charging of capacitor will be fast without more power dissipation. which is known as active-pull up or totem-pole O/P.

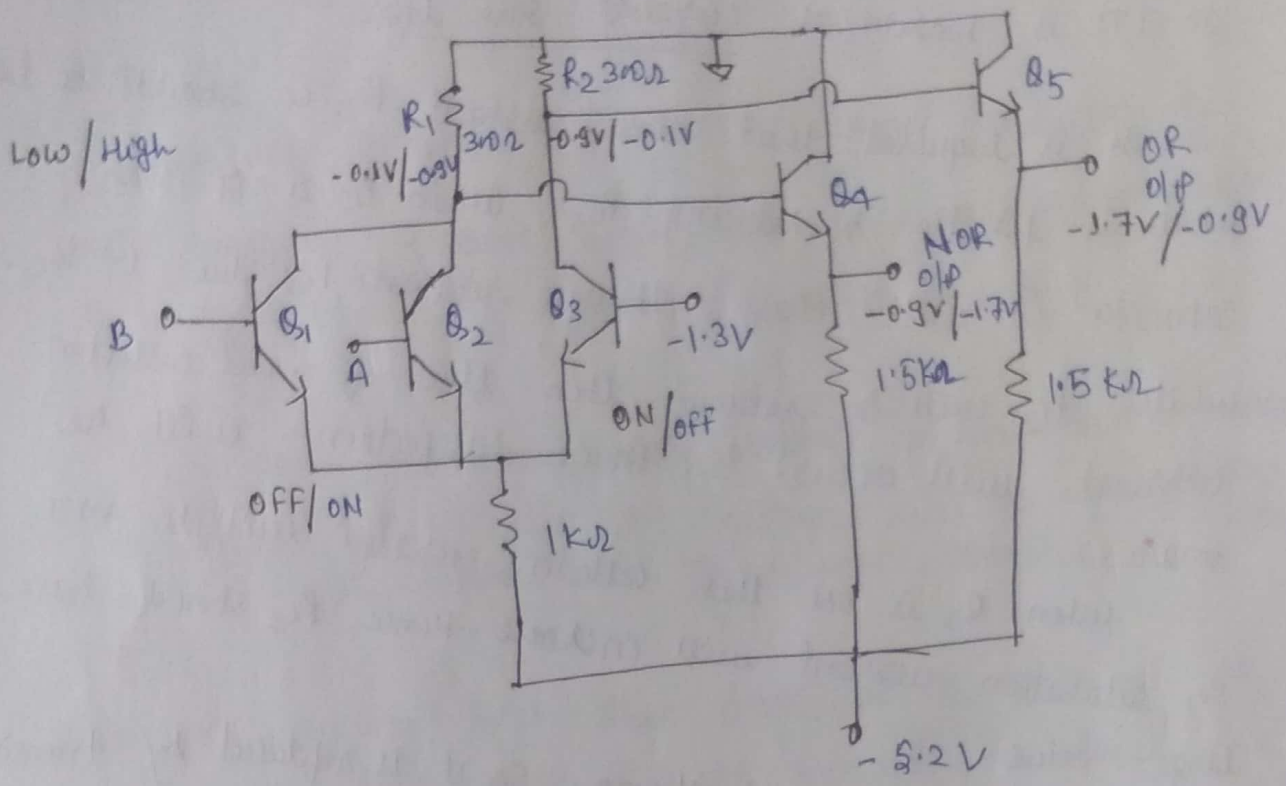


TTL gate with Totem-pole O/P drives

* when Q_1 is saturative
→ then $Q_2 \rightarrow$ ON
then $Q_3 \rightarrow$ ON but Q_4 OFF
→ when $Q_2 \rightarrow$ OFF
then $Q_3 \rightarrow$ OFF but $Q_4 \rightarrow$ ON

* when Q_2 OFF then
$V_0 = V_{CC} - I_{C4} R_{C4} - V_{CE(sat)}(Q_3)$
$\rightarrow 0.7 (V_\gamma)$

* ECL (Emitter coupled logic) or Current mode logic (CML) or Current steering logic (CSL):



2 I/Ps ECL OR/NOR gate:

→ Transistor Q_2 & Q_3 are differential amplifier. Q_1 || Q_2.

Q_4 & Q_5 are emitter followers.

→ Low I/P or O/P → -1.7 V & High I/P or O/P → -0.9V.

→ when the I/P A & B both are low i.e. -1.7V, then Q_3 is more forward bias than Q_1 & Q_2. So, Q_3 is ON & Q_1, Q_2 is OFF. The value of R_2 is selected such that current flowing through Q_3 puts collector at -0.9V. So Emitter of Q_5 is -0.9 - 0.8 = ~~-1.7~~ -1.7V. i.e. O/P of is Low i.e. OR gate.

The base current of Q_4 through R_1 is small. So that collectors of Q_1 & Q_2 at about -0.1V. so emitter of Q_4 is at -0.1 - 0.8 = -0.9V. i.e. NOR O/P is High.

→ when any or both I/Ps are high then corresponding transistor will be ON and Q_3 will be OFF due to less forward bias. Collectors of Q_1 & Q_2 are at -0.9V. So, NOR O/P is -0.9V - 0.8V = -1.7 V i.e. logic 0. Very small current flow through R_2, so, OR O/P is -0.1 - 0.8 = -0.9V i.e. logic 1.

→ It provides common mode rejection. O/P is taken at emitter terminal so O/P impedance is low. It has large fan-out.

→ It is fastest due to following reasons :-

(i) It is non-saturated logic. storage time delays are eliminated. So, speed of operation is fast.

(ii) currents are high and O/P impedance is low. So, stray capacitance charge & discharge quickly.

(iii) The limited voltage swing.

→ It operates on principle of current switching.

Disadv:

(i) High cost
(ii) Low noise margin
(iii) High power dissipation
(iv) Due to negative supply Vee, it is difficult to use.
(v) Problem of cooling.

* Comparisions:

Parameters	RTL	DCTL	DTL	TTL	ECL
Components					
Noise-margin	Poor	Poor	High	Medium	Low
Fan-out	Low(4)	Low(4)	Medium(8)	High(10)	Very High(25
Power-dissipation (mW)	30	30	8.12	10	40-55 2 0.15
Delay (nsec)	12	10	30	10	.100 40
Figure of merit	144	1300	300	100	