

## → Phase-locked loops

### → Introduction:-

The phase-locked loop (PLL) is an important building block of linear systems.

→ The electronic phase-locked loop (PLL) came in the 1930s when it was used for radar synchronisation and communication applications.

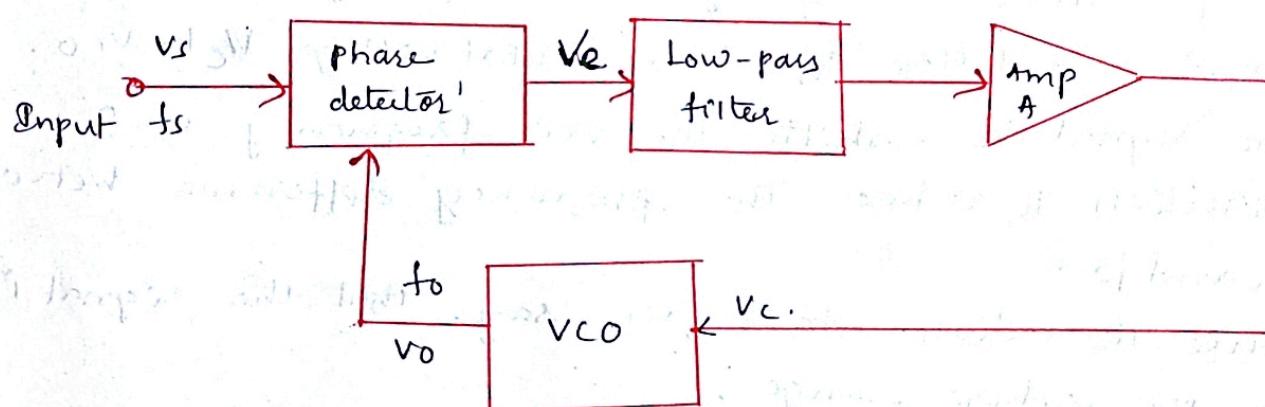
→ The high cost of realising PLL in discrete form limited its use earlier.

→ Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs.

→ This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc.

### → Basic Principles:-

→ The basic block schematic of the PLL is shown in fig.



→ This feedback system consists of:

1. Phase detector / comparator
2. A low pass filter
3. An error amplifier
4. A voltage controlled oscillator.

→ The VCO is a free running multivibrator and operates at a set frequency  $f_0$  called free running frequency.

$$f_0 = \frac{2(V_{cc} - V_c)}{C \cdot R_T \cdot V_{cc}}$$

- This frequency is determined by an external timing capacitor and an external resistor.
- It can also be shifted to either side by applying a dc control voltage  $V_c$  to an appropriate terminal of the LC.
- The frequency deviation is directly proportional to the dc control voltage and hence it is called a voltage controlled oscillator or VCO.
- If an input signal  $V_s$  of frequency  $f_s$  is applied to the PTL, the phase detector compares the phase and frequency of the incoming signal to that of the output  $V_o$  of the VCO.
- If the two signals differ in frequency and/or phase, an error voltage  $V_e$  is generated.
- The phase detector is basically a multiplier and produces the sum ( $f_s + f_o$ ) and difference ( $f_s - f_o$ ) components at its output.
- The high frequency component ( $f_s + f_o$ ) is removed by the Low pass filter and the difference frequency component is amplified and then applied as control voltage  $V_c$  to VCO.
- The signal  $V_c$  shifts the VCO frequency in a direction to reduce the frequency difference between  $f_s$  and  $f_o$ .
- Once the action starts, we say that the signal is in the capture range.
- The VCO continues to change the frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. The output frequency  $f_o$  of VCO is identical to  $f_s$  except for a finite phase difference  $\phi$ .

- This phase difference  $\phi$  generates a corrective control voltage  $V_c$  to shift the VCO frequency from  $f_0$  to  $f_s$  and thereby maintain the lock.
- Once locked, PLL tracks the frequency changes of the input signal.
- Thus, a PLL goes through three (i) free running (ii) capture (iii) locked or tracking.
- Lock-in Range :- Once the PLL is locked, it can track frequency changes in the incoming signals.
- The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range.
- The lock range is usually expressed as a percentage of  $f_0$ , the VCO frequency.
- Capture Range :- The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of  $f_0$ .
- Pull-in-time :- The total time taken by the PLL to establish lock is called pull-in-time.
- Phase detector / comparator :-  
The phase detection is the most important part of the PLL system. There are two types of phase detectors used, analog and digital.
- Analog phase detector :-  
The principle of analog phase detection using switch type phase detector is shown in fig.

→ An electronic switch 's' is opened and closed by signal coming from VCO (normally a square wave) as shown in fig (b).

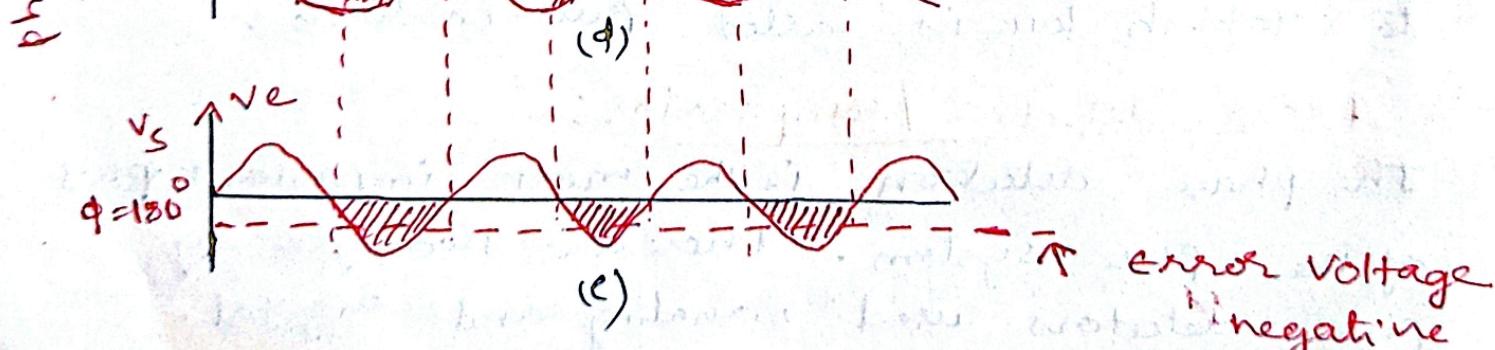
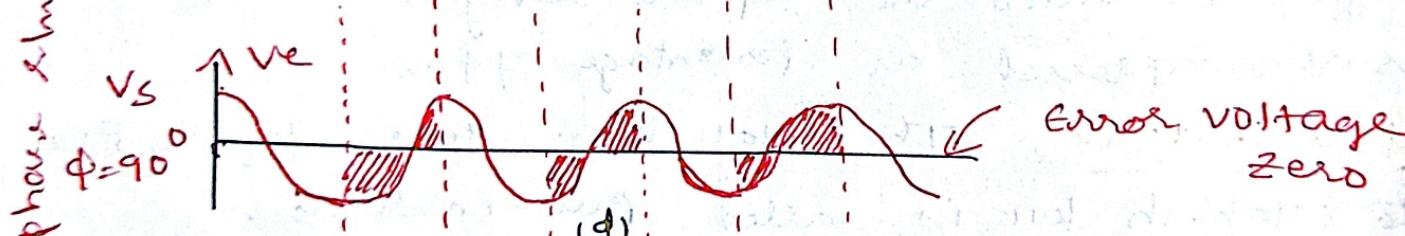
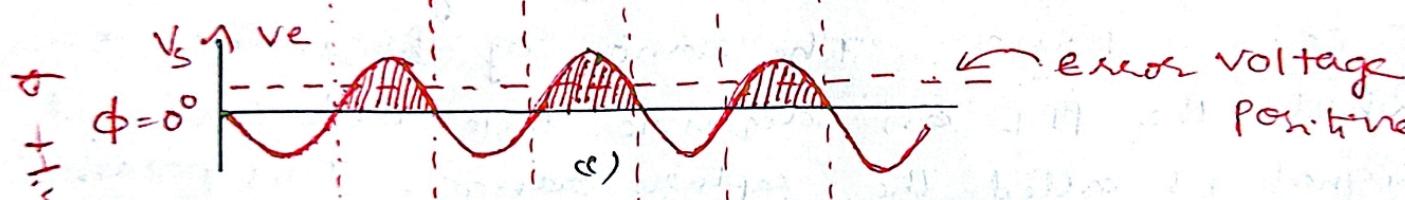
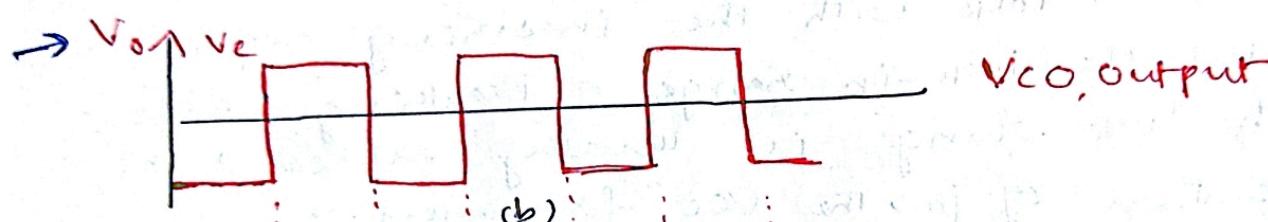
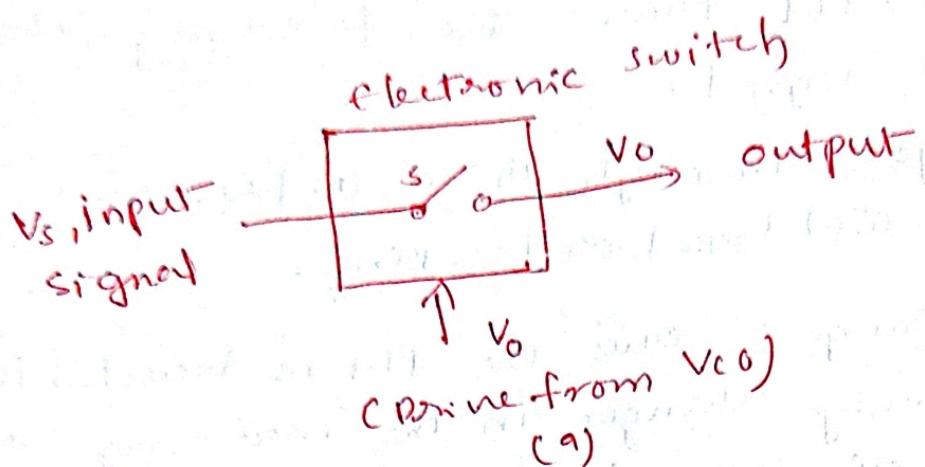


Fig: Phase detector for PLL (a) Basic scheme  
 (b) VCO output waveform. Input and output waveform (hatched) of phase detector for  
 (c)  $\phi = 0^\circ$ , (d)  $\phi = 90^\circ$ , (e)  $\phi = 180^\circ$

↓ shaded by means of time scanned by Scanner Go

- The input signal is, therefore, chopped at a repetition rate determined by VCO frequency.
- Fig(c) shows the input signal  $V_s$  assumed to be in phase ( $\phi = 0^\circ$ ) with VCO output  $V_o$ .
- Since the switch  $S$  is closed only when VCO output is positive, the output waveform  $V_e$  will be half sinusoids (shown hatched).
- Similarly, the output waveform for  $\phi = 90^\circ$  and  $\phi = 180^\circ$  is shown in fig.(d,e).
- This type of phase detector is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged.
- The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line in fig (c,d,e).
- It may be seen that the error voltage is zero when the phase shift between the two inputs is  $90^\circ$ . So, for perfect lock, the VCO output should be  $90^\circ$  out of phase with respect to the input signal.
- Analysis:
- A phase comparator is basically a multiplier which multiplies the input signal ( $V_s = V_s \sin 2\pi f_s t$ ) by the VCO signal ( $V_o = V_o \sin(2\pi f_o t + \phi)$ ). Thus the phase comparator output is
- $$V_e = k V_s V_o \sin(2\pi f_s t) \sin(2\pi f_o t + \phi)$$

where  $K$  is the phase comparator gain (or attenuation constant) and  $\phi$  is the phase shift between the input signal and the VCO output.

$$V_e = \frac{K V_s V_o}{2} [ \cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi) ]$$

when at lock, that is  $f_s = f_o$

$$V_e = \frac{K V_s V_o}{2} [ \cos(-\phi) - \cos(2\pi \times 2f_o t + \phi) ]$$

→ This shows that the phase comparator output contains a double frequency term and a dc term  $(K V_s V_o / 2) \cos \phi$  which varies as a function of phase  $\phi$ , that is  $\cos \phi$  between the two signals.

→ The double frequency term is eliminated by the low pass filter and the dc signal is applied to the modulating input terminal of a VCO.

→ It can be seen that in the perfect locked state ( $f_s = f_o$ ), the phase shift should be  $90^\circ$  ( $\cos 90^\circ = 0$ ), in order to get zero error signal, that is  $V_e = 0$ .

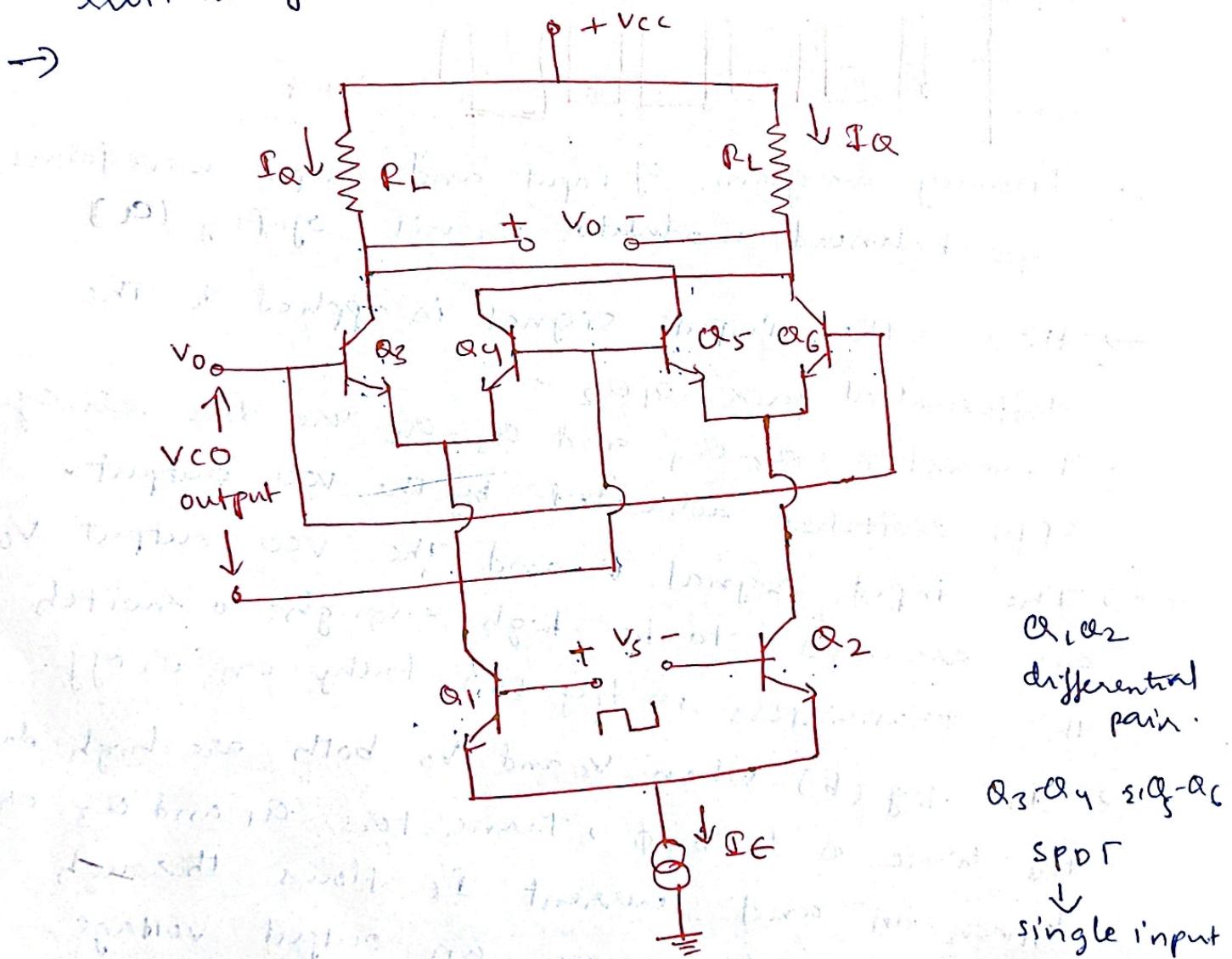
→ There are two problems associated with the switch type phase detector:

1. The output voltage  $V_e$  is proportional to the input signal amplitude  $V_s$ . This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude.

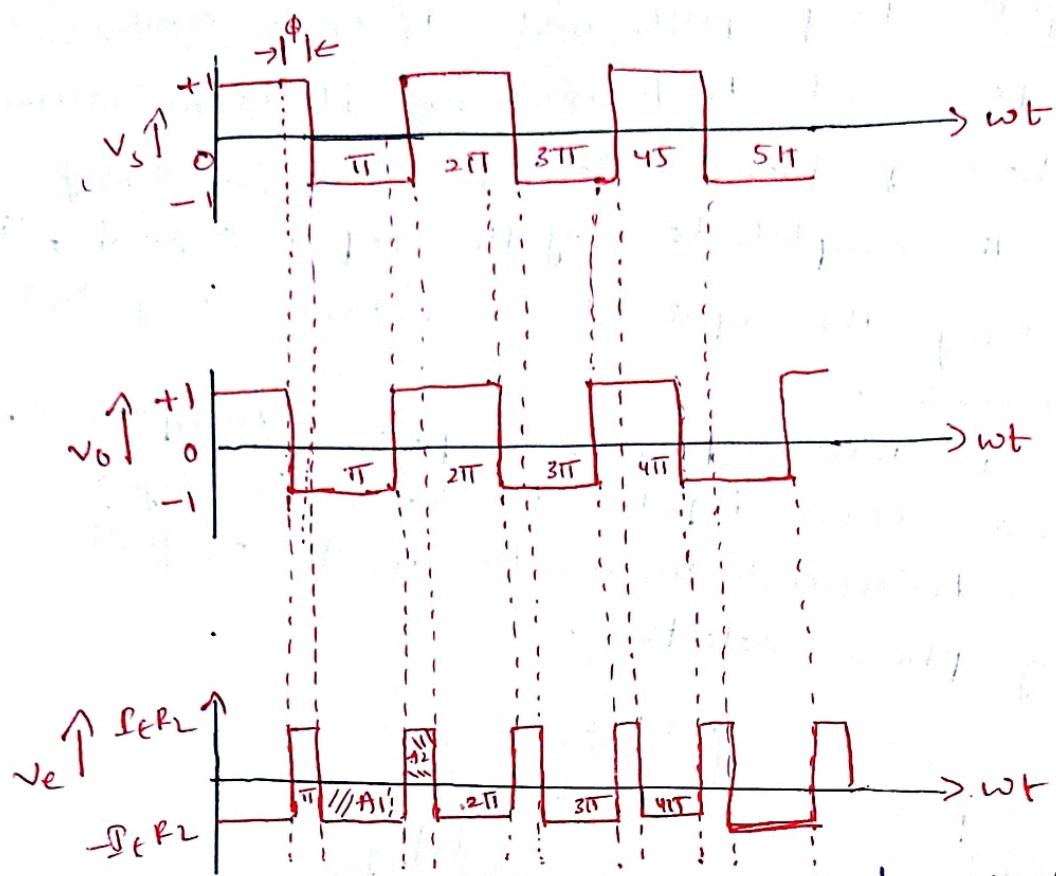
(4)

2. The output is proportional to  $\cos\phi$  and not proportional to  $\phi$  making it non-linear.

- Both these problems can be eliminated by limiting the amplitude of the input signal, that is converting the input to a constant amplitude square wave.
- A circuit which performs phase comparison with square wave input is shown in fig. as full-wave switching phase detector.
- This is a balanced modulator used in VCO.



(a) Phase detector for VCO PLL



Fig(b) Timing diagrams of input and output waveforms for balanced modulator circuit of fig (a)

- Here the input signal is applied to the differential pair  $Q_1-Q_2$ .
- Transistor  $Q_3-Q_4$  and  $Q_5-Q_6$  are two sets of SPDT switches activated by the VCO output.
- The input signal  $V_s$  and the VCO output  $V_o$  are assumed to be high enough to switch the transistors in fig (a) fully on or off.
- In fig (b) when  $V_s$  and  $V_o$  both are high during the time  $0$  to  $\pi-\phi$ , transistors  $Q_1$  and  $Q_3$  are driven on and current  $I_E$  flows through  $Q_1$  and  $Q_3$ . This gives an output voltage,

$$V_o = -I_{ERL} R_L$$

→ Next for the period  $(\pi - \phi)$  for  $\pi$ , when  $V_S$  is high and  $V_O$  is low, transistors  $Q_1$  and  $Q_2$  are driven on resulting in an output voltage.

$$V_C = I_C R_L$$

→ In this way, the output voltage waveform  $V_C$  in fig (b) is obtained.

→ The average value of the phase detector output  $V_C$  can be calculated as,

$$(V_C)_{AV} = \frac{1}{\pi} [ (area A_1) + (area A_2) ]$$

$$= \frac{1}{\pi} [ I_C R_L \phi + (-I_C R_L) \times (\pi - \phi) ]$$

$$= \frac{1}{\pi} [ I_C R_L \phi - I_C R_L \pi + I_C R_L \phi ]$$

$$= \frac{1}{\pi} [ 2 I_C R_L \phi - I_C R_L \pi ]$$

$$= \frac{I_C R_L (2\phi - \pi)}{\pi}$$

$$= I_C R_L \left( \frac{2\phi - \pi}{\pi} \right) \checkmark$$

$$= \frac{4 I_C R_L}{\pi} \left( \phi - \frac{\pi}{2} \right)$$

$$= K_\phi \left( \phi - \frac{\pi}{2} \right)$$

$$[\because I_C = 2 I_Q]$$

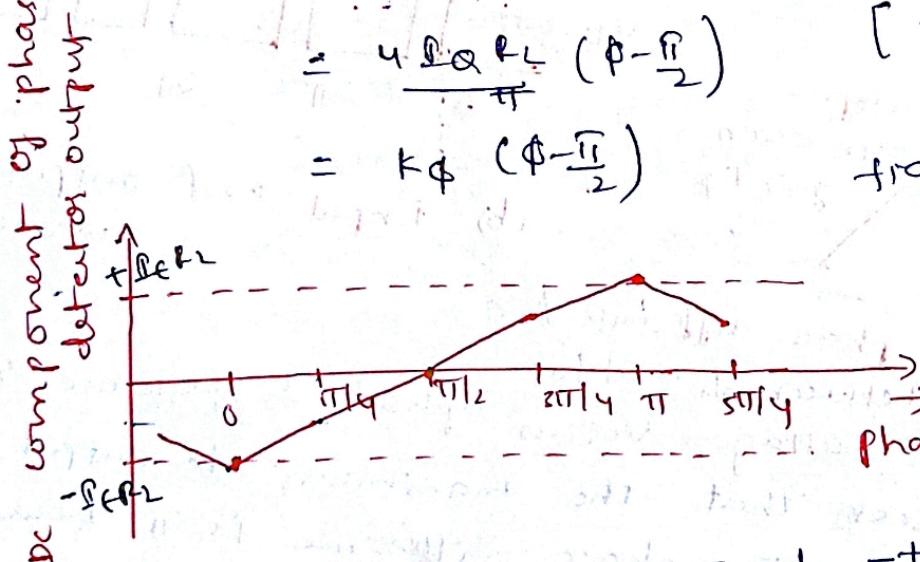
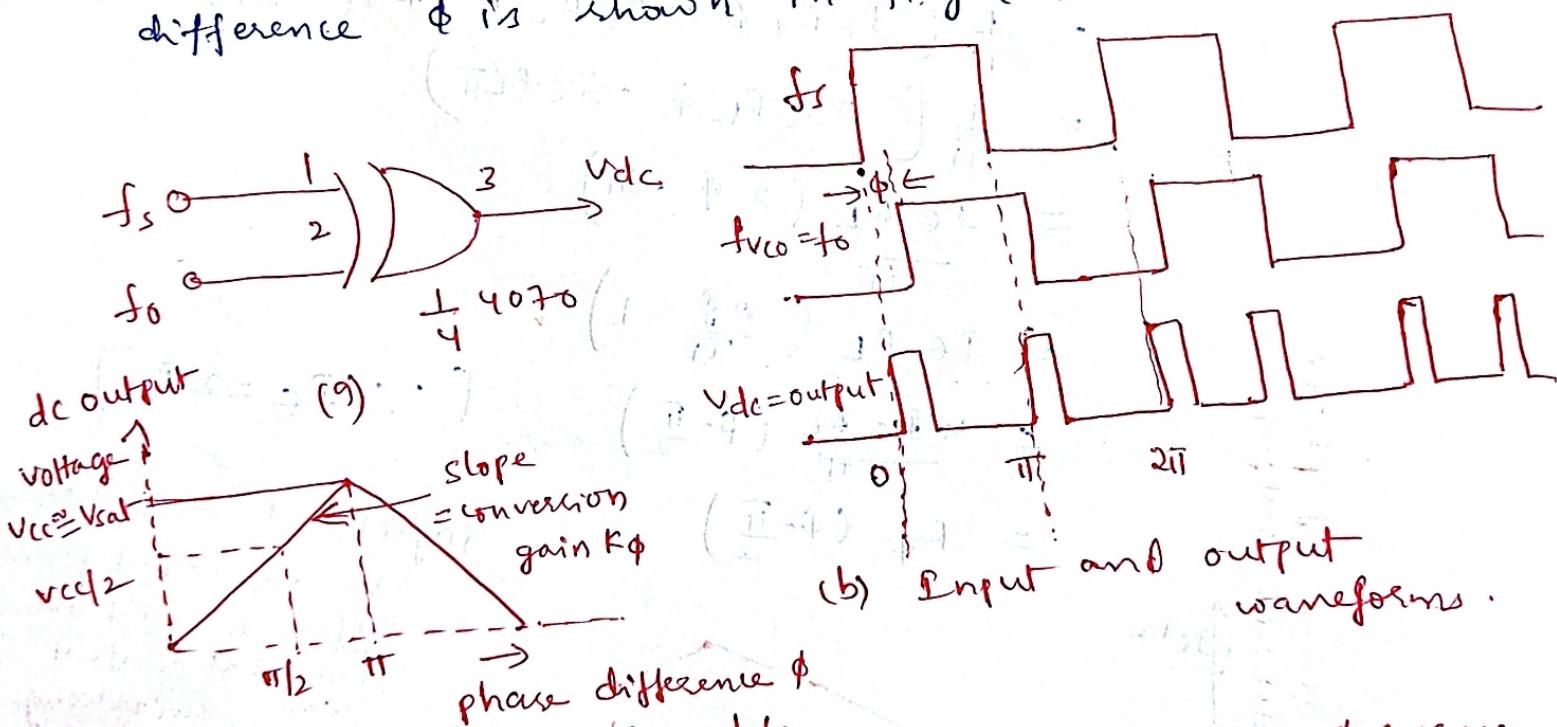


fig (c) output dc voltage versus input phase difference of balanced modulator full wave switching phase detector.

→ where  $K_\phi$  is the phase angle-to-voltage transfer co-efficient or, the conversion ratio of the phase detector. This linear relationship between  $V_C$  and  $\phi$  is depicted in

## → Digital phase detector:-

- Fig(a) shows the digital type XOR (exclusive-OR) phase detector.
- It uses CMOS type 4070 Quad 2-input XOR gate.
- The output of the XOR gate is high when only one of the input signals  $f_s$  or  $f_o$  is high.
- This type of detector is used when both the input signals are square waves.
- The input and output waveforms for  $f_s = f_o$  are shown in fig (b).
- In this fig,  $f_s$  is leading  $f_o$  by  $\phi$  degrees.
- The variation of dc output voltage with phase difference  $\phi$  is shown in fig (c).



(b) Input and output waveforms.

(c) DC output voltage versus phase difference  $\phi$  curve.

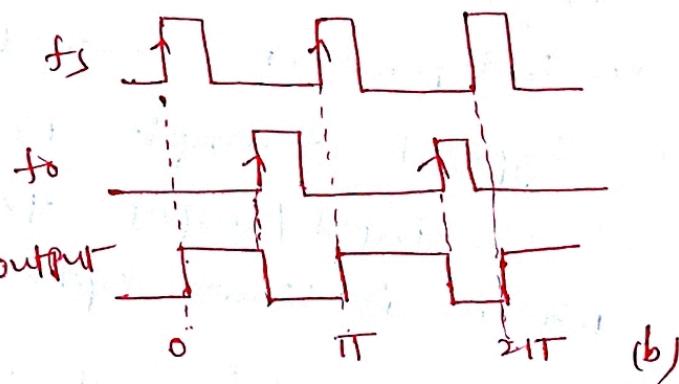
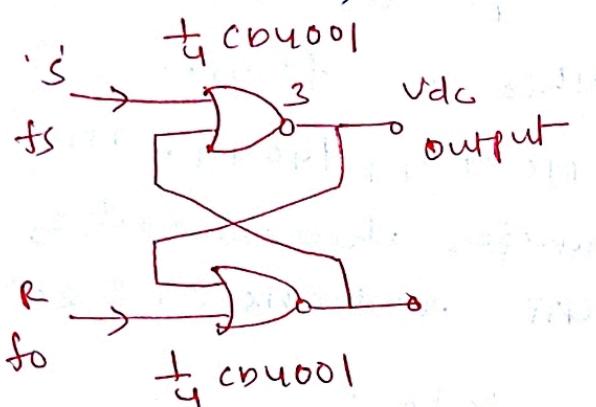
- It can be seen that the maximum dc output voltage occurs when the phase difference is  $\pi$  because the output of the gate remains high throughout.
- The slope of the curve gives the conversion ratio  $k_\phi$  of the phase detector.

(6)

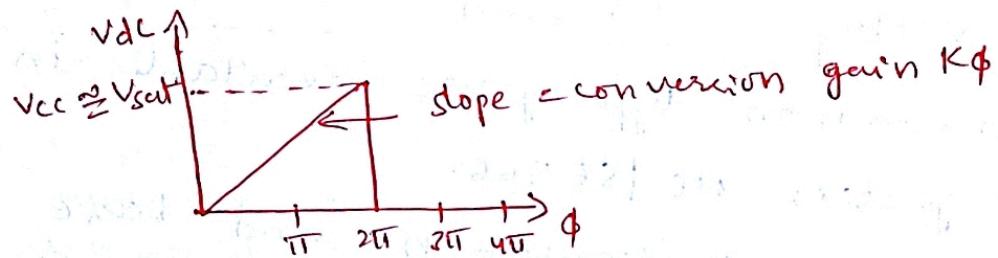
→ So, the conversion ratio  $K\phi$  for a supply voltage  $V_{cc} = 5V$  is,

$$K\phi = \frac{S}{\pi} = 1.59 V/\text{rad}$$

→ Another type of digital phase detector is an edge-triggered phase detector as shown in fig. below : (a)



(a)



phase difference between  $f_s$  and  $f_o$

(c)

- (a) Edge-triggered phase detector using CD4001, Quad 2-input NOR gate ; (b) Input and output waveforms, (c) dc output voltage vs phase difference  $\phi$ .

- The circuit is an R-S flip-flop made by NOR gates, such as CD 4001.
- This circuit is useful when  $f_s$  (incoming signal) and  $f_o$  (VCO output) are both pulse waveforms with duty cycle less than 50 percent.
- The output of the RS flip-flop changes its state on the leading edge of  $f_s$  and  $f_o$  is shown in fig(b).

- The variation of dc output voltage Vs phase difference between  $f_s$  and  $f_o$  is shown in fig (c).
- This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear upto  $360^\circ$  compared to  $180^\circ$  in the case of exclusive-or detector.
- Digital phase detector is also available in independent monolithic IC form.
- A typical example is MC4344/4044. This IC gives input/output transfer characteristic which is linear upto  $4\pi$  radians or  $\pm 20^\circ$ .
- Voltage controlled oscillator:
- A common type of VCO available in IC form is magnetics NE1SE566.
- The pin configuration and basic block diagram of 566 VCO are shown in fig(a), (b).
- Referring to fig(b), a timing capacitor  $C_t$  is linearly charged or discharged by a constant current source/sink.
- The amount of current can be controlled by changing the voltage  $V_c$  applied at the modulating input (pin 5) or by changing the timing resistor  $R_t$  external to IC chip.
- The voltage at pin 6 is held at the same voltage as pin 5.
- Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases,

resulting in less voltage across  $R_T$  and thereby decreasing the charging current.

### Voltage controlled oscillator

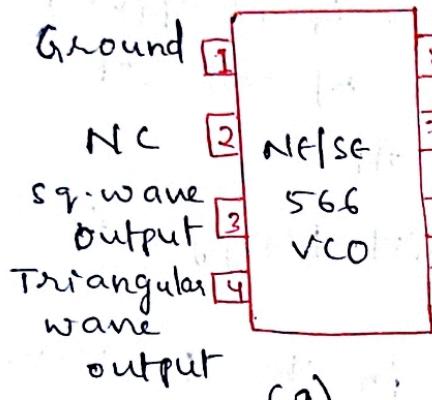
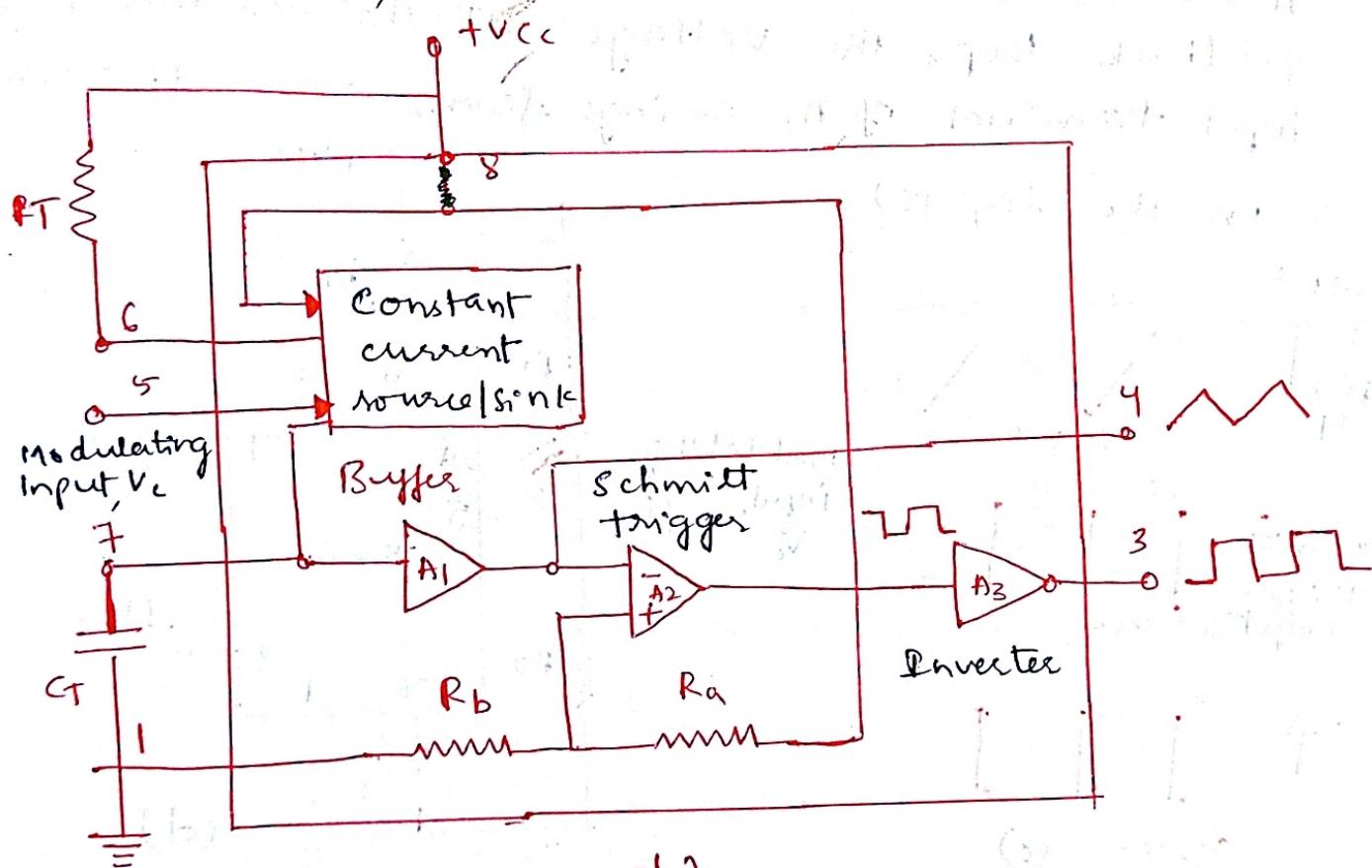


Fig (a) pin configuration

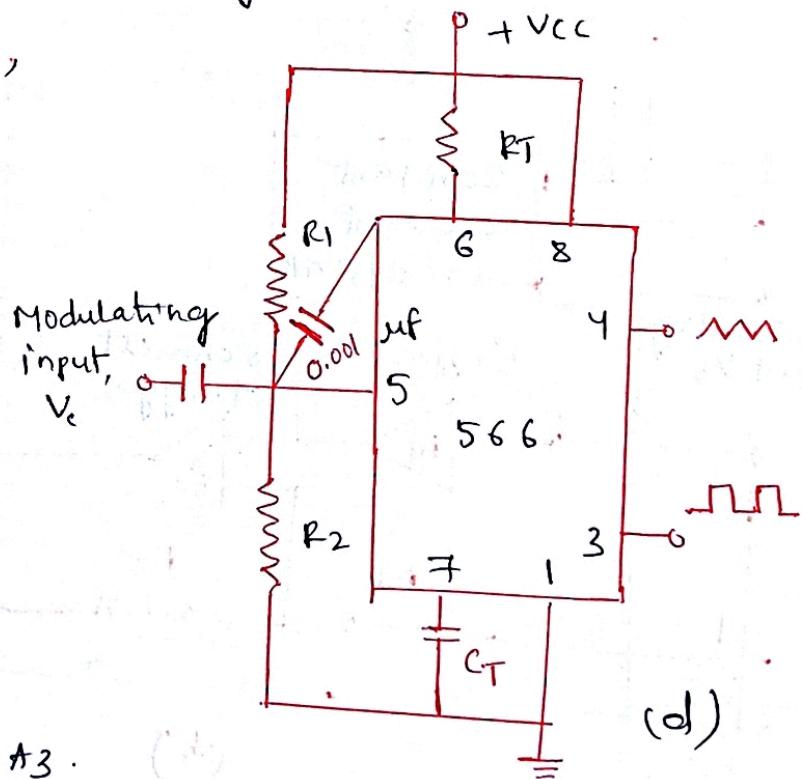
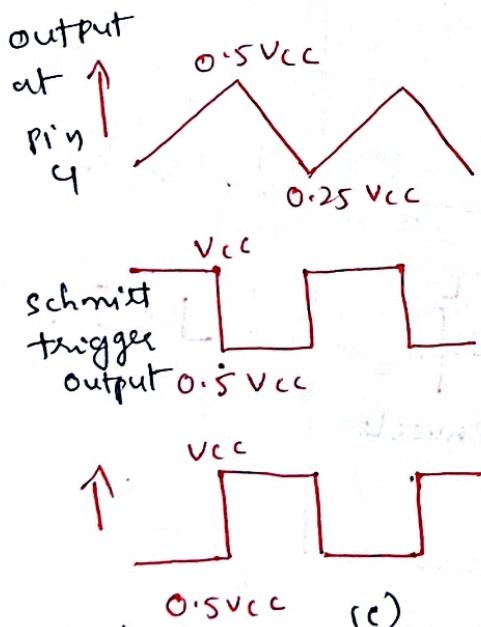
Fig (b) Block diagram



- A small capacitor of  $0.001\mu F$  should be connected between pins 5 and 6 to eliminate possible oscillations.
- A VCO is commonly used in converting low frequency signals such as EEGs, EKGs into an audio frequency range.

- These audio signals can be transmitted over telephone lines or a two way radio communication systems for diagnostic purposes or can be recorded on a magnetic tape for further reference.
- The voltage across the capacitor  $C_T$  is applied to the inverting input terminal of schmitt trigger  $A_2$  via buffer amplifier  $A_1$ .
- The output swing of the schmitt trigger is designed to  $V_{CC}$  and  $0.5V_{CC}$ .
- If  $R_a$  and  $R_b$  are equal  $R_a = R_b$  in the positive feedback loop, the voltage at the non-inverting input terminal of  $A_2$  swings from  $0.5V_{CC}$  to  $0.25V_{CC}$ .

→ In the fig (c),



fig(c) Output waveform (d) Typical connection diagram.

→ When the voltage on the  $C_T$  exceeds  $0.5V_{CC}$  during charging, the output of the schmitt trigger goes Low ( $0.5V_{CC}$ ).

- The capacitor now discharges and when it is at  $0.25V_{cc}$ , the output of schmitt trigger goes HIGH ( $V_{cc}$ ).
- since the source and sink currents are equal, capacitor charges and discharges for the same amount of time.
- This gives a triangular voltage waveform across  $C_T$  which is also available at pin 4.
- The square wave output of the schmitt trigger is inverted by inverter  $A_3$  and is available at pin 3.
- The inverter  $A_3$  is basically a current amplifier used to drive the load.
- The output waveforms are shown in fig(c)
- The output frequency of the VCO can be calculated as:
- The total voltage on the capacitor changes from  $0.25V_{cc}$  to  $0.5V_{cc}$ .
- Thus  $\Delta V = 0.25V_{cc}$ .
- The capacitor charges with a constant-current source. It obtains current  $i$
- so,  $\frac{\Delta V}{\Delta t} = \frac{i}{C_T}$
- or,  $\frac{0.25V_{cc}}{\Delta t} = \frac{i}{C_T}$
- or  $\Delta t = \frac{0.25V_{cc}C_T}{i}$

→ the time period  $T$  of the triangular waveform  
 $= 2\Delta t$ . The frequency of oscillator  $f_0$  is,

$$f_0 = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{1}{0.5V_{CC}C_T}$$

$$\text{But, } i = \frac{V_{CC} - V_C}{R_T}$$

where,  $V_C$  is the voltage at pin 5. therefore,

$$f_0 = \frac{V_{CC} - V_C}{0.5V_{CC} R_T C_T}$$

$$f_0 = \frac{2(V_{CC} - V_C)}{C_T R_T V_{CC}}$$

- The output frequency of the VCO can be changed either by (i)  $R_T$  (ii)  $C_T$  or (iii) the voltage  $V_C$  at the modulating input terminal pin 5.
- The voltage  $V_C$  can be varied by connecting a  $R_1 R_2$  circuit as shown in fig(d).
- The components  $R_T$  and  $C_T$  are first selected so that VCO output frequency lies in the centre of the operating frequency range.
- Now the modulating input voltage is usually varied from  $0.75V_{CC}$  to  $V_{CC}$  which can produce a frequency variation of about 10 to 1.
- With no modulating input signal, if the voltage at pin 5 is biased at  $\frac{7}{8}V_{CC}$ , the VCO output frequency is  $f_0 = \frac{2(V_{CC} - \frac{7}{8}V_{CC})}{C_T R_T V_{CC}} = \frac{2V_{CC}}{8R_T C_T} = \frac{1}{4R_T C_T}$

$$f_0 = \frac{0.25}{R_T C_T}$$

→ Voltage to frequency conversion factor :-

→ A parameter of importance for VCO is voltage to frequency conversion factor  $K_V$  and is defined as :  $K_V = \frac{\Delta f_0}{\Delta V_C}$

→ Here  $\Delta V_C$  is the modulation voltage required to produce the frequency shift  $\Delta f_0$  for a VCO.

→ If we assume that, the original frequency is  $f_0$  and the new frequency is  $f_1$ , then,

$$\Delta f_0 = f_1 - f_0 = 2 \left( \frac{V_{CC} - V_C + \Delta V_C}{CTR T V_{CC}} \right) - 2 \left( \frac{V_{CC} - V_C}{CTR T V_{CC}} \right)$$

$$\Delta f_0 = \frac{2 \Delta V_C}{CTR T V_{CC}}$$

putting the value of  $CTR T$  from  $T = \frac{1}{R_f C_f} \cdot \frac{1}{4 R_f L_f}$

$$CTR T = \frac{1}{4 f_0}$$

$$\therefore \Delta V_C = \Delta f_0 \cdot \frac{1}{4 f_0} \cdot \frac{V_{CC}}{2} = \Delta f_0 \cdot \frac{V_{CC}}{8 f_0}$$

$$\text{or } K_V = \frac{\Delta f_0}{\Delta V_C} = \frac{\Delta f_0}{\Delta f_0 \cdot \frac{V_{CC}}{8 f_0}} = \frac{8 f_0}{V_{CC}}$$

$$K_V = \frac{8 f_0}{V_{CC}}$$

→ Low pass filter:

→ The filter used in a PLL may be either passive type or active type as shown in fig.

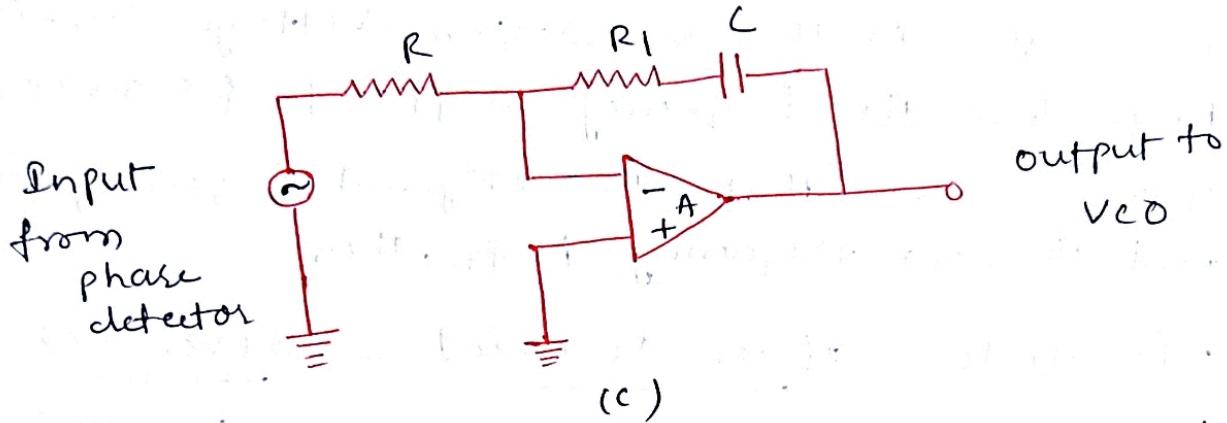
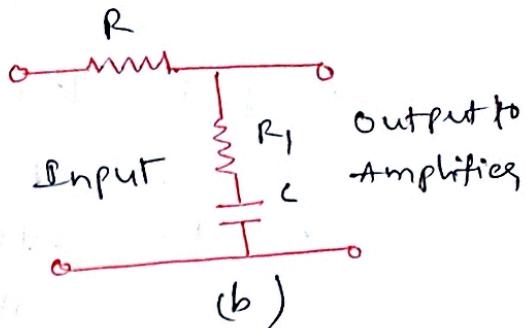
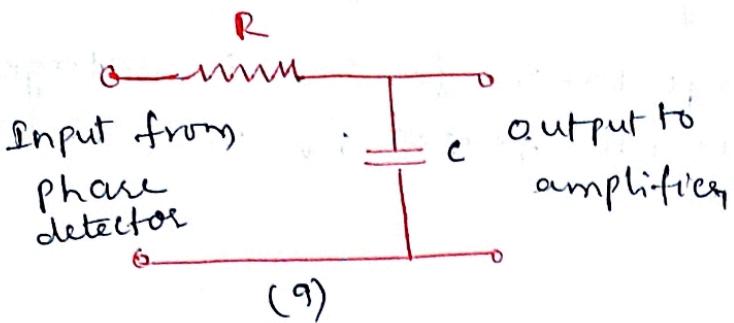


Fig  
(a) Low pass filter, (b) passive filter (c) Active filter.

- The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL.
- These characteristics include capture and lock range, band-width and transient response.
- If filter band-width is reduced, the response time increases.
- However, reducing the band-width of the filter also reduces the capture range of the PLL.
- The filter serves one more important purpose.
- The charge on the filter capacitor gives a short time 'memory' to the PLL.
- Thus, even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO till

it picks up signal again.

→ This produces a high noise immunity and locking stability.

### → Monolithic phase-Locked Loop:

→ All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL.

→ However, a number of manufacturers have introduced monolithic PLLs too.

→ Some of the important monolithic PLLs are SEINe 560 series introduced by signetics and LM560 series by national semiconductor.

→ The SEINe 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges.

→ Since 565 is the most commonly used PLL, will see some of the important features of this IC chip.

### → IC PLL 565:

→ 565 is available as a 14-pin DIP package

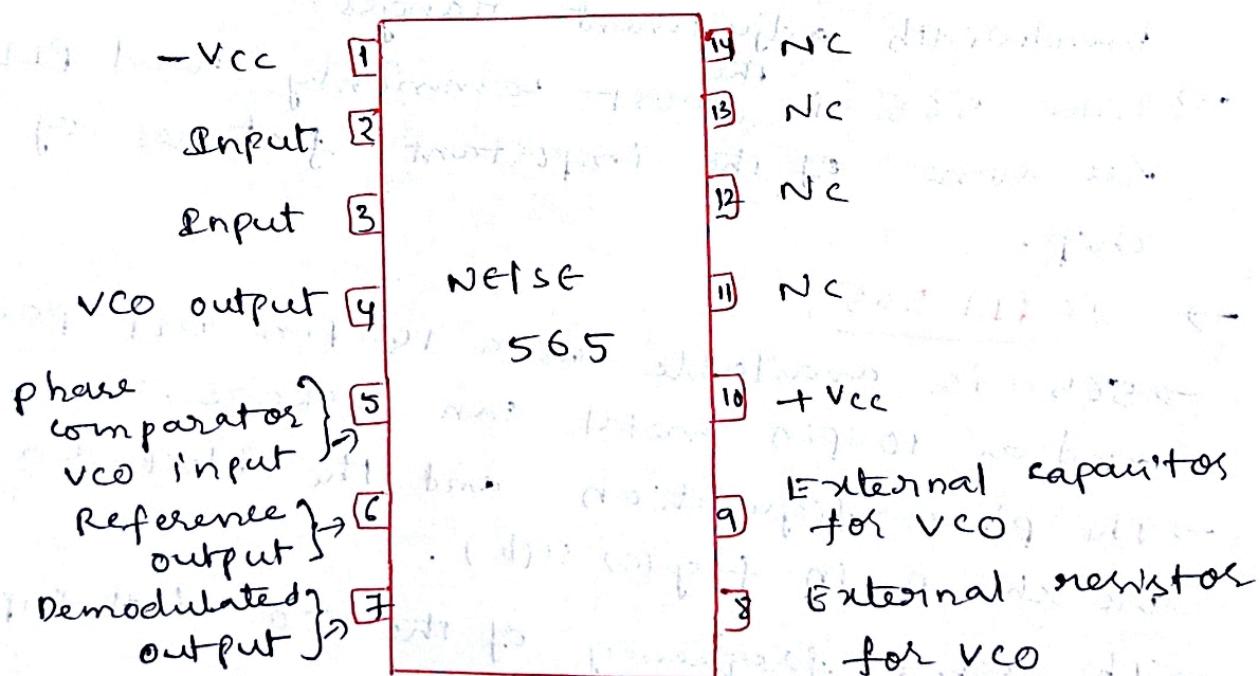
and as 10-pin metal can package.

→ The pin configuration and the block diagram are shown in fig (a) & (b).

→ The output frequency of the VCO (both inputs 2, 3 grounded) is given by  $f_o = \frac{0.25}{R_T C_T} \text{ Hz}$ .

where  $R_T$  and  $C_T$  are the external resistor and capacitor connected to Pin 8 and Pin 9.

- A value between  $2k\Omega$  and  $20k\Omega$  is recommended for  $R_T$ .
- The VCO free running frequency is adjusted with  $R_T$  and  $C_T$  to be at the centre of the input frequency range.
- The phase locked loop is internally broken between the VCO input and the phase comparator input.
- A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare it with input signals.
- A capacitor 'C' is connected between pin 7 and pin 10 (Supply terminal) to make a low pass filter with the internal resistance of  $3.6k\Omega$ .



Fig(a) Pin diagram

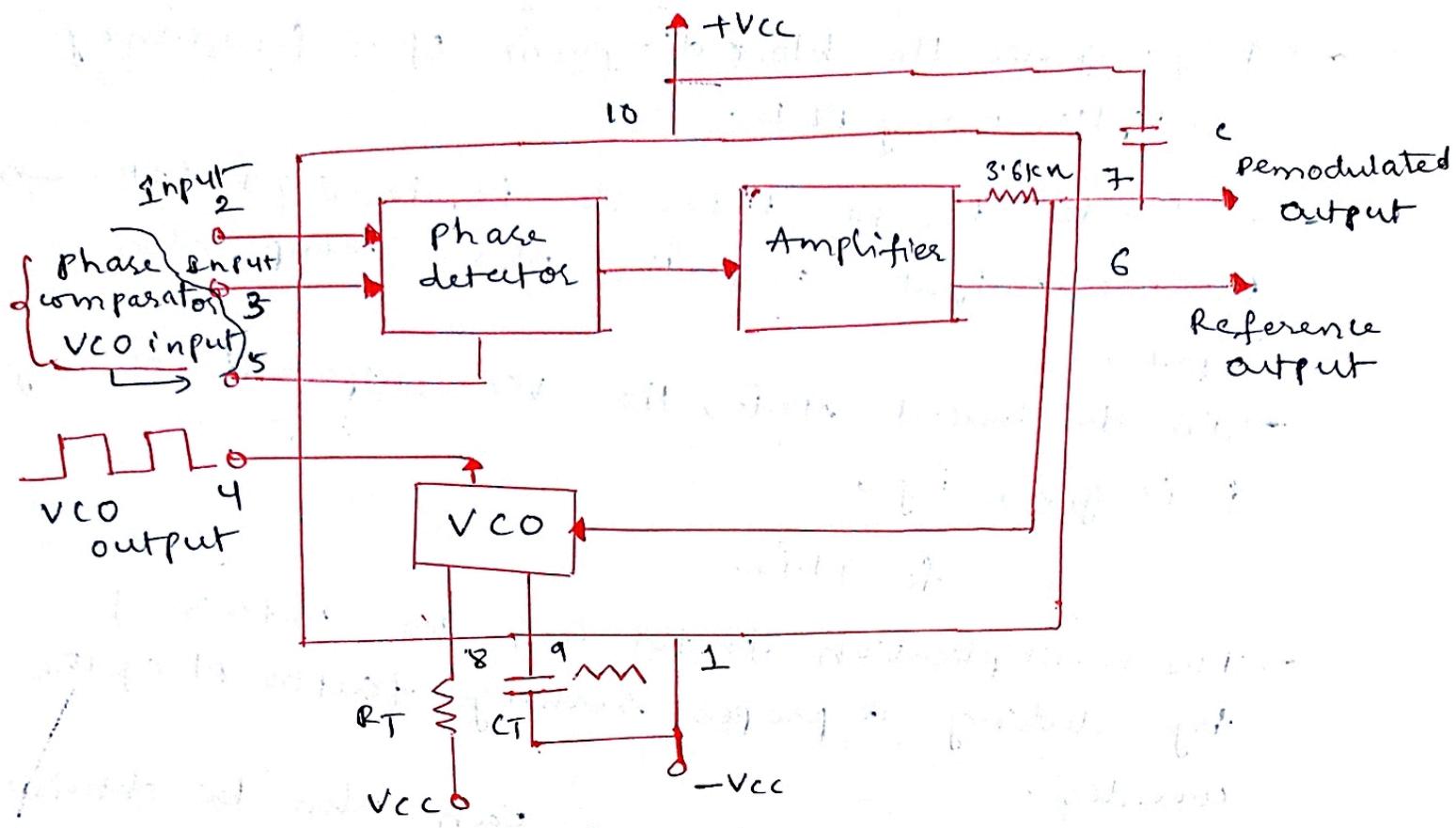


Fig. (b) NELSC 565 PLL block diagram.

→ PLL applications :-

→ Frequency multiplication / division

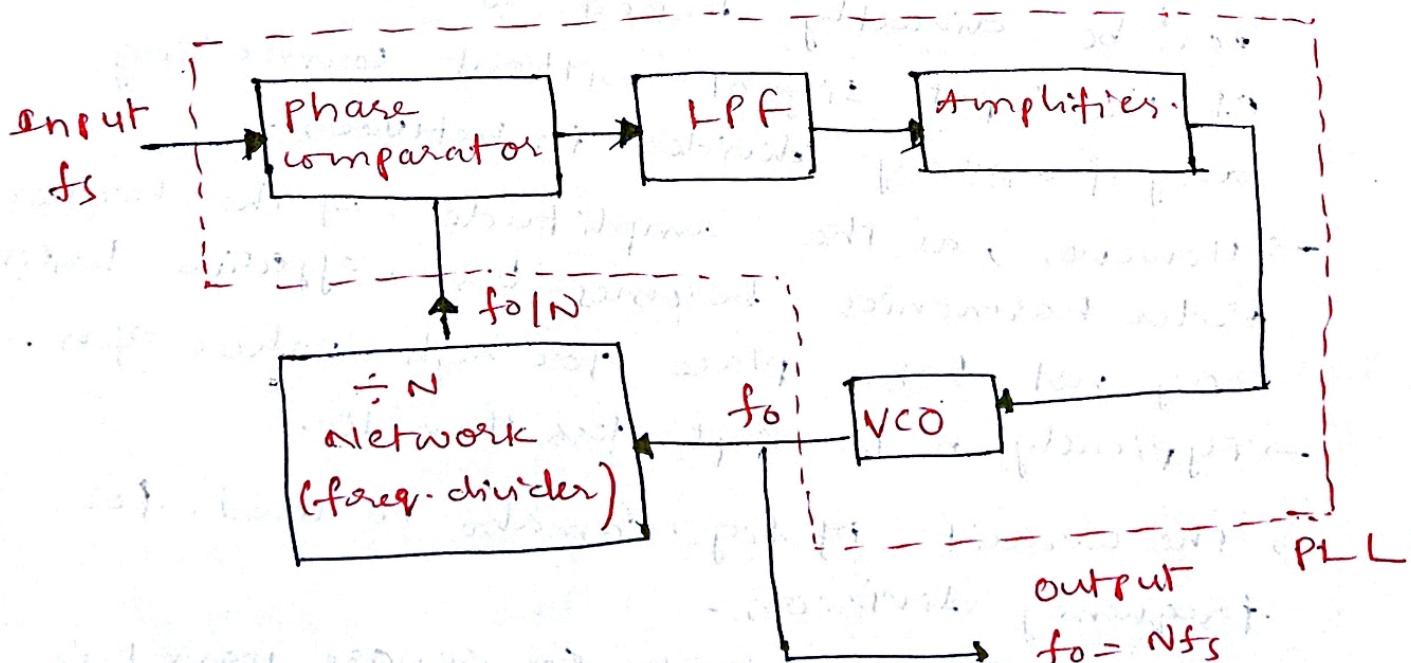


Fig: frequency multiplier using the PLL.

→ Fig. gives the block diagram of a frequency multiplier using PLL.

→ A divide by  $N$  network is inserted between the VCO output and the phase comparator input.

→ In the locked state, the VCO output frequency  $f_0$  is given by,

$$f_0 = N f_s.$$

→ The multiplication factor can be obtained by selecting a proper scaling factor  $N$  of the counter.

→ Frequency multiplication can also be obtained by using PLL in its harmonic locking mode.

→ If the input signal is rich in harmonics e.g. square wave, pulse train etc., then VCO can be directly locked to the  $n$ -th harmonic of the input signal without connecting any frequency divider in between.

→ However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of  $n$ .

→ Typically  $n$  is kept less than 10.

→ The circuit of fig. can also be used for frequency division.

→ Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the  $m$ -th harmonic of the VCO output with the input signal  $f_s$ .

→ The output  $f_o$  of VCO is now given by

$$f_o = \frac{f_s}{m}$$

→ Frequency translation:

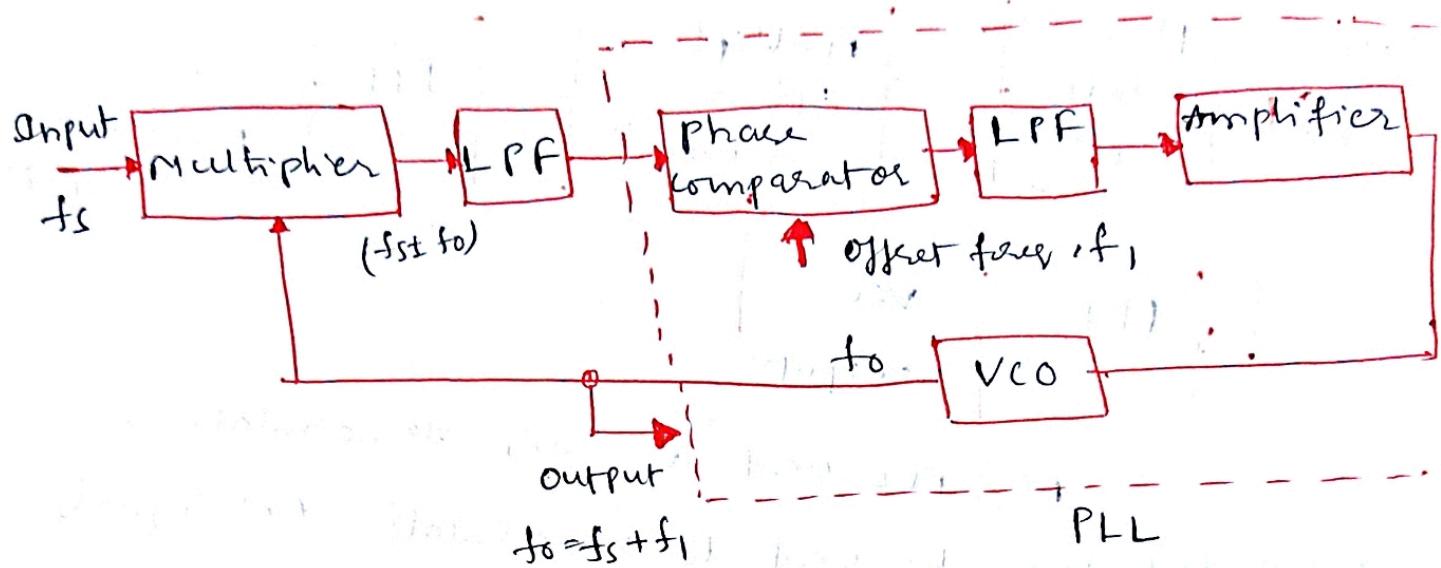


Fig: PLL used as a frequency translator.

→ A schematic for shifting the frequency of an oscillator by a small factor is shown in fig.

→ It can be seen that a mixer (or multiplier) and a low pass filter are connected externally to the PLL.

→ The signal  $f_s$  which has to be shifted, and the output frequency  $f_o$  of the VCO are applied as inputs to the mixer.

→ The output of the mixer contains the sum and difference of  $f_s$  and  $f_o$ .

→ However, the output of LPF 1 contains only the difference signal ( $f_o - f_s$ ).

→ The translation, or offset frequency  $f_1$  ( $f_1 < f_s$ ) is applied to the phase comparator.

→ When PLL is in locked state,

$$f_o - f_s = f_1$$

thus, it is possible to shift the incoming frequency  $f_s$  by  $f_1$ .

→ AM detection:

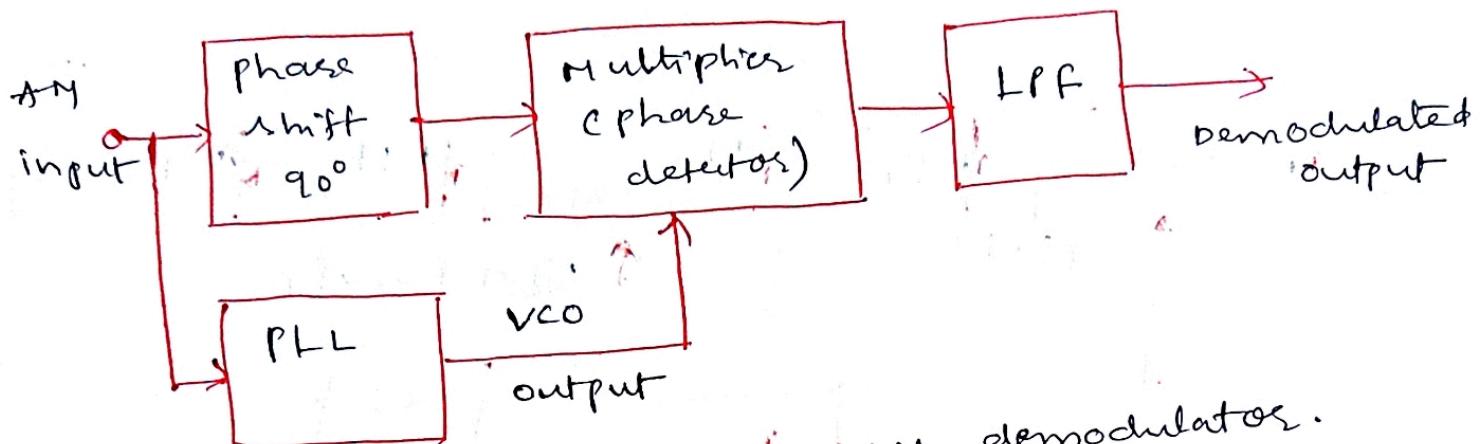


Fig: PLL used as AM demodulator.

- A PLL may be used to demodulate AM signals as shown in fig.
- The PLL is locked to the carrier frequency of the incoming AM signals.
- The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier.
- Since VCO output is always  $90^\circ$  out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by  $90^\circ$  before being fed to the multiplier.
- This makes both the signals applied to the multiplier in same phase.
- The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF.

→ Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

→ FM demodulation:-

- If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal.
- The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.
- The VCO transfer characteristics determine the linearity of the demodulated output.
- Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.