

UNIT-I

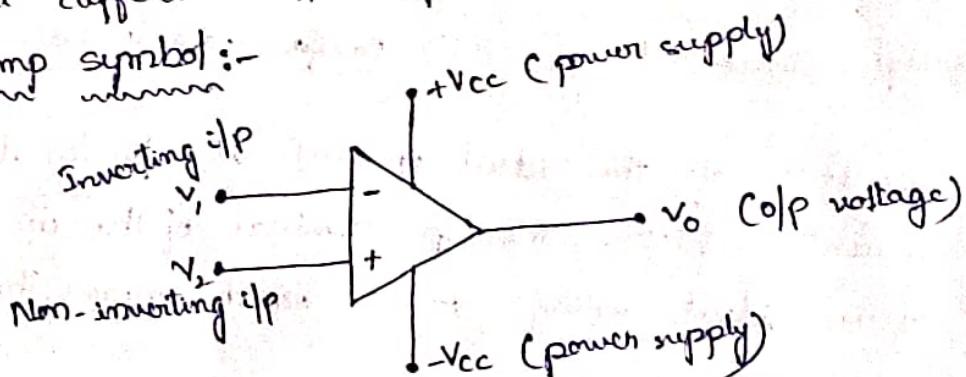
OPERATIONAL AMPLIFIER

Operational amplifier :- It is commonly referred to as op-amp.

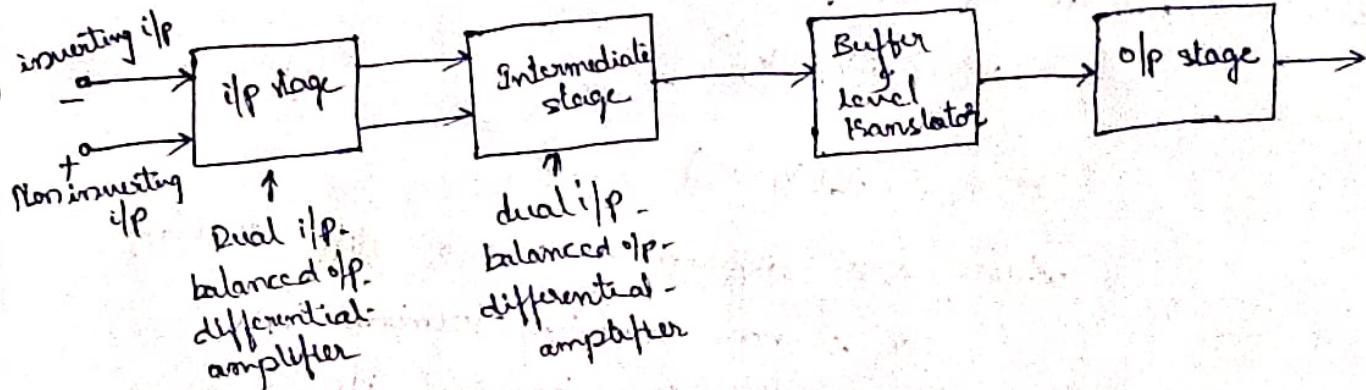
It is defined as a direct coupled high gain amplifier with one (or) more differential amplifiers used to amplify both A.C. and D.C. signals which can also perform mathematical operations like addition, subtraction, multiplication & integration etc.

An op-amp is a DC coupled high voltage amplifier ckt with a difference i/p signal.

Op-amp symbol :-



Block diagram of op amp :-



Ideal op-amp :-

The ideal operational amplifier is a differential i/p and single-ended o/p device (i.e., differential amplifier). It amplifies the difference b/w the two inputs signals.

The equivalent circuit and transfer characteristics of ideal op-amp is shown in below figure.

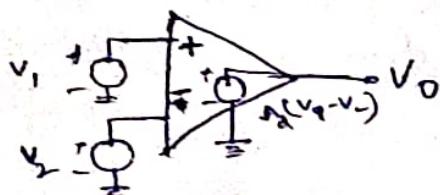
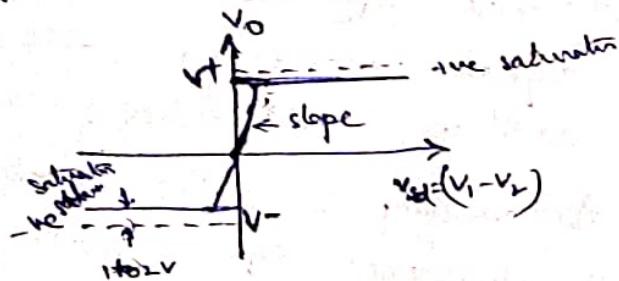


Fig (a) Ideal op-amp equivalent circuit



(b) Transfer characteristics

The input impedance of the ideal op-amp is infinite it means that the o/p current is zero. The o/p terminal of the op-amp acts as the o/p of an ideal voltage source which means the small o/p impedance is zero.

In ideal op-amp, the o/p voltage v_o is proportional to the difference b/w two i/p sigs. Hence we can write,

$$v_o \propto (V_1 - V_2)$$

$$\Rightarrow v_o = A_d(V_1 - V_2)$$

where A_d is differential gain of differential amp.

V_1 is non-inverting terminal i/p

V_2 is Inverting terminal i/p.

→ If we apply two i/p signals are equal in all the respects to the differential amplifier i.e., $V_1 = V_2$, then the ideal o/p voltage

$$v_o = A_d(V_1 - V_2) \text{ must be zero.}$$

But practically, when $(V_1 = V_2) \neq 0$, there exist some o/p signal called common mode signal. So that i.e., $V_c = \frac{V_1 + V_2}{2}$.

so that the differential amplifier produces o/p pr voltage proportional to such common mode sig. $v_o = A_c \cdot V_c$

For an ideal amplifier, differential gain "A_d" must be infinite and common mode gain "A_c" must be zero. So, when $V_1 = V_2$, the differential amplifier will produce zero o/p with a characteristic called common mode rejection.

Common Mode Rejection Ratio (CMRR):-

When the same voltage is applied to both the i/p's, the differential amplifier is said to be operated in common mode configuration. Many disturbance sig's, noise sig's appear as a common o/p signal to both the i/p terminals of the differential amplifier. Such common signals should be rejected by the differential amplifier.

The ability of differential amplifier to reject a common mode sig is expressed by a ratio called Common Mode Rejection Ratio denoted as "CMRR".

It is defined as the ratio of differential voltage gain A_d to common mode voltage gain A_c .

$$CMRR = \rho = \left| \frac{A_d}{A_c} \right|$$

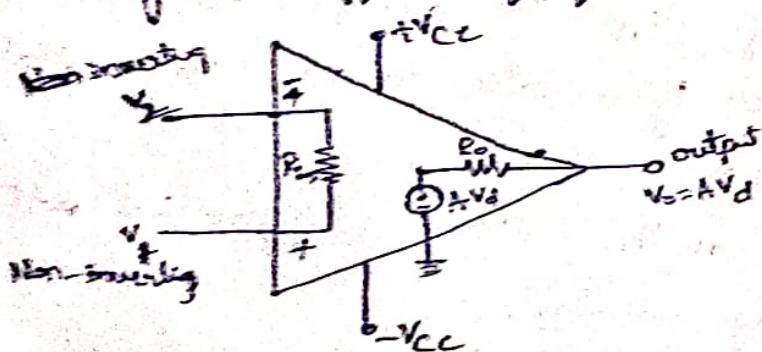
Ideally, common mode gain is zero, hence ideal value of CMRR is infinite.

Characteristics of ideal op-amp :-

- (i) Infinite input resistance ($R_i = \infty$)
- (ii) Infinite voltage gain ($A = \infty$)
- (iii) Zero op. resistance ($R_o = 0$)
- (iv) Zero offset voltage ($V_{off} = 0$)
- (v) Infinite bandwidth ($B.W = \infty$)
- (vi) Infinite CMRR ($CMRR = \infty$)
- (vii) Infinite slew rate ($S = \infty$)
- (viii) No effect of temp. (characteristics don't drift with temp.)

Practical op-amp :-

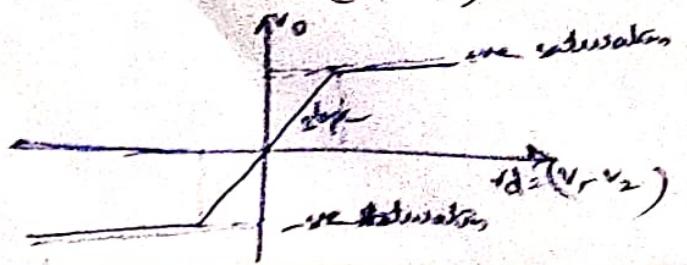
A practical op-amp is not ideal. The equivalent circuit of a practical op-amp is shown in below figure. The equivalent circuit represents the parameters in terms of physical components and it is used for analyzing the operating principles of op-amps and in observing the effects of feedback.



$\rightarrow A \cdot V_d$ is an equivalent Thevenin voltage source and R_d Thevenin equivalent resistance

$$V_d = A(V_s)$$

$$V_d = A(V_1 - V_2).$$

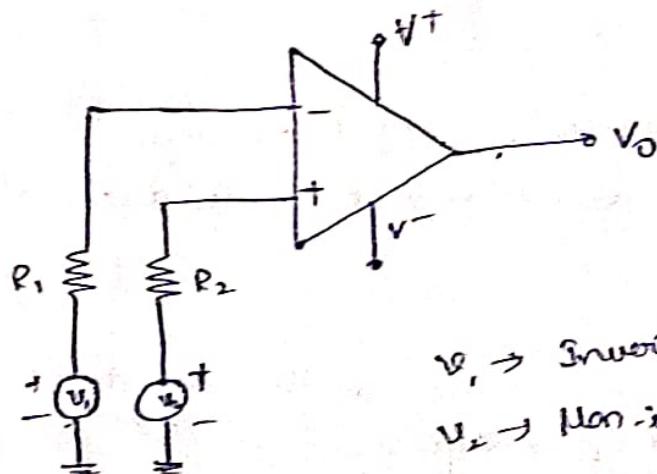


Characteristics of practical op-amp :-

- (i) High i/p resistance
- (ii) High voltage gain
- (iii) Low o/p resistance
- (iv) Low offset voltage
- (v) High bandwidth
- (vi) High CMRR
- (vii) High slew rate

Modes of operation of op-amp :-

Open loop operation of op-amp :-



$V_1 \rightarrow$ Inverting i/p voltage

$V_2 \rightarrow$ Non-inverting i/p voltage

The simplest way to use an op-amp is in the open-loop. As the gain is infinite for an opamp, the op will always saturate either positive (+) or negative.

If $V_1 > V_2$ then the op will saturate with a negative ($-V_{sat}$)

If $V_1 < V_2$ then the op will saturate with a positive ($+V_{sat}$)

It has only two possible o/p voltages i.e., $+V_{sat}$ ($V_1 > V_2$)
 $-V_{sat}$ ($V_1 < V_2$)

Virtual ground concept:

This means the differential voltage V_d b/w the i/p terminals is essentially zero even if o/p voltage is few volts. Due to large open-loop gain of op-amp, the difference voltage V_d is almost zero.

$$V_o = V_d A_{OL} \Rightarrow V_d = \frac{V_o}{A_{OL}} = \text{almost zero}$$

$$\therefore V_d = V_+ - V_- = 0$$

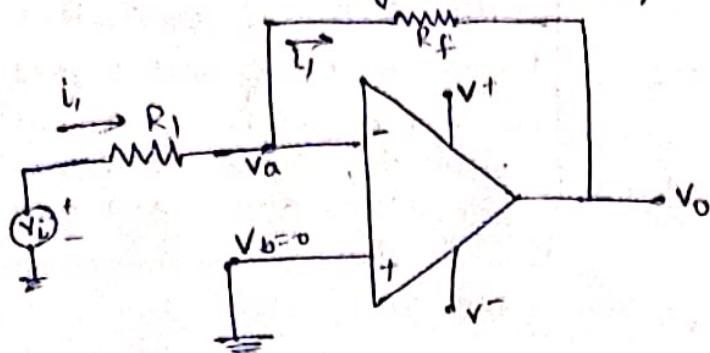
$$\therefore V_+ = V_-$$

Now, if the non-inverting terminal is grounded by the concept of virtual short, the inverting terminal is also at ground potential, though there is no physical connection. This called virtual ground concept.

Inverting amplifier :-

Inverting amplifier is an amplifier circuit where the non-inverting terminal is grounded and if it is applied at the inverting terminal.

It has a negative feedback. So that the o/p of the op-amp is fed back to inverting ip through feedback resistor 'R_f'.



Analysis: For simplicity assume an ideal op-amp.

According to virtual ground concept, node 'a' also at ground potential since $V_a = 0$.

$$\therefore i_1 = \frac{V_i}{R_1}$$

Since op-amp draws no current, all the current flowing through R_1 must flow through R_f . The o/p voltage is,

$$V_o = -i_1 R_f = -\frac{V_i R_f}{R_1}$$

$$\therefore \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

-ve sign indicate 180° phase shift. Hence it is inverting amplifier.

The gain of inverting amplifier is $\boxed{\frac{V_o}{V_i} = -\frac{R_f}{R_1}}$

Alternatively,-

Notat equation at node 'a'.
Apply KCL at node 'a'.

$$\frac{V_i - V_a}{R_1} = \frac{V_a - V_o}{R_f}$$

As per virtual ground, $V_a = 0$.

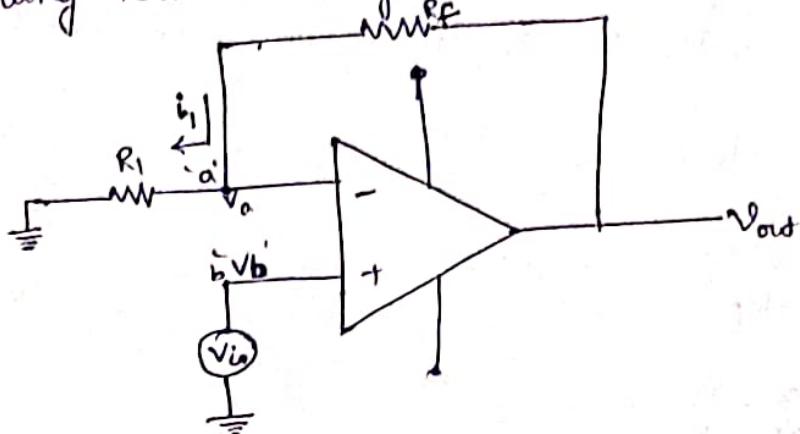
$$\Rightarrow \frac{V_i}{R_1} = -\frac{V_o}{R_f}$$

$$\therefore V_o = -\frac{R_f}{R_1} V_i$$

$$\therefore \text{the gain } A = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Non-inverting amplifier :-

Non-inverting amplifier is an op-amp amplifier circuit where the input is applied at the non-inverting terminal and inverting terminal is grounded.



According to virtual ground concept

$$V_a = V_b$$

$$\text{As per KCL, } V_b = V_i$$

$$\therefore V_a = V_i$$

Apply KCL at node 'a'.

$$\frac{V_o - V_a}{R_f} = \frac{V_a - 0}{R_1}$$

$$\Rightarrow \frac{V_o - V_i}{R_f} = \frac{V_i}{R_1}$$

$$\Rightarrow \frac{V_o}{R_f} - \frac{V_i}{R_f} = \frac{V_i}{R_1}$$

$$\Rightarrow \frac{V_o}{R_f} = V_i \left(\frac{1}{R_1} + \frac{1}{R_f} \right)$$

$$\Rightarrow V_o = V_i \cdot R_f \left(\frac{R_f + R_1}{R_1 R_f} \right)$$

$$\Rightarrow V_o = \left(\frac{R_f + R_1}{R_1} \right) V_i$$

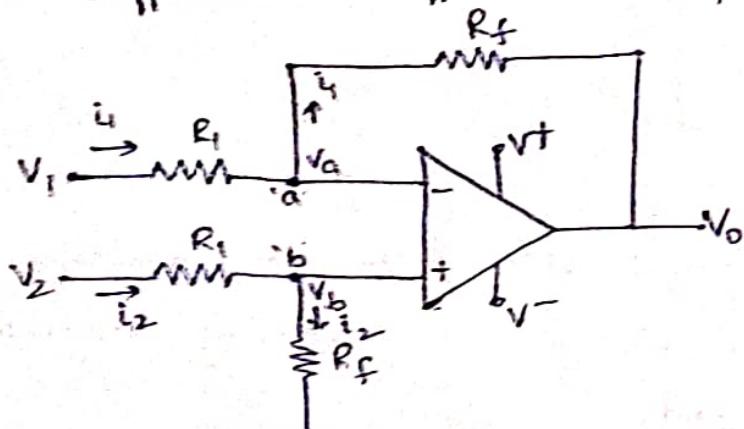
$$\Rightarrow V_o = \left(1 + \frac{R_f}{R_1} \right) V_i$$

The gain of non-inverting amplifier

$$\text{is } \frac{V_o}{V_i} = \left(1 + \frac{R_f}{R_1} \right)$$

Differential amplifier :-

A circuit that amplifies the difference between two signals is called a difference (or) differential amplifier.



This type of amplifier circuit is very useful in instrumentation circuits.

Analysis :- Apply KCL at node 'a'

$$\frac{V_1 - V_a}{R_1} = \frac{V_a - V_o}{R_f}$$

$$\frac{V_1}{R_1} - \frac{V_a}{R_1} = \frac{V_a}{R_f} - \frac{V_o}{R_f}$$

$$\frac{V_1}{R_1} + \frac{V_o}{R_f} = V_a \left[\frac{1}{R_1} + \frac{1}{R_f} \right] \quad \text{--- (1)}$$

Apply KCL at node 'b'

$$\frac{V_2 - V_b}{R_2} = \frac{V_b}{R_f}$$

$$\frac{V_2}{R_2} = V_b \left[\frac{1}{R_2} + \frac{1}{R_f} \right]$$

$$\Rightarrow V_b = \frac{V_2}{R_2 \left[\frac{1}{R_2} + \frac{1}{R_f} \right]} \quad \text{--- (2)}$$

According to virtual ground concept, $V_o = V_b$.

∴ From eqns (1) & (2), we get,

$$\frac{V_1}{R_1} + \frac{V_0}{R_f} = \frac{V_2}{R \left[\frac{1}{R_1} + \frac{1}{R_f} \right]} \left[\frac{1}{R_1} + \cancel{\frac{1}{R_f}} \right]$$

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_0}{R_f} = \frac{V_2}{R_1}$$

$$\Rightarrow \frac{V_0}{R_f} = \frac{V_2 - V_1}{R_1}$$

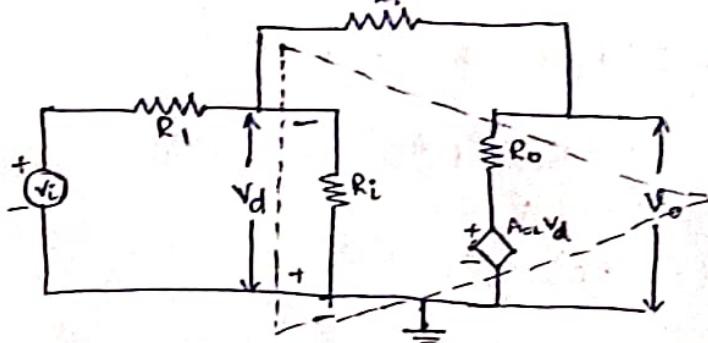
$$\Rightarrow V_0 = \frac{R_f}{R_1} (V_2 - V_1)$$

Such a circuit is very useful in detecting very small difference in signals, since the gain R_f/R_1 can be chosen to be very large.

For example, if $R_f = 100R_1$, then a small difference ($V_2 - V_1$) is amplified 100 times.

If all resistors are equal, then it acts as subtraction.

Practical Inverting amplifier :-



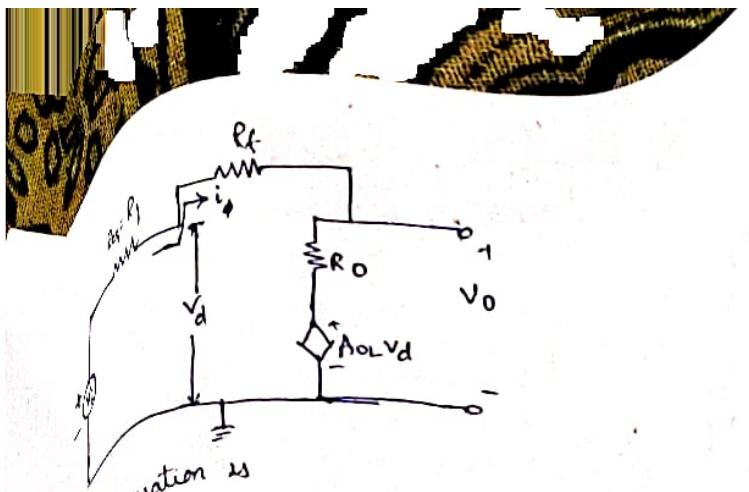
The resistors R_1 & R_i are parallel. As per op-amp characteristics R_i is very high.

$$\therefore \frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_i} = \frac{R_1 + R_i}{R_1 R_i}$$

$$R_{eq} = \frac{R_1 R_i}{(R_1 + R_i)} \quad \therefore R_1 + R_i \approx R_i, \text{ since } R_i \text{ is very high.}$$

$$\therefore R_{eq} = R_1$$

∴ The above circuit is simplified as below.



adapt loop equation 2s

$$v_o = iR_o + A_{OL}v_d \quad \text{--- (1)}$$

$v_d + iR_f + v_o = 0 \quad \text{--- (2)}$

From equation (1), $v_d = \frac{v_o - iR_o}{A_{OL}}$

sub. v_d value in eqn (2)

$$\frac{v_o - iR_o}{A_{OL}} + iR_f + v_o = 0$$

$$\Rightarrow v_o - iR_o + i \cdot R_f \cdot A_{OL} + v_o A_{OL} = 0$$

$$\Rightarrow v_o [1 + A_{OL}] + i [A_{OL}R_f - R_o] = 0$$

$$\Rightarrow v_o (1 + A_{OL}) = i (R_o - R_f \cdot A_{OL}) \quad \text{--- (3)}$$

Now the KVL loop equation gives,

$$v_i = i(R_1 + R_f) + v_o \quad \text{--- (4)}$$

From eqn (3), we get,

$$i = \frac{v_o (1 + A_{OL})}{(R_o - R_f \cdot A_{OL})}$$

Sub. 'i' value in eqn (4), we get

$$v_i = \frac{v_o (1 + A_{OL})}{(R_o - R_f \cdot A_{OL})} (R_1 + R_f) + v_o$$

$$v_i = v_o \left[\frac{(1 + A_{OL})(R_1 + R_f)}{(R_o - R_f \cdot A_{OL})} + 1 \right] = v_o \left[\frac{(1 + A_{OL})(R_1 + R_f)}{R_o - R_f \cdot A_{OL}} + 1 \right]$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{R_o - R_f \cdot A_{OL}}{(1 + A_{OL})(R_f + R_i) + R_o + R_f \cdot A_{OL}}$$

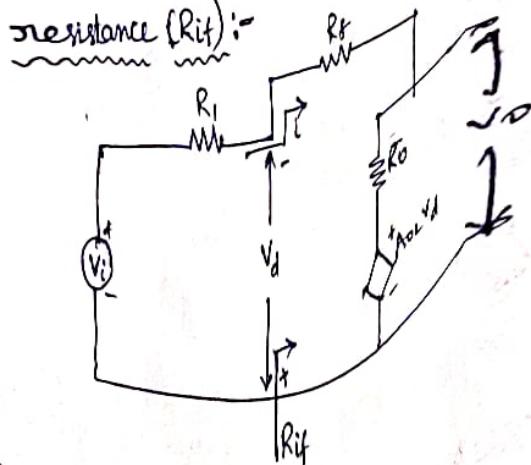
$$\Rightarrow A_{CL} = \frac{R_o - R_f \cdot A_{OL}}{R_f + R_i + A_{OL} \cdot R_i + A_{OL} \cdot R_f + R_o - R_f \cdot A_{OL}}$$

$$\Rightarrow A_{CL} = \frac{R_o - R_f \cdot A_{OL}}{R_o + R_f + R_i (1 + A_{OL})}$$

\therefore the practical gain of an inverting amplifier is,

$$A_{CL} = \frac{R_o - R_f \cdot A_{OL}}{R_o + R_f + R_i (1 + A_{OL})}$$

Input resistance (R_{if}):



Input resistance, $R_{if} = \frac{V_d}{i}$

The loop

equation is,

$$V_d + i(R_f + R_o) + A_{OL}V_d = 0$$

$$\Rightarrow V_d(1 + A_{OL}) + i(R_f + R_o) = 0$$

$$\Rightarrow V_d(1 + A_{OL}) = -i(R_f + R_o)$$

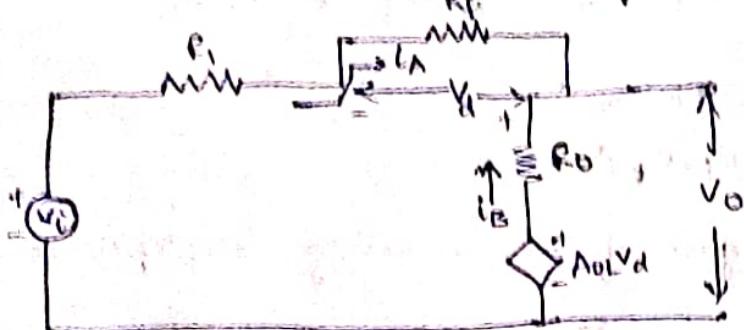
$$\Rightarrow \frac{V_d}{i} = -\frac{(R_f + R_o)}{(1 + A_{OL})}$$

P. ... n.o. 1

Output resistance (R_{op}):

The op-amp impedance ' R_{op} ' is calculated from the open circuit output voltage ' V_{oc} ' and short circuit current ' I_{sc} '.

The equivalent circuit for calculating ' R_{op} ' is,



Under short circuit conditions, at o/p,

$$i_A = \frac{V_i}{R_f + R_f} \quad \text{--- (1)}$$

$$i_B = \frac{A_{OL} V_d}{R_o} \quad \text{--- (2)}$$

$$V_d = -i_A R_f \quad \text{--- (3)}$$

Substituting (3) in (2) we get,

$$i_B = \frac{A_{OL} (-i_A \cdot R_f)}{R_o}$$

$$i_{sc} = i_A + i_B$$

$$\Rightarrow i_{sc} = \frac{V_i}{R_f + R_f} - \frac{A_{OL} \cdot i_A \cdot R_f}{R_o}$$

$$= \frac{V_i \cdot R_o - (R_f + R_f) (A_{OL} \cdot i_A \cdot R_f)}{(R_f + R_f) \cdot R_o}$$

$$\text{From eqn (1), } V_i = i_A (R_f + R_f)$$

$$i_{sc} = \frac{V_i \cdot R_o - V_i \cdot A_{OL} \cdot R_f}{(R_f + R_f) \cdot R_o}$$

$$\Rightarrow I_{BE} = \frac{V_i (R_0 + A_{OL} R_f)}{R_0 (R_1 + R_f)} \quad \text{--- (4)}$$

Since, $I_{BE} = \frac{V_{BE}}{R_{BE}}$

$$\Rightarrow R_{OF} = \frac{V_{BE}}{I_{BE}} \quad \text{--- (5)}$$

$$A_{CL} = \frac{V_{OC}}{V_i} \quad \text{if } L.C.T., \quad A_{CL} = \frac{R_0 \cdot R_f \cdot A_{OL}}{R_0 + R_1 + R_f + R_1 A_{OL}}$$

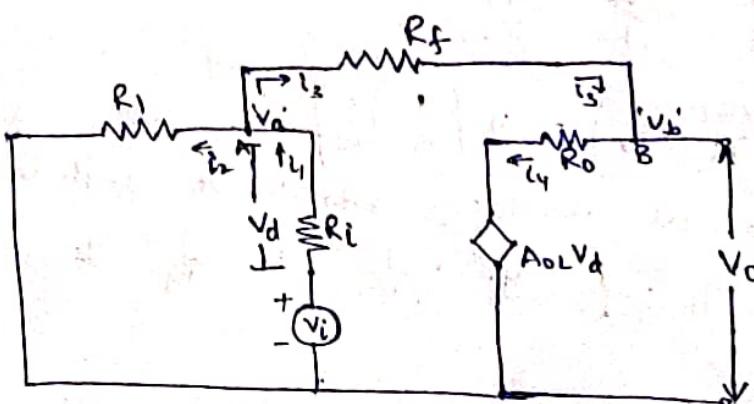
$$\Rightarrow V_{OC} = \frac{V_i (R_0 - R_f \cdot A_{OL})}{R_0 + R_1 + R_f + R_1 A_{OL}} \quad \text{--- (6)}$$

Sub. eqn (4) & (6) in eqn (1) we get,

$$R_{OF} = \frac{\frac{V_i (R_0 - R_f \cdot A_{OL})}{R_0 + R_1 + R_f + R_1 (1 + A_{OL})}}{\frac{V_i (R_0 - R_f \cdot A_{OL})}{R_0 (R_1 + R_f)}}$$

$$\Rightarrow R_{OF} = \frac{R_0 (R_1 + R_f)}{R_0 + R_f + R_1 (1 + A_{OL})}$$

Practical Non-inverting amplifier :-



$$V_a = V_i + V_d \Rightarrow V_d = V_a - V_i$$

$$V_b = V_o$$

Apply KCL at node A:

$$I_1 = I_2 + I_3$$

$$\Rightarrow \frac{V_C - V_A}{R_1} = \frac{V_A}{R_1} + \frac{V_A - V_B}{R_2}$$

$$\therefore \frac{(V_A - V)}{R_1} = \frac{V_A}{R_1} + \frac{V_A - V_B}{R_2}$$

$$\therefore \frac{V_A}{R_1} = \frac{V_C - V}{R_1} + \frac{V_C - V_B - V_B}{R_2}$$

$$\therefore \frac{V_A}{R_1} = V_C + \frac{V_C}{R_1} - \frac{V_B}{R_1} - \frac{V_B}{R_2} - \frac{V_B}{R_3}$$

$$\therefore \frac{V_A}{R_1} = V_C \left(1 + \frac{1}{R_1} \right) - V_B \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) \quad (1)$$

Apply KCL at node B:

$$I_2 = I_3$$

$$\frac{V_B - V_A}{R_2} = \frac{V_B - V_C - V_A}{R_3}$$

$$\frac{V_B - V_A}{R_2} = \frac{V_B - V_C - V_A}{R_3}$$

$$\frac{V_B}{R_2} + \frac{V_A}{R_1} = \frac{V_B}{R_3} + \frac{V_C - V_A}{R_1}$$

$$\frac{V_B}{R_2} + V_A \left(\frac{1}{R_1} + \frac{1}{R_1} \right) = V_B \left(\frac{1}{R_3} + \frac{1}{R_1} \right) \quad (2)$$

For simplicity, let us consider admittance instead of resistance,
then $\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} = Y_1 + Y_2 + Y_3 = Y_A$

eqn(1) becomes:

$$V_A (Y_A) = V_C (Y_1 + Y_2) + V_B (Y_2 + Y_3 + Y_1) = V_B \quad (3)$$

eqn(2) becomes:

$$V_B (Y_1 + Y_2 + Y_3 + Y_1) = V_B (Y_1 + Y_3) = 0 \quad (4)$$

$$\text{From eqn ④, } v_d = \frac{v_0 - v_i(y_1 + y_f)}{y_1 + y_f + y_0} \quad \text{⑤}$$

sub eqn ⑤ in eqn ③ we get,

$$v_0(y_0 + y_1) = v_i y_f + \left(\frac{v_0 y_f - v_i(y_1 + y_f)}{y_1 + y_f + y_0} \right) \cdot (A_{0L} y_0 + y_f)$$

$$\Rightarrow v_0(y_0 + y_1) = \frac{v_i y_f (y_0 + y_1 + y_f) + [v_0 y_f - v_i(y_1 + y_f)](A_{0L} y_0 + y_f)}{(y_1 + y_f + y_0)}$$

$$\Rightarrow v_0(y_0 + y_1)(y_0 + y_1 + y_f) = v_i y_f (y_1 + y_f + y_0) + v_0 y_f (A_{0L} y_0 + y_f) = v_i(y_1 + y_f)(A_{0L} y_0 + y_f)$$

$$\Rightarrow v_0 \left[y_0 y_f + y_0 y_1 + y_0 y_f + y_1 y_f + y_1 y_f + y_0^2 \right] = v_i \left[y_1 y_f + y_0 y_f + y_0^2 \right] + v_0 \left[y_0 y_f A_{0L} + y_0^2 \right] \\ = v_i \left[y_1 y_f + y_0 y_f + y_0^2 \right]$$

$$\Rightarrow v_0 \left[y_0 y_f + y_0 y_1 + y_0 y_f + y_1 y_f + y_1 y_f + y_0^2 - y_1 y_f A_{0L} \right] = v_i \left[y_1 y_f + y_0 y_f + y_0^2 - y_1 y_f A_{0L} \right]$$

$$\Rightarrow \frac{v_0}{v_i} = \frac{y_1 y_f + y_0 y_f + y_0^2}{y_0 y_f + y_0 y_1 + y_0 y_f + y_1 y_f + y_1 y_f + y_0^2 - y_1 y_f A_{0L}}$$

$$\Rightarrow \frac{v_0}{v_i} = \frac{y_1 y_f + y_0 y_f + y_0^2}{y_0 y_f (1 - A_{0L}) + (y_0 + y_1)(y_1 + y_f)}$$

~~If $A_{0L} \rightarrow \infty$~~ the above eqn can be written as

$$A_{0L} = \frac{y_1 y_f + y_0 y_f + y_0^2}{y_0 y_f (1 - A_{0L})}$$

$$A_{0L} = \frac{y_1 y_f + y_0 y_f + y_0^2}{y_0 y_f (A_{0L} - 1)}$$

$$A_{0L} = \frac{y_1 y_f + y_0 y_f + y_0^2}{y_0 y_f (A_{0L} - 1)}$$

$$A_{0L} = \frac{y_1 y_f + y_0 y_f + y_0^2}{y_0 y_f (A_{0L} - 1)}$$

$$(y_1 y_f + y_0 y_f + y_0^2)$$

$$\Rightarrow A_{0L} = \frac{y_1 y_f + y_0 y_f + y_0^2}{y_0 y_f} = 1 + \frac{y_1 y_f}{y_0 y_f} = 1 + \frac{y_1}{y_0}$$

Characteristics of op-amp :-

DC Characteristics of op-amp :-

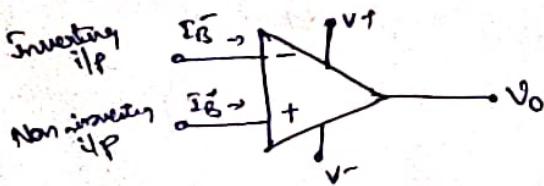
An ideal op-amp draws no current from the source, and its response is also independent of temp. However, a real op-amp does not act this way. A real op-amp also shifts its operation with temperature.

The DC characteristics will add the various components to the dc op voltage. They are-

- (i) Input Bias current.
 - (ii) Input offset current.
 - (iii) Input offset voltage.
 - (iv) Thermal drift.
- (i) Input Bias current :-

We know that, an ideal op-amp draws no current from the input terminals, but practically input terminals conduct a small value of current to bias the i/p transistor.

The i/p of an op-amp is a differential amplifier which is made up of BJT (BiFET). The i/p transistor must be biased into their linear region by supplying current with external circuit.



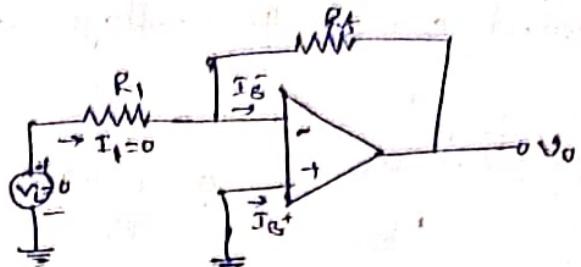
The base currents entering into inverting terminal is I_B^- and non-inverting terminal is I_B^+ .

(Both I_B^- and I_B^+ are not same due to the internal imbalances between two inputs.)

the "input bias current" (I_B) is an average value of the base currents entering into the terminals of an op-amp.

$$\therefore I_B = \frac{I_B^+ + I_B^-}{2}$$

consider the basic inverting amplifier as shown in below.

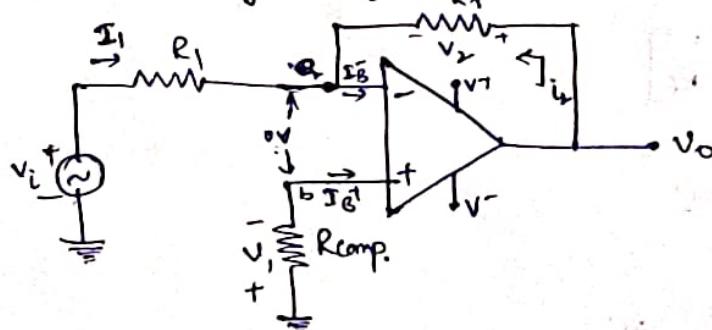


$$N.K \pi, v_o = -\frac{R_f}{R_1} R_i v_i$$

$$\text{if } v_i = 0, \text{ then } v_o = 0$$

$$\text{But due to } I_B^-, v_o = -(I_B^-) R_f$$

Generally for an op-amp bias current is 500nA. To compensate the effect of the o/p bias current, a compensation resistor "Rcomp" has to be added between the non-inverting terminal and ground as shown in below. the current I_B^+ flowing through the resistor "Rcomp" will develop a voltage of v_1 across across it.



Apply KVL, we get,

$$-v_1 + 0 + v_2 - v_o = 0$$

$$v_o = v_2 - v_1$$

By properly selecting value of R_{comp} , v_1 can be cancelled with v_2 and the o/p v_o will be zero.

the value of R_{comp} is said to be derived as,

Compensation:

$$V_i = I_B^+ R_{comp}$$

$$I_B^+ = \frac{V_i}{R_{comp}}$$

As per virtual ground concept, the voltage at node "a"

so, with $V_i = 0$, we get,

$$I_1 = \frac{V_i - V_a}{R_1} = \frac{0 - (-V)}{R_1}$$

$$\Rightarrow I_1 = \frac{V_1}{R_1}$$

Similarly, $I_2 = \frac{V_1}{R_f}$

for compensation, $V_o = 0$

$$V_o = V_2 - V_1 = 0$$

$$\Rightarrow V_2 = V_1$$

$$\therefore I_2 = \frac{V_1}{R_f}$$

Apply KCL at node "a", we get

$$I_B^- = I_1 + I_2$$

$$I_B^- = \frac{V_1}{R_1} + \frac{V_1}{R_f}$$

$$I_B^- = V_1 \left[\frac{1}{R_1} + \frac{1}{R_f} \right]$$

We know that $I_B^+ = \frac{V_1}{R_{comp}}$

Assuming $I_B^- = I_B^+$

$$V_1 \left(\frac{R_1 + R_f}{R_1 R_f} \right) = \frac{V_1}{R_{comp}}$$

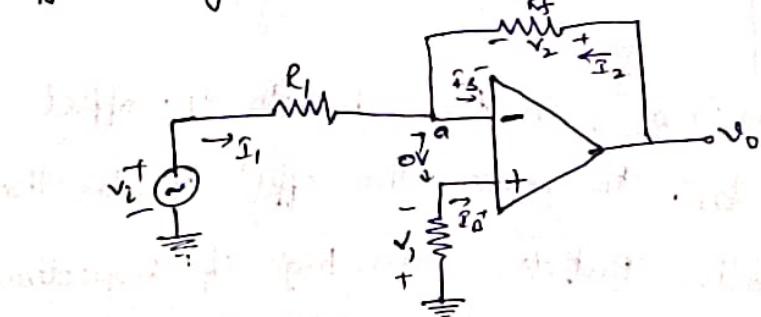
$$\Rightarrow R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$$

$$\Rightarrow R_{comp} = R_1 \parallel R_f$$

Input offset current (I_{os}):-

The input bias current compensation works only if $I_B^+ = I_B^-$. As no two transistors are identical, there will always be some difference between the I_B^+ & I_B^- . This difference is called the i/p offset current (I_{os}). $I_{os} = |I_B^+ - I_B^-|$

Ideally its value is within the range of 200 nA. Even with the bias current compensation, offset current will produce an o/p voltage when the i/p voltage v_i is zero.



$$V_1 = I_B^+ \cdot R_{comp}$$

$$I_1 = \frac{V_1}{R_1} \quad \text{--- (1)}$$

Apply KCL at node 'a'

$$I_1 + I_2 = I_B^-$$

$$I_2 = I_B^- - I_1 \quad \text{--- (2)}$$

Apply KVL, we get

$$V_0 + V_2 - 0 - V_1 = 0$$

$$V_0 = V_2 - V_1$$

$$= I_2 \cdot R_f - I_B^+ \cdot R_{comp}$$

~~From (2)~~

$$\Rightarrow V_0 = (I_B^- - I_1) R_f - I_B^- \cdot R_{comp} \quad [\because \text{from (2)}]$$

$$\Rightarrow V_0 = I_B^- \cdot R_f - I_1 \cdot R_f - I_B^- \cdot R_{comp}$$

$$\Rightarrow V_0 = I_B^- \cdot R_f - \frac{V_1}{R_1} R_f - I_B^- \cdot R_{comp} \quad [\because \text{from (1)}]$$

$$\Rightarrow V_o = I_B^- R_f - I_B^+ \cdot R_{cap} \cdot \frac{R_f}{R_1} - I_B^+ \cdot R_{cap} \quad \left\{ \text{if } V_i = I_B^+ \cdot R_{cap} \right\}$$

W.K.T. $R_{cap} = \frac{R_1 \cdot R_f}{R_1 + R_f}$

$$\Rightarrow V_o = I_B^- R_f - I_B^+ \left(\frac{R_1 R_f}{R_1 + R_f} \right) \left(\frac{R_f}{R_1} + 1 \right)$$

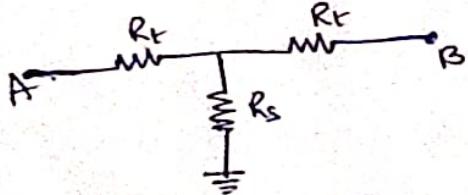
$$\Rightarrow V_o = I_B^- R_f - I_B^+ \left(\frac{R_f}{R_1 + R_f} \right) \left(\frac{R_1 + R_f}{R_1} \right)$$

$$\Rightarrow V_o = (I_B^- - I_B^+) R_f$$

$$\Rightarrow V_o = I_{os} R_f$$

Ideally o/p voltage has to be zero, but due to the offset current (I_{os}) the o/p is $R_f \cdot I_{os}$. To reduce the effect of I_{os} the feedback resistor must be small. But, to obtain high o/p impedance R_1 must be large. If R_1 is large, R_f must be large to maintain the required gain.

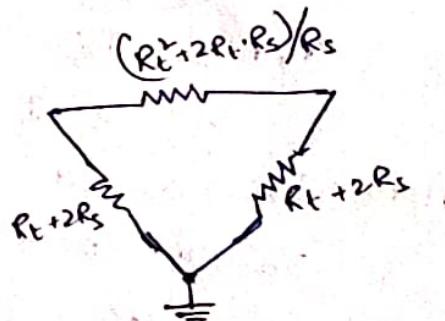
The T-fb n/w is a good solution as it allow large fb resistance while keeping the resistance to ground



$$R_f = \frac{R_t^2 + 2 \cdot R_f \cdot R_s}{R_s}$$

$$R_t \ll \frac{R_E}{2}$$

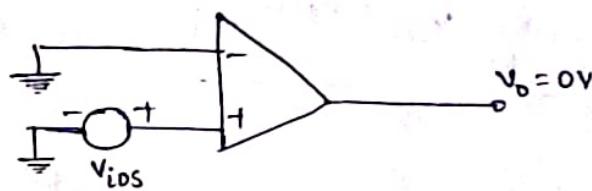
$$R_s = \frac{R_t^2}{R_f - 2R_E}$$



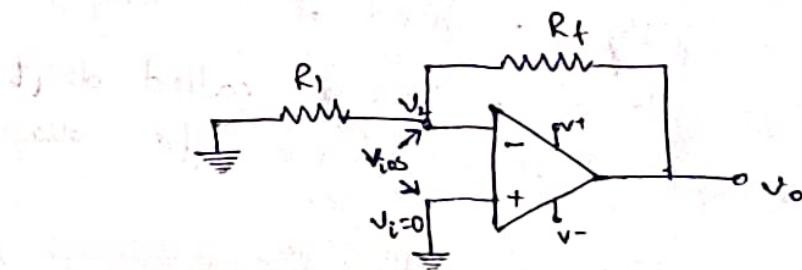
(iii) Input offset voltage :- (V_{ios})

Even after many compensation techniques, the o/p voltage is not zero with zero i/p. This is due to imbalances internally.

A small voltage is applied at the i/p terminal to make the o/p zero. This voltage is called i/p offset voltage " V_{ios} ". This voltage is required to be applied at the i/p for making o/p voltage to zero as shown in below.



Now let us consider the ckt,



$$V_o = \left(\frac{R_f}{R_1 + R_f} \right) V_1 \quad [\because \text{voltage divider}]$$

$$\Rightarrow V_o = \left(\frac{R_1 + R_f}{R_1} \right) V_1$$

$$\Rightarrow V_o = \left(1 + \frac{R_f}{R_1} \right) V_1$$

$$V_{ios} = |V_1 - V_o| \quad \& \quad V_1 = 0$$

$$\Rightarrow V_{ios} = V_o$$

$$\therefore V_o = \left(1 + \frac{R_f}{R_1} \right) V_{ios}$$

Total o/p offset voltage (V_{oT}) :-

i/p offset voltage produced the total output offset voltage is the offset voltage at the o/p due to the i/p bias current(I_B)

i/p offset voltage (V_{ios}) :-

$$V_{oT} = V_o(\text{due to } I_B) + V_o(\text{due to } V_{ios})$$

$$= R_f I_B + \left(1 + \frac{R_f}{R_i}\right) V_{ios}$$

with $R_{comp}, I_B \rightarrow I_{os}$

$$\therefore V_{oT} = \left(1 + \frac{R_f}{R_i}\right) V_{ios} + R_f I_{os}$$

(iv) Thermal Drift :-

Bias current, offset current & offset voltage change with temperature. A circuit carefully designed at 25°C may not remain so when the temp. raises to 35°C . This is called drift. Often, offset current drift is expressed in $\text{nA}/^\circ\text{C}$ and offset voltage drift in $\text{mV}/^\circ\text{C}$.

There are very few ckt techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temp.

The average rate of change of i/p offset voltage per unit change in temp. is called thermal voltage drift.

$$\frac{\Delta V_{io}}{\Delta T} \rightarrow \text{mV}/^\circ\text{C}$$

$$\frac{\Delta I_{io}}{\Delta T} \rightarrow \text{thermal current drift, } \text{nA}/^\circ\text{C}$$

A.C. Characteristics

The important A.C. characteristics of an op-amp are :-

- (i) Frequency response
- (ii) slew rate.

(i) Frequency response :-

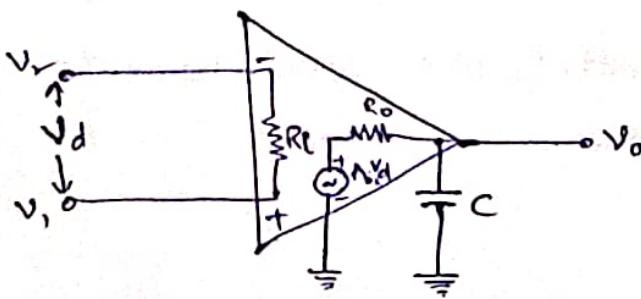
An op-amp has infinite bandwidth in ideal mode. As the frequency increases the gain decreases. The drop in gain with rise in frequency is due to capacitive effect.

- Two major sources are responsible for capacitive effects on op-amp
- a) Physical characteristics of semiconductor devices. Op-amps are built using BJTs & FET which contain junction capacitors.
- b) The internal construction of op-amp also contributes to the presence of capacitance.

In op-amp, no. of transistors, resistors & capacitors etc are integrated on the same substrate. If two transistors act as insulator & helps in separating the components. If two conducting paths are separated by an insulator it acts as capacitor. Due to various components no. of such capacitances are formed.

The cumulative effect of these capacitors due to char. of semiconductor devices and internal construction of op-amp causes the gain to decrease as the frequency increases.

- To obtain the "frequency response" consider high frequency model of op-amp with a capacitor 'C' at o/p.



Let $-jX_C$ be the capacitive reactance due to capacitor C :

Using voltage divider rule,

$$V_o = \frac{-jX_C}{R_o - jX_C} (A_{OL} V_d)$$

W.K.T. $-j = V_j$ & $X_C = \frac{1}{2\pi f C}$

$$\therefore V_o = \frac{\frac{1}{j2\pi f C}}{R_o + \frac{1}{j2\pi f C}} (A_{OL} V_d)$$

$$\Rightarrow V_o = \frac{\frac{1}{j2\pi f C}}{\frac{jR_o 2\pi f C + 1}{j2\pi f C}} \times (A_{OL} V_d)$$

$$\Rightarrow V_o = \frac{A_{OL} \cdot V_d}{1 + j2\pi f R_o C}$$

Hence, the open loop voltage gain as a function of frequency is,

$$\text{or } A_{OL}(f) = \frac{V_o}{V_d} = \frac{A_{OL}}{1 + j2\pi f R_o C}$$

Let $f_0 = \frac{1}{j2\pi R_o C}$, then

$$A_{OL}(f) = \frac{A_{OL}}{1 + j(f/f_0)}$$

Where, $A_{OL}(f) \rightarrow$ open loop gain as a function of frequency

$A_{OL} \rightarrow$ open gain of op-amp at 0 Hz.

$f \rightarrow$ operating frequency

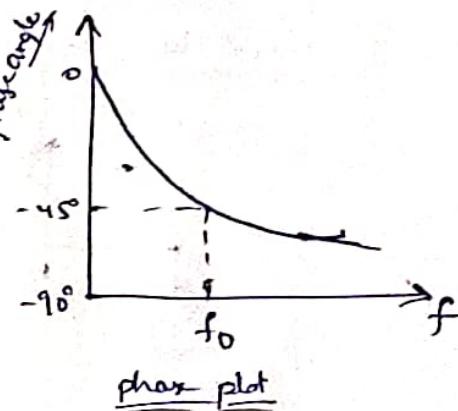
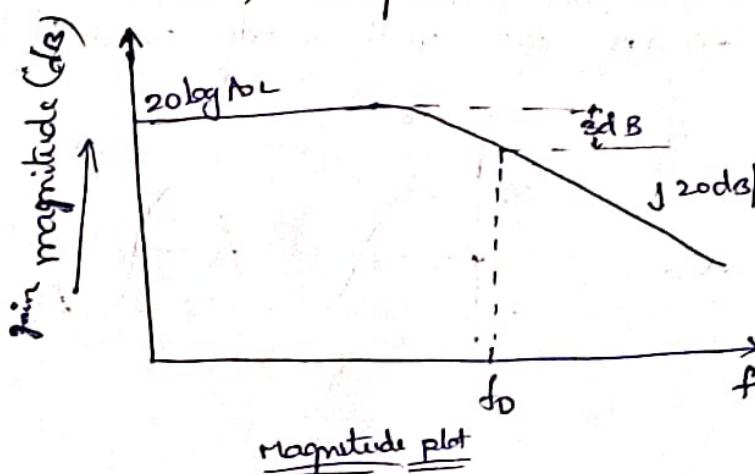
$f_0 \rightarrow$ break frequency of the op-amp

f_0 (break frequency) depends on the value of 'c' and o/p resistance R_o .
∴ f_0 is fixed for a given op-amp.

The open loop gain magnitude is, $|A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1+(f/f_0)^2}}$

phase angle is, $\phi(f) = -\tan^{-1}(\frac{f}{f_0})$

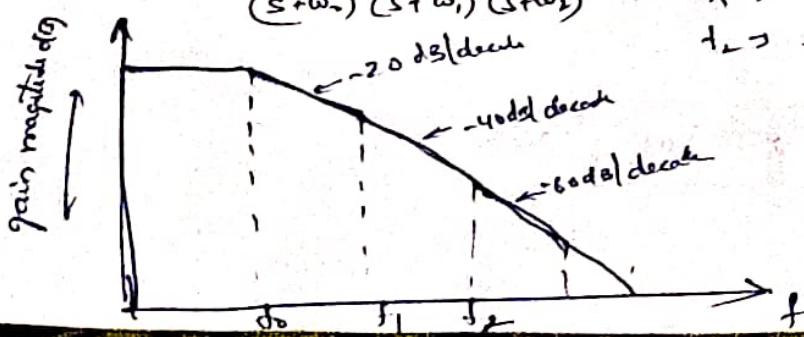
- For frequencies $f \ll f_0$, magnitude of the gain is $20 \log(A_{OL})$ dB.
- At $f = f_0$, the gain is 3dB down from the dc value of A_{OL} in dB. This frequency is called corner frequency.
- For $f \gg f_0$, the gain decreases at the rate of -20dB per decade.



- There is only single change in slope of magnitude plot called single break frequency due to one capacitor.
- However in practical op-amp there are no. of stages. Each stage introduces capacitive component. Thus there are no. of different break frequencies.

$$A_{OL}(f) = \frac{A_{OL}}{\left[1 + j\frac{f}{f_0}\right] \left[1 + j\frac{f}{f_1}\right] \left[1 + j\frac{f}{f_2}\right]} \dots \quad \text{where } \omega_0 f_0 < f_1 < f_2$$

$$\Rightarrow A_{OL}(f) = \frac{A_{OL} \omega_0 \omega_1 \omega_2}{(s + \omega_0)(s + \omega_1)(s + \omega_2)} \quad \begin{aligned} f_0 &\rightarrow -20 \text{ dB/decade} \\ f_1 &\rightarrow -40 \text{ dB/decade} \\ f_2 &\rightarrow -60 \text{ dB/decade} \end{aligned}$$



(ii) Slew rate :-

The slew rate is defined as the maximum rate of change of output voltage w.r.t. time, usually specified in V/μs.

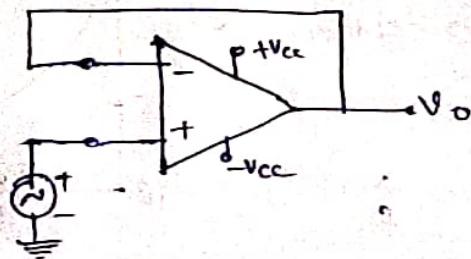
Mathematically, it is specified as,

$$S = \frac{dV_o}{dt} \Big|_{\text{max}}$$

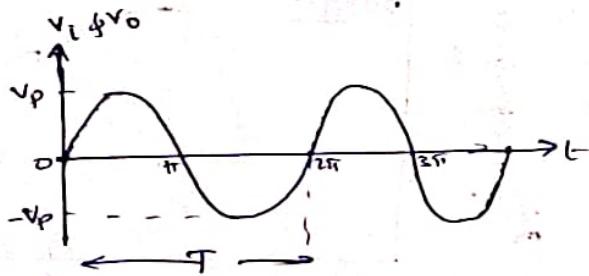
→ Higher the value of slew rate, less is the distortion and better is the performance.

Slew rate equation :-

Consider unity gain op-amp circuit with purely sinusoidal input. The o/p must be same as i/p.



(voltage follower)



$$V_{in} = V_m \sin \omega t \quad \& \quad V_o = V_m \sin \omega t$$

$$\therefore \frac{dV_o}{dt} = V_m (\omega \cos \omega t)$$

$$\text{But } S = \text{slew rate} = \frac{dV_o}{dt} \Big|_{\text{max}}$$

∴ the max. value of $\omega \cos \omega t = 1$.

$$\therefore S = \frac{dV_o}{dt} \Big|_{\text{max}} = V_m \omega$$

$$\Rightarrow S = 2\pi f V_m \quad \text{V/sec}$$

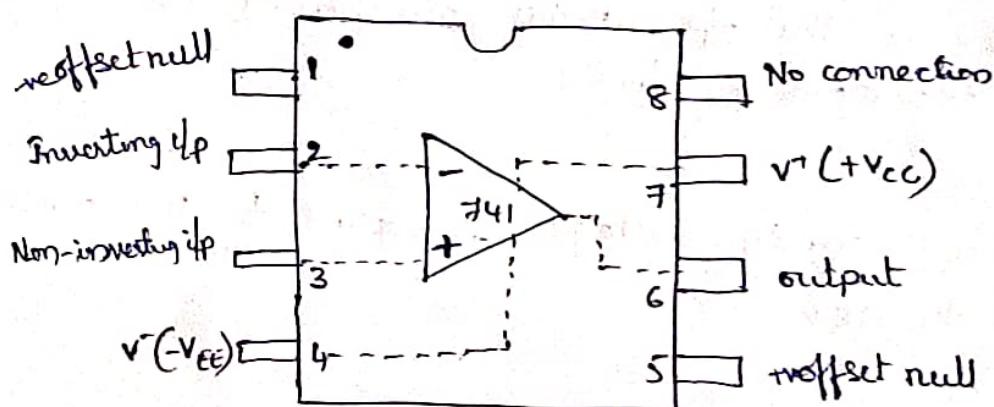
IC 741 op-amp:-

A popular ^{IC} version of op-amp is 741. The manufacturer of 741 is Fairchild Semiconductor. It is available in all three packages i.e., 8-pin metal can, 10-pin flat pack, 8-pin DIP, 14-pin DIP.

Features of 741 op-amp:-

- High input voltage range.
- Offset voltage null capability
- Short circuit protection
- No frequency compensation required (internal freq. compensation).
- Excellent temp. stability.
- Large common mode to differential voltage range.
- No latch up.

IC 741 pin diagram and description:-



The IC 741 is 8-pin IC, available in DIP (dual in line package) as shown in above figure.

Pin-1: (Offset Null) :-

It is used to nullify the offset voltage at the ~~inverting~~ inverting terminal.

Pin-2 (Inverting input) :-

All the i/p signals at this pin will be inverted at output pin-6.

Pin-3 (Non-inverting i/p) :-

All the i/p signals at this pin will be processed normally without inversion.

Pin-4 (-V_{EE}) :-

The negative voltage supply is applied to this pin. Range is from -5V to -18V.

Pin-5 (Offset null) :-

It is used to nullify the offset voltage at the non-inverting terminal.

Pin-6 (Output) :-

We can observe the o/p. at this pin either inverting or non-inverting for corresponding i/p.

Pin-7 (+V_{CC}) :-

The positive supply voltage is applied to this terminal. Range is from +5V to +18V.

Pin-8 (No connection) :-

This pin is not connected.

Applications of op-amp: An op-amp has many applications.

Linear applications :- Adder, subtractor, voltage to current converter, I to V converters, Instrumentation amplifier, power amplifiers etc.

Non-linear applications :- Rectifier, peak detector, clipper, clammer, sample & hold ckt, multipliers etc.

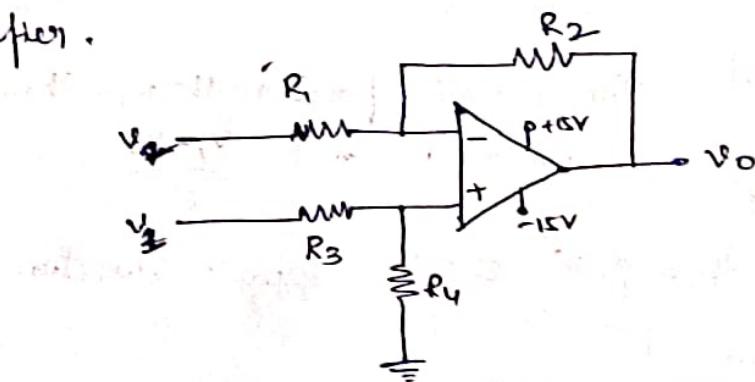
Instrumentation amplifier :-

In many industrial applications, some consumer applications it is required to control and measure some physical quantities like temperature, humidity, water flow, light intensity etc.

These quantities are usually measured with the help of transducers.

The o/p of the transducer has to be amplified in order to drive it to the indicator or display.

The instrumentation amplifier does this amplification work. It is also called as data amplifier and is basically a difference amplifier.



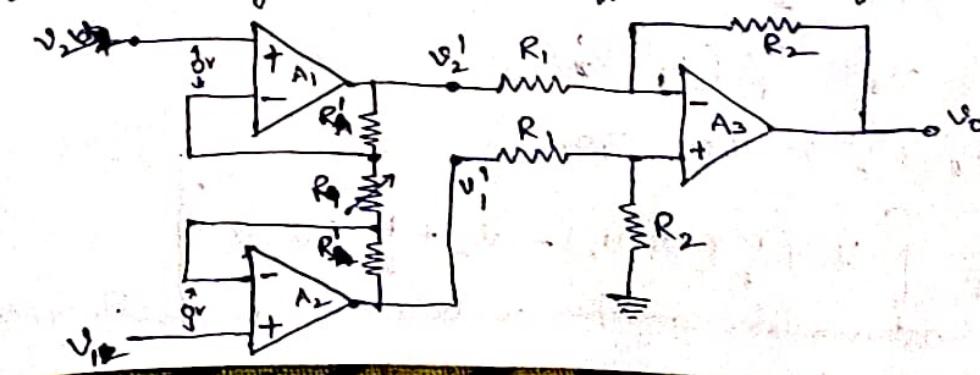
W.K.T., for basic differential amplifier,

$$V_0 = \frac{R_2}{R_1} (V_1 - V_2)$$

but here it is possible, when $\frac{R_1}{R_3} = \frac{R_3}{R_4}$.

If $R_1 = R_2 = 1k$ & $R_3 = R_4 = 100k\Omega$, then $\frac{R_1}{R_3} = \frac{R_3}{R_4}$

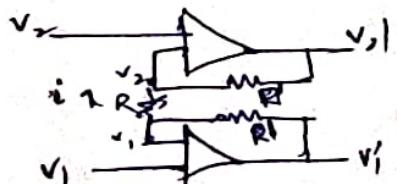
But, the impedance on -ve terminal of the op-amp is low which leads to loading effect. In order to avoid the loading effect, we use high resistive buffer ckt. before the i/f as shown in below



The op-amps A_1 & A_2 have differential i/p voltage as zero. For $v_1 = v_2$, i.e., under common mode condition, the voltage across R' will be zero. As no current flows through R & R' the non-inverting amplifier A_1 acts as voltage follower, so output $v'_1 = v_2$. similarly A_2 acts as voltage follower so $v'_2 = v_1$.

If $v_1 \neq v_2$, then there will be a current 'i' through R & R' , and $(v'_1 - v'_2) > (v_1 - v_2)$. This circuit will have more differential gain and CMRR, when compared to single op-amp ckt.

Output of instrumentation amplifier :-



The current flowing through the resistor R' is $i = \frac{v_1 - v_2}{R}$

As the current 'i' flows through R' . But, in opposite direction.

$$v'_1 = v_1 - (-i)R'$$

$$\boxed{v'_1 = v_1 + \left(\frac{v_1 - v_2}{R}\right) R'} \Rightarrow v'_1 = v_1 + -v_1 + v_2$$

$$v'_2 = v_2 - i \cdot R'$$

$$\Rightarrow \boxed{v'_2 = v_2 - \left(\frac{v_1 - v_2}{R}\right) R'}$$

Analysis of op-amp A_3 :

Since op-amp A_3 is a differential amplifier

$$\text{Then } v_o = \frac{R_2}{R_1} (v'_1 - v'_2)$$

substitute v'_1 & v'_2 in above eqn.

$$\therefore v_o = \frac{R_2}{R_1} \left\{ v_1 + \frac{R'}{R} (v_1 - v_2) - v_2 + \frac{R'}{R} (v_1 - v_2) \right\}$$

The difference gain of this instrumentation amplifier can be varied by varying variable resistor R .

$$\Rightarrow V_o = \frac{R_2}{R_1} \left[(V_1 - V_2) + \frac{2R_1}{R} (V_1 - V_2) \right]$$

$$\Rightarrow V_o = \frac{R_2}{R_1} \left[\left(1 + \frac{2R_1}{R} \right) (V_1 - V_2) \right]$$

The gain of instrumentation amplifier = $\frac{R_2}{R_1} \left(1 + \frac{2R_1}{R} \right)$.

The difference gain of this instrumentation amplifier can be varied by using variable resistor "R".

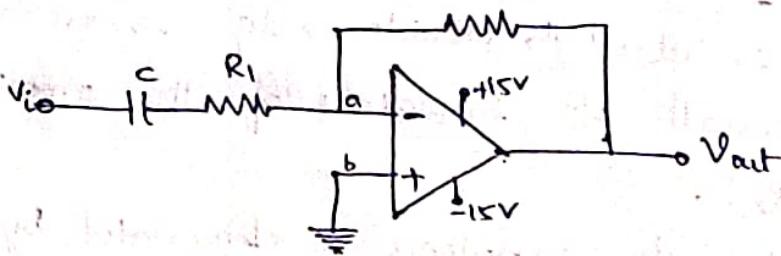
A.C. Amplifier :-

The operational amplifier works for both AC & DC signals.

If ac frequency response of an op-amp is to be analysed (Q) if an AC sig is superimposed on to a DC sig, it is ~~never~~ necessary to block DC components. This can be done by the AC amplifier.

An AC amplifier is an electronic ckt which blocks DC components and amplifies the AC signals. AC amplifiers are inverting and non-inverting type.

Inverting AC amplifier :-



The capacitor 'C' blocks the DC component of the input and together the combination of R_1 & C sets the lower 3dB frequency of amplifier.

$$\text{From fig: } Z_1 = R_1 + \frac{1}{sc} \quad [\because \frac{1}{sc} = \text{Capacitor reactance}]$$

$$\Rightarrow Z_1 = \frac{sR_1C + 1}{sc}$$

$W.K.T.$ for inverting amplifier,

$$V_o = \frac{R_f}{Z_1} \cdot V_i$$

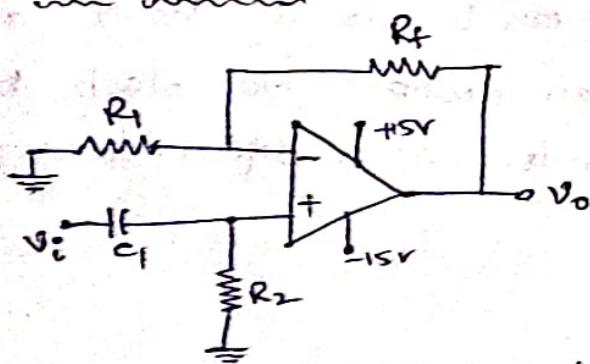
$$\Rightarrow V_o = \frac{-R_f \cdot S_C}{1 + R_i \cdot S_C} \cdot V_i$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{-R_f \cdot S_C}{1 + R_i \cdot S_C}$$

$$\Rightarrow A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_i} \left[\frac{-R_f \cdot S_C}{R_i \cdot R_f \left[\frac{1}{R_i C} + S \right]} \right]$$

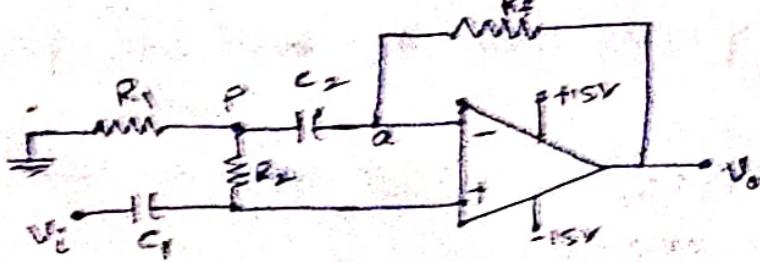
$$\Rightarrow A_{CL} = \frac{-R_f}{R_i} \left[\frac{S}{S + \frac{1}{R_i C}} \right]$$

Non-inverting AC amplifier:-



Here a resistor R_2 is added to provide a dc return to ground. But, R_2 reduces the overall input impedance of the amplifier (which is approximately becomes R_i).

This problem of low ip impedance is eliminated by connecting a capacitor C_2 as shown in below.



' C_2 ' is large enough to act as a short ckt for AC signals.
The node 'P' is almost at same potential as the +ve terminal, so that
 R_2 carries no current leading to high o/p impedance.

Differentiator & Integrator circuits:-

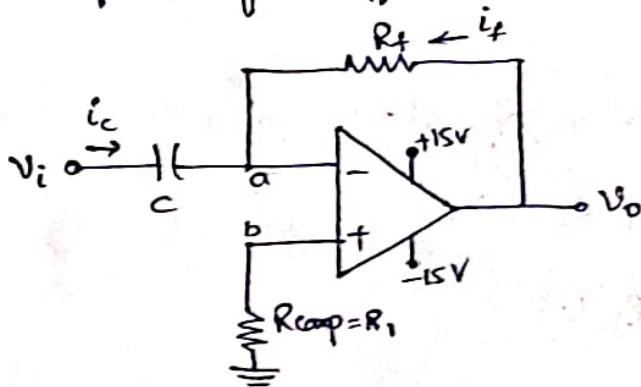
By introducing reactance into the feedback loops of an op-amp amplifier ckt's, we can cause the o/p to respond to the changes in the o/p voltage over time

Integrator produces o/p voltage proportional to the product of o/p voltage and the time

Differentiator produces a voltage proportional to the o/p voltage rate of change.

Differentiator:-

It performs the mathematical operation of differentiation
the o/p waveform of differentiator is a derivative of i/p waveform



The voltage at node 'a' i.e., V_a is zero (virtual ground).

$$\therefore V_a = 0$$

The current through capacitor is, $i_c = C \cdot \frac{d(V_i - V_a)}{dt}$

\Rightarrow

$$\Rightarrow i_c = C \cdot \frac{dV_i}{dt} \quad \text{--- (1)}$$

The current flowing through the feedback resistance

$$i_f = \frac{v_o}{R_f} \quad \text{--- (2)}$$

Apply KCL at node 'a' we get,

$$i_c + i_f = 0$$

$$\Rightarrow C \frac{dv_i}{dt} + \frac{v_o}{R_f} = 0$$

$$\Rightarrow C \frac{dv_i}{dt} = -\frac{v_o}{R_f}$$

$$\Rightarrow v_o = -R_f \cdot C \cdot \frac{dv_i}{dt}$$

$$\Rightarrow v_o \propto \frac{dv_i}{dt}$$

The op-amp voltage v_o is a constant ($-R_f \cdot C$) times of the derivative of the input voltage ' v_i '.

The -ve sign indicates the 180° phase shift of the op-amp v_o w.r.t. the input voltage ' v_i '.

The phasor representation of above eqn' is

$$V_o(s) = -R_f \cdot C \cdot s \cdot V_i(s)$$

$$\Rightarrow \frac{V_o(s)}{V_i(s)} = -R_f \cdot C \cdot s$$

$$\Rightarrow \text{gain}(A) = -R_f \cdot C \cdot s$$

In steady state, put $s=j\omega$, we get, $A = -R_f \cdot C \cdot j\omega$

the magnitude of gain is,

$$\Rightarrow |A| = \left| \frac{V_o}{V_i} \right| = |R_f \cdot C \cdot j\omega|$$

$$= \omega \cdot R_f \cdot C$$

$$= 2\pi f \cdot R_f \cdot C$$

$$\Rightarrow |A| = \frac{f}{\frac{1}{2\pi R_f C}}$$

$$\text{Let } f_a = \frac{1}{2\pi R_f C}$$

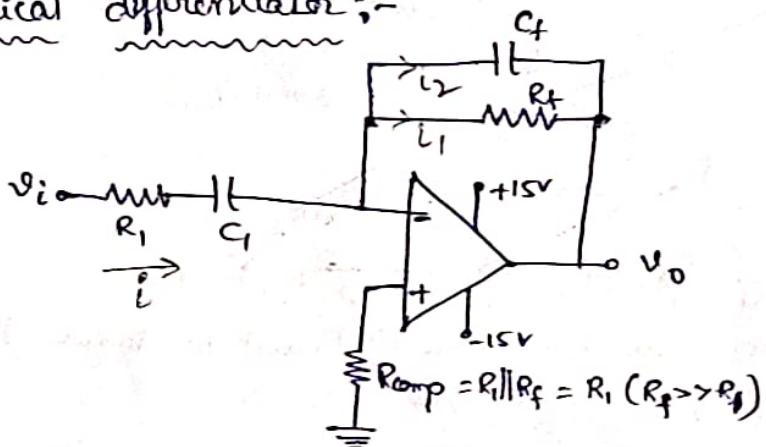
$$\Rightarrow |A| = \frac{f}{f_a}$$

$$\text{At } f=f_a, |A| = \frac{f}{f_a} = 1 \Rightarrow 0 \text{ dB.}$$

As the frequency increases, the gain increases at rate of ~~+20dB/decade~~
+20dB/decade. Thus at high frequency a differentiator becomes unstable. The i/p impedance decreases with increase in freq. so that the ckt becomes sensitive to high frequencies.

A practical differentiator will eliminate the instability and high freq. noise.

Practical differentiator :-



The transfer function of above ckt is,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_f}{Z_1}$$

$$= -\frac{s \cdot R_f \cdot C_1}{(1+s \cdot R_1 \cdot C_1) (1+s \cdot R_f \cdot C_f)}$$

$$\# R_f C_f = R_1 C_1$$

$$\Rightarrow \frac{V_o(s)}{V_i(s)} = -\frac{s \cdot R_f \cdot C_1}{(1+s \cdot R_1 \cdot C_1)^2}$$

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{1+sR_1C_1}{sC_1}$$

$$\therefore i = \frac{sC_1 V_i(s)}{(1+sR_1C_1)}$$

$$i_1 = \frac{V_a - V_o(s)}{R_f} = -\frac{V_o(s)}{R_f}$$

$$i_2 = -C_f \frac{dV_o}{dt} = -sC_f V_o(s)$$

$$i = i_1 + i_2$$

$$\frac{sC_1 V_i(s)}{1+sR_1C_1} = \frac{-V_o(s)}{R_f} - sC_f V_o(s)$$

$$\frac{sC_1 V_i(s)}{1+sR_1C_1} = -V_o(s) \left(\frac{1+sR_1C_1}{R_f} + sC_f \right)$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_f C_1}{(1+sR_1C_1)^2 + s^2 C_f^2}$$

$$f_f \leq j\omega$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-j\omega R_f C_1}{(1+j\omega R_f C_1)^2}$$

$$\omega = 2\pi f$$

$$\Rightarrow \frac{V_o(s)}{V_i(s)} = \frac{-j\omega R_f C_1}{(1+j2\pi f R_f C_1)^2}$$

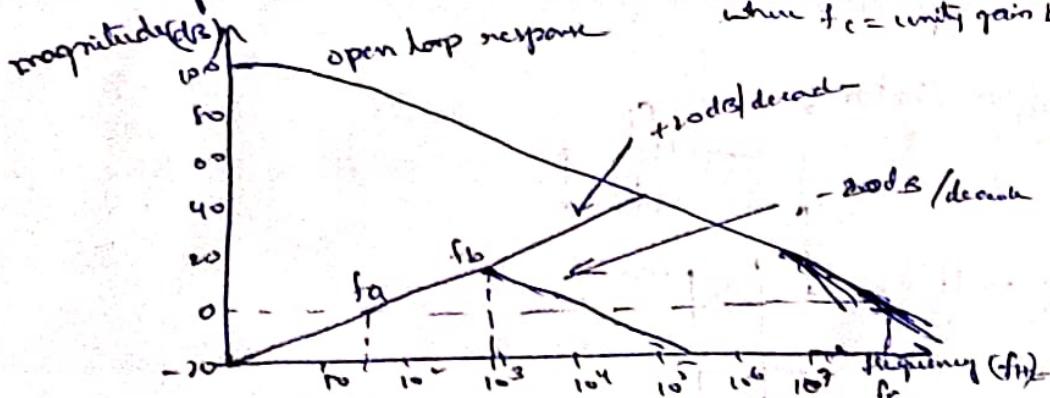
$$\Rightarrow \frac{V_o(s)}{V_i(s)} = \frac{-j(f/f_a)}{[1+j(f/f_b)]^2} ; f_a = \frac{1}{2\pi R_f C_1} \text{ where; } f_b = \frac{1}{2\pi R_f C_1}$$

From the above equation,

→ If $f < f_b \rightarrow$ gain increases at $+20 \text{ dB/decade}$ freq.

→ If $f > f_b \rightarrow$ gain decreases at -20 dB/decade

→ The value of f_b should be selected such that $f_a < f_b < f_c$.
where $f_c = \text{unity gain bandwidth}$.



For a good differentiation, the time period 'T' must be larger than or equal to $R_f C_1$. $T \geq R_f C_1$.

→ In order to design a good differentiator circuit, the following step followed.

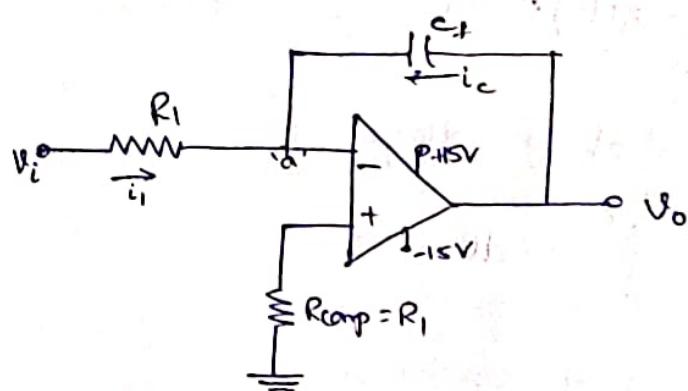
- * Choose choose 'f_a' equal to the highest freq. of the i/p signal.
- * Assume a practical value of C_1 ($< 1 \mu F$) and then calculate R_f .
- * Choose $f_b = 10 \cdot f_a$, Now calculate the value of R_f & C_f . So that, $R_f C_1 = R_f C_f$.

Integrator:-

It performs the mathematical operation of integration.

The op-amp waveform of integrator is a integration of i/p waveform.

An integrator can be designed by interchanging capacitor and resistor in a differentiator.



Current through the resistor 'R₁' is,

$$i_1 = \frac{V_i}{R_1} \quad \text{--- (1)}$$

Current through the capacitor 'C_f' is

$$i_c = C_f \cdot \frac{dV_o}{dt} \quad \text{--- (2)}$$

Apply KCL at node 'a' we get,

$$i_1 + i_c = 0$$

$$\Rightarrow \frac{V_i}{R_1} + C_f \cdot \frac{dV_o}{dt} = 0$$

$$\Rightarrow C_f \cdot \frac{dV_o}{dt} = -\frac{V_i}{R_1}$$

$$\Rightarrow \frac{dV_o}{dt} = -\frac{1}{R_1 C_f} V_i$$

$$\Rightarrow dV_o = -\frac{1}{R_1 C_f} V_i dt$$

Integrating on both sides, we get,

$$\int_0^t dv_o = \int_0^t -\frac{1}{R_1 C_f} \cdot v_o dt$$

$$\Rightarrow V_o(t) - V_o(0) = -\frac{1}{R_1 C_f} \int_0^t v_i dt$$

$$\Rightarrow V_o(t) = -\frac{1}{R_1 C_f} \int_0^t v_i(t) dt + V_o(0) \quad \text{--- (1)}$$

where $V_o(0)$ = initial op voltage.

$$\therefore V_o(t) \propto \int_0^t v_i(t) dt$$

The phasor equivalent of eqn (1) is,

$$V_o(s) = -\frac{1}{R_1 C_f} \cdot \frac{1}{s} \cdot V_i(s)$$

$$\Rightarrow \frac{V_o(s)}{V_i(s)} = \frac{-1}{s R_1 C_f}$$

In steady state, $s=j\omega$ we get,

$$A = \frac{-1}{j\omega R_1 C_f}$$

$$\Rightarrow A = \frac{-1}{j 2\pi f R_1 C_f}$$

$$\Rightarrow |A| = \frac{1}{(f/f_b)} \quad \left(\because f_b = \frac{1}{2\pi R_1 C_f} \right)$$

$$\Rightarrow |A| = \frac{f_b}{f}$$

If $f = f_b$, then $|A| = 1$ = 0dB.

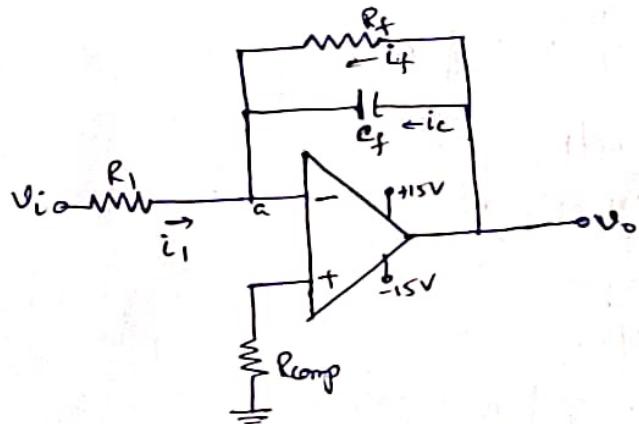
If $\omega = 0 \Rightarrow$ gain becomes infinite, capacitor acts as an open ckt.

In practical, the gain cannot be infinite. i.e., the op-amp saturates at the voltage close to positive (+) negative power supply depending on the polarity of the op-amp signal.

- Gain of the integrator decreases with increase in frequency
- Integrator doesn't have freq. problem like in a differentiator.

Practical Integrator: (Lossy Integrator) :-

The gain of an integrator at low frequency can be limited to avoid saturation problem. This can be done by placing a resistor in parallel to the capacitor as shown below.



The parallel combination of a capacitor and the resistance will behave like a practical capacitor which dissipates power. Thus it is called as lossy Integrator.

The resistance 'Rf' limits the low freq. gain to $-R_f/R_1$. Generally 'Rf' should be 10 times ~~of~~ than R_1 . Due to this resistor, the integrator ckt is stabilized at low frequencies.

Analysis:-

$$\text{From the fig; } i_1 = \frac{v_i}{R_1}, \quad i_f = \frac{v_o}{R_f}, \quad i_c = C_f \frac{dv_o}{dt}$$

Apply KCL at node 'a' we get,

$$i_1 + i_f + i_c = 0.$$

$$\frac{\partial \psi}{\partial r} + \frac{\partial \psi}{\partial \theta} + C_0 \frac{\partial^2 \psi}{\partial \theta^2} = 0$$

$$\frac{\partial \psi}{\partial r} = - \left[C_0 \frac{\partial^2 \psi}{\partial \theta^2} + \frac{\partial \psi}{\partial \theta} \right]$$

$$\Rightarrow \psi = - \frac{C_0}{R_0} \left[C_0 \frac{\partial \psi}{\partial \theta} + \frac{\psi}{R_0} \right]$$

The phase gradient of ψ is

$$\Rightarrow \psi(r) = - \frac{C_0}{R_0} \left[C_0 \cdot \sin \psi(r) + \frac{\psi(r)}{R_0} \right]$$

$$\Rightarrow \psi(r) \left[1 + \frac{C_0 C_0}{R_0^2} \right] = - \frac{C_0}{R_0} \psi(r)$$

$$\Rightarrow \frac{\psi(r)}{\psi(r)} = \frac{-C_0 R_0}{(1 + \frac{C_0 C_0}{R_0^2})}$$

In steady state, $\frac{d\psi}{dr} = 0$

$$\Rightarrow A = \frac{-C_0 R_0}{(1 + \frac{C_0 C_0}{R_0^2})}$$

Magnitude of gain =

$$|A| = \frac{R_0 |R_0|}{\sqrt{1 + \frac{C_0 C_0}{R_0^2}}}$$

At low freq i.e. $\omega = 0$, the gain becomes constant, i.e., $R_0 |R_0|$,

$$|A| = \frac{R_0 |R_0|}{\sqrt{1 + \frac{C_0 C_0}{R_0^2}}}$$

$$= |A| = \frac{R_0 |R_0|}{\sqrt{1 + (\frac{f}{f_0})^2}} \quad \text{where } f_0 = \frac{1}{2\pi R_0 C_0}$$

If $t = t_0$, then $\sqrt{1 + \left(\frac{t}{t_0}\right)^2} = \sqrt{1 + 1^2} = \sqrt{2}$.

$$\therefore A_v = \frac{1}{\sqrt{2}} \left(\frac{R_f}{R_i} \right) \quad //$$

[Ends below R_i , at $t = t_0$].

Comparator :-

A comparator is a circuit which compares a signal voltage applied at one ip of an op-amp with the reference voltage at the other input.

In a comparator circuit the op-amp is used in open loop mode, with $df = v_{sat} (= V_C)$.

There are two types of comparators. They are:-

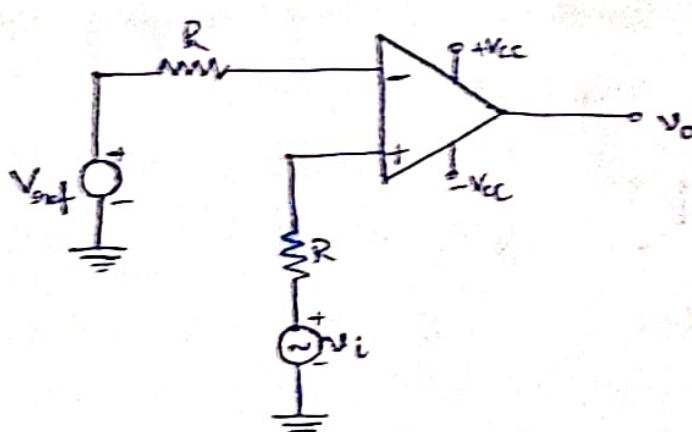
(i) Non-inverting comparator

(ii) Inverting comparator.

(i) Non-inverting comparator :-

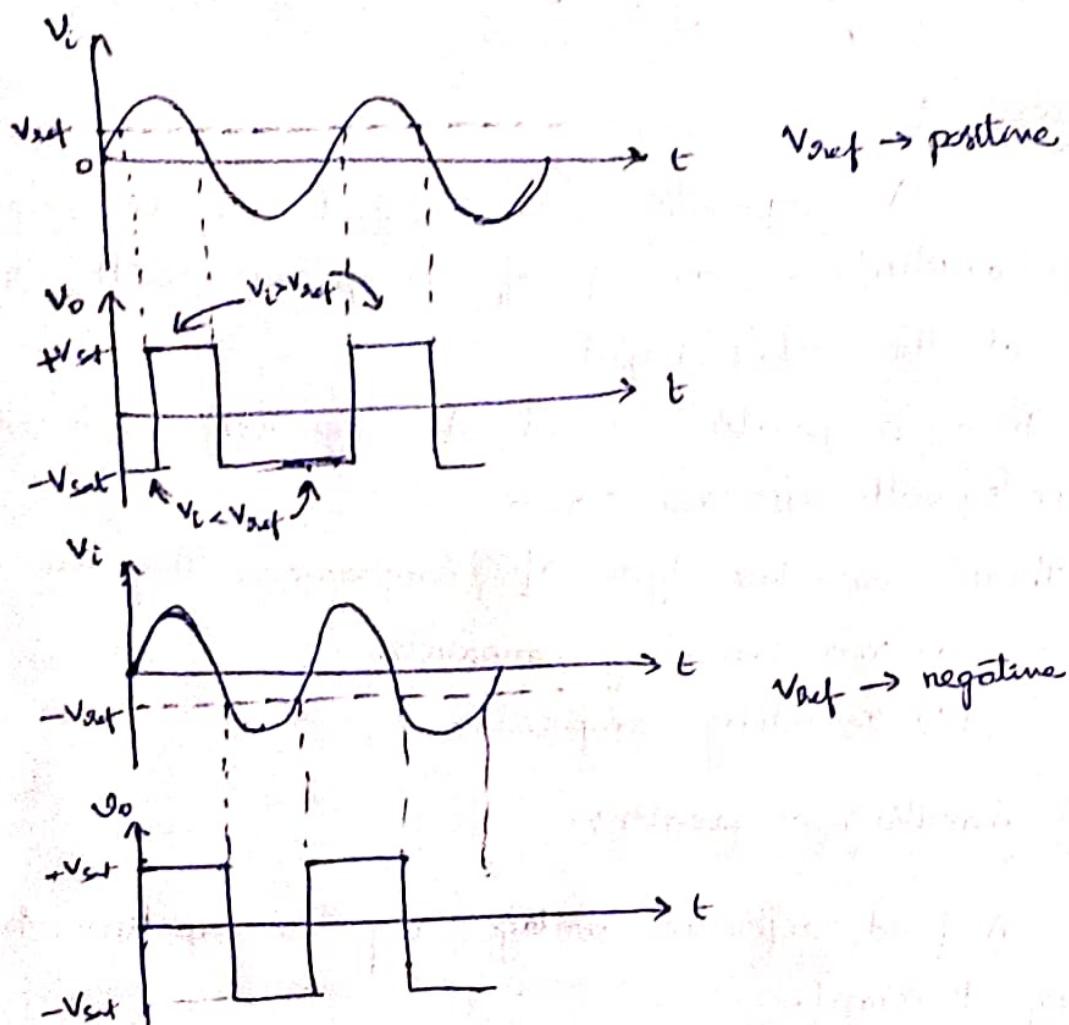
A fixed reference voltage V_{ref} is applied to the inverting terminal.

A time varying sig 'Vi' is applied to non-inverting terminal.



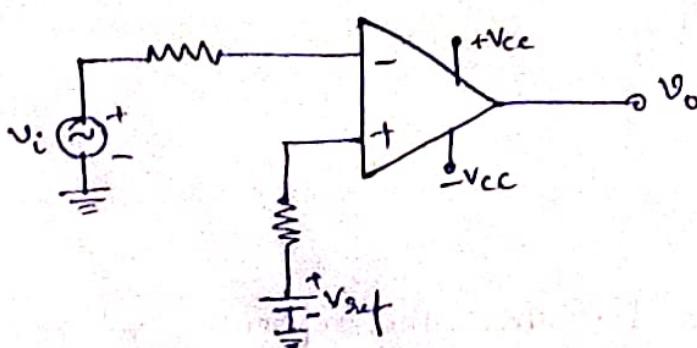
If the ip voltage 'Vi' is less than the reference voltage, then the op voltage is $-V_{sat}$. i.e., $Vi < V_{ref} \Rightarrow V_o = -V_{sat}$

If the i/p voltage is more than the reference voltage, then the o/p voltage is " $+V_{sat}$ ". i.e., $V_i > V_{ref} \Rightarrow V_o = +V_{sat}$ "



Inverting Comparator :-

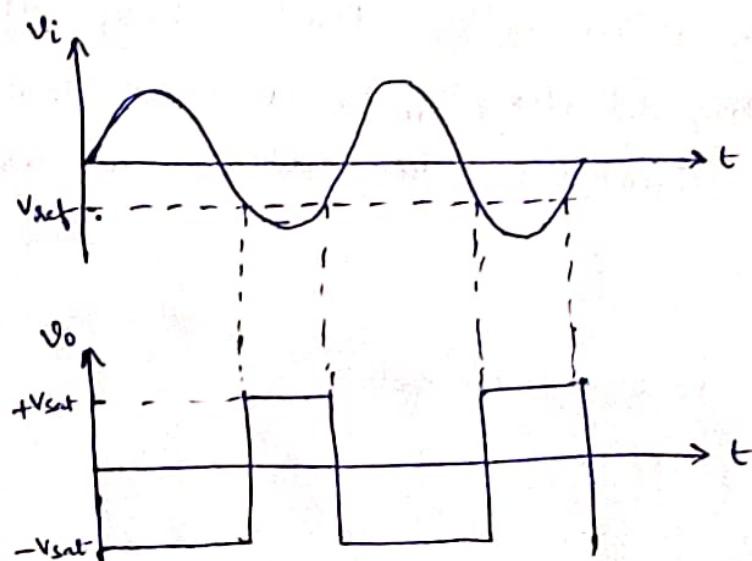
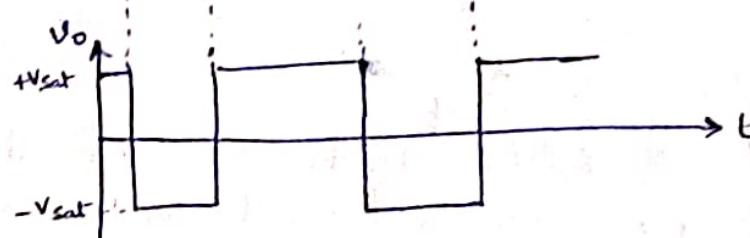
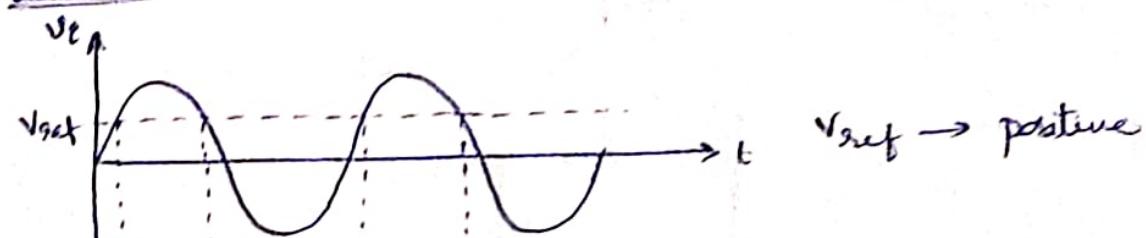
In inverting comparator, a fixed reference voltage is applied at the non-inverting terminal. A time varying i/p signal v_i is applied at the inverting terminal.



→ If the i/p voltage ' v_i ' is less than reference voltage ' v_{ref} ', then the o/p voltage ' v_o ' is " $+v_{sat}$ ". i.e., $v_i < v_{ref} \Rightarrow v_o = +v_{sat}$.

→ If the i/p voltage ' v_i ' is greater than reference voltage ' v_{ref} ', then the o/p voltage ' v_o ' is " $-v_{sat}$ ". i.e., $v_i > v_{ref} \Rightarrow v_o = -v_{sat}$.

i/p & o/p waveforms :-



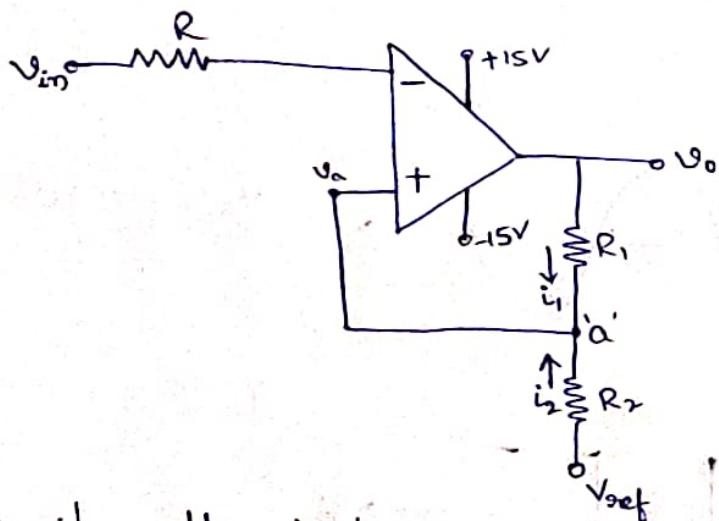
Applications of comparator :-

Some important applications of comparator are:-

- (i) Zero crossing detector (v) Level detector
- (ii) Window detector (vi) Duty cycle controller
- (iii) Time marker generator (vii) Pulse generator.
- (iv) Phase meter.

Schmitt Trigger (Regenerative Comparator) :-

Schmitt trigger is an electronic circuit which converts any continuous signal into a square (or) pulse wave. It is also called as regenerative comparator.



The input voltage v_i is applied to the -ve terminal and feedback voltage is applied at the terminal. The input voltage triggers the op-amp every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}). The difference b/w these two voltages is called hysteresis ($V_{UT} - V_{LT}$).

Apply KCL at node 'a', we get

$$i_1 + i_2 = 0$$

$$\Rightarrow \frac{V_{ref} - v_a}{R_2} + \frac{V_o - v_a}{R_1} = 0$$

$$\Rightarrow v_a \left[\frac{1}{R_1} + \frac{1}{R_2} \right] = \frac{V_o}{R_1} + \frac{V_{ref}}{R_2}$$

$$\Rightarrow v_a \left[\frac{R_1 + R_2}{R_1 R_2} \right] = \frac{R_2 V_o + R_1 V_{ref}}{R_1 R_2}$$

$$\Rightarrow V_a = \frac{R_2}{R_1+R_2} V_o + \frac{R_1}{R_1+R_2} V_{ref}$$

' V_a ' is the voltage of the positive terminal of op-amp.
As the op-amp is used in open-loop mode its o/p is either $+V_{sat}$ or $-V_{sat}$.

(8) $-V_{sat}$:

If $V_{in} > V_a$, then $V_o = -V_{sat}$

$V_{in} < V_a$ then $V_o = +V_{sat}$

$$\therefore V_a = V_{ref} \left[\frac{R_1}{R_1+R_2} \right] \pm V_{sat} \left[\frac{R_2}{R_1+R_2} \right]$$

If $V_o = +V_{sat}$, then $V_a = V_{UT}$.

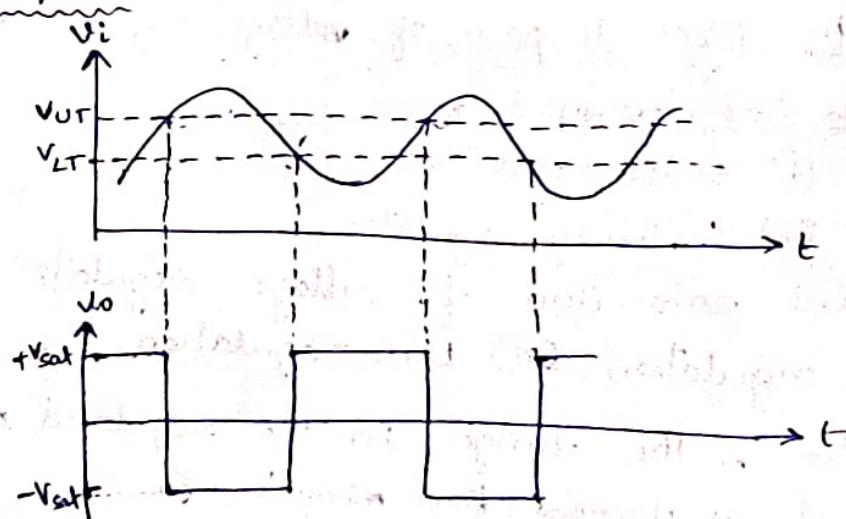
$$\therefore V_{UT} = V_{ref} \left[\frac{R_1}{R_1+R_2} \right] + V_{sat} \left[\frac{R_2}{R_1+R_2} \right]$$

If $V_o = -V_{sat}$, then $V_a = V_{LT}$.

$$\therefore V_{LT} = V_{ref} \left[\frac{R_1}{R_1+R_2} \right] - V_{sat} \left[\frac{R_2}{R_1+R_2} \right]$$

The i/p voltage ' v_i ' must become lesser than V_{LT} in order to cause V_o to switch from $-V_{sat}$ to $+V_{sat}$.

i/p & o/p waveforms:-



$$V_{DT} = V_{DT} - V_{LT}$$

$$\Rightarrow H = \frac{S R_2 V_{sat}}{R_1 + R_2}$$

Introduction to voltage Regulators :-

The function of voltage regulator is to provide a stable DC voltage for powering other electronic circuits.

If the input is AC, then it has to be rectified, filtered and then applied to the regulator circuit.

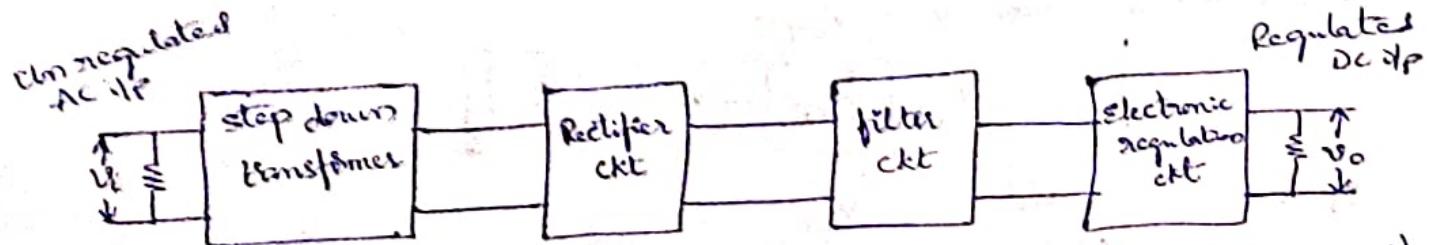


fig:- Block diagram of voltage regulator (AC input).

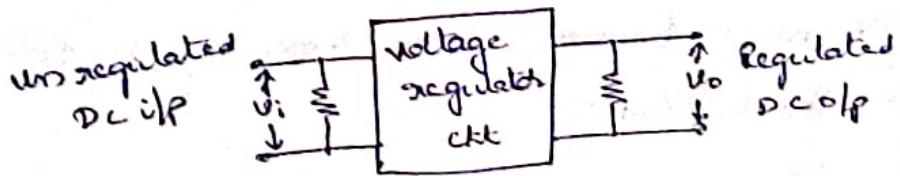


fig:- Block diagram of voltage regulator (DC input)

Voltage regulators are classified as,

(i) Series regulator

(ii) Switching regulator.

The two important parameters of voltage regulators are:-

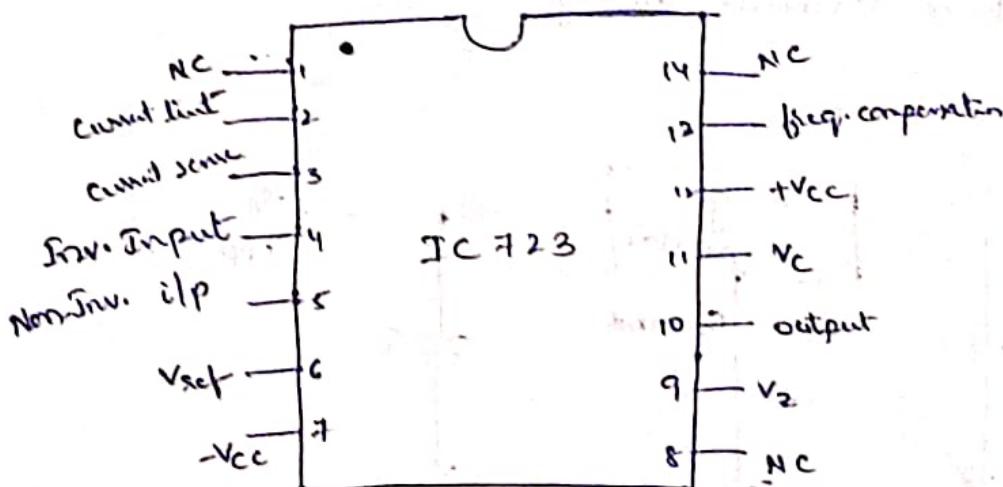
(i) Load regulation (ii) Line regulation.

- Load regulation is the change in the regulated o/p voltage when the load current is changed from min. to max.
- Line regulation indicates the effect of change in the i/p line voltage on the o/p voltage of the regulator.

General purpose Linear IC 723 Regulator :-

The popular general purpose precision regulator is IC 723. It is a monolithic linear I.C. in different physical packages.

The pin diagram of IC 723 is shown below.



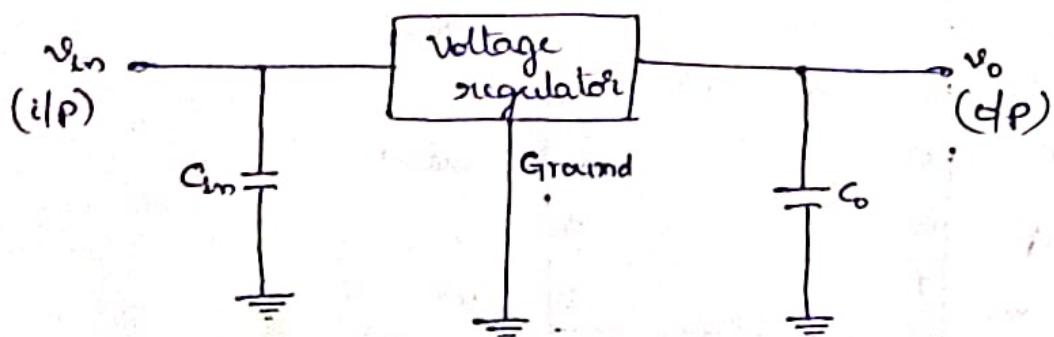
Important features of IC 723 :-

- It works as voltage regulator at output voltage ranging from 2 to 37 volts at current upto 150 mA.
- It can be used at load currents greater than 150mA with use of suitable NPN or PNP external pass transistors.
- Input & o/p short circuit protection is provided.
- It has good line and load regulation (0.03%).
- Wide variety of applications of series, shunt, switching and flat regulator.
- Low temp. drift and high ripple rejection.
- low standby current drain.
- small size, lower cost.
- Relative ease with which power supply can be designed.
- It provides a choice of supply voltage.

three terminal IC voltage regulators :-

As the name suggests, three terminal voltage regulators have three terminals namely ip which is unregulated (v_{in}), regulated op(v_o), and common (as) a ground terminal.

The basic three terminal voltage regulator is as shown in below figure.

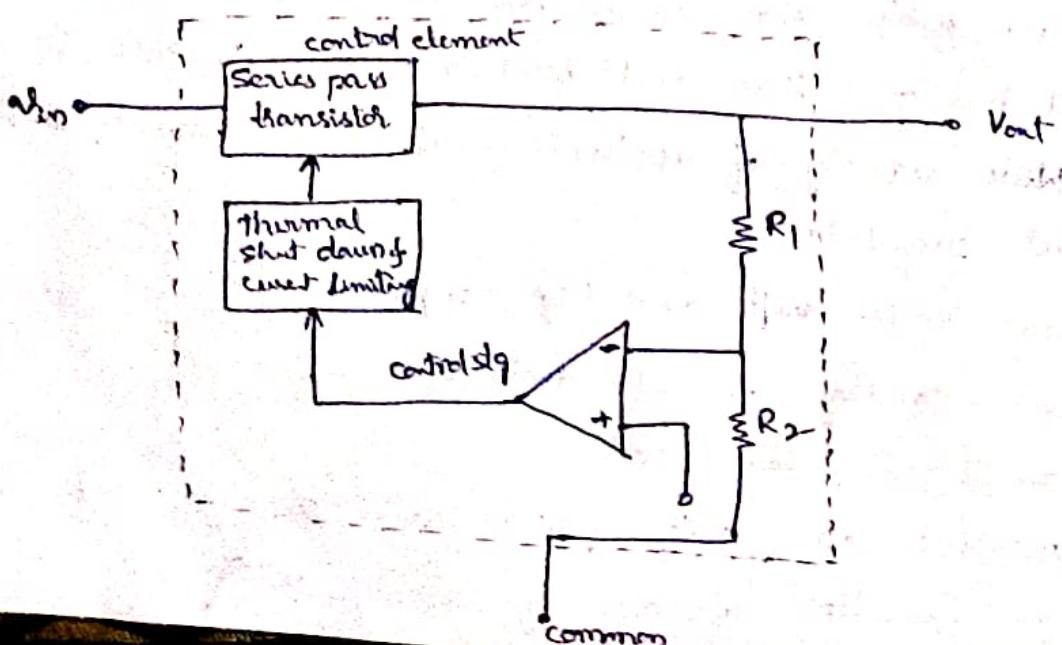


These regulators don't require any feedback connections.

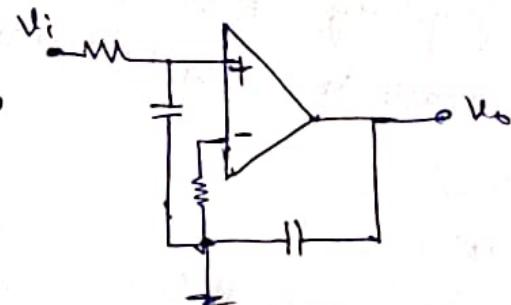
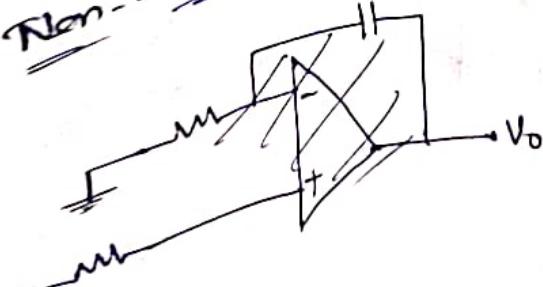
The capacitor 'C_{in}' is required if regulator is located at appreciable distance more than 5cm from a power supply filter.

The op capacitor 'C_o' may not be needed but if used it improves the transient response of the regulator.

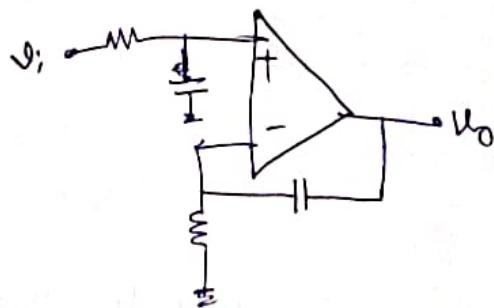
Block diagram of basic three terminal IC regulator :-



Non-inverting integrator



Non-inverting differentiator



- Q) Design a practical integrator with the following specifications.
- To integrate signals down to 200 Hz, and to produce peak voltage of 0.1V.
 - b) when the i/p $V_i = 10 \text{ mV} (2\pi \times 10^4 t) \text{ mV}$

Find the d.c. component at the o/p when the i/p is 10mV d.c.

Hint:-

$$f_{c1} = 200 \text{ Hz}$$

$$V_o(\text{peak}) = 0.1 \text{ V} \quad \text{when } V_i(\text{peak}) = 10 \text{ mV}$$

$$\text{gain} = 10$$

$$\rightarrow V_o(t) = -\frac{1}{R_1 C_f} \int v_i(t) dt$$

$$\rightarrow \text{D.C. component in o/p} = \text{D.C. gain} \times \text{D.C.i/p}$$

UNIT-II

Op-amp, IC-555 & IC 565 Applications

Active filters:-

A filter is a circuit that is designed to pass a specified band of frequencies while attenuating all the signals outside that band. It is a frequency selective circuit. Filters are used in circuits, which require the separation of signals according to their frequencies.

The filters are basically classified as: active filters and passive filters.

The passive filter networks use only passive components like resistor, inductor & capacitors.

The active filter uses active elements such as op-amps, transistors along with R, L & C.

Modern active filters don't use inductors as the inductors are bulky, heavy & non-linear. And also power dissipation is more.

The active filters uses capacitive feedback to avoid using of inductors.

The most commonly used filters are:-

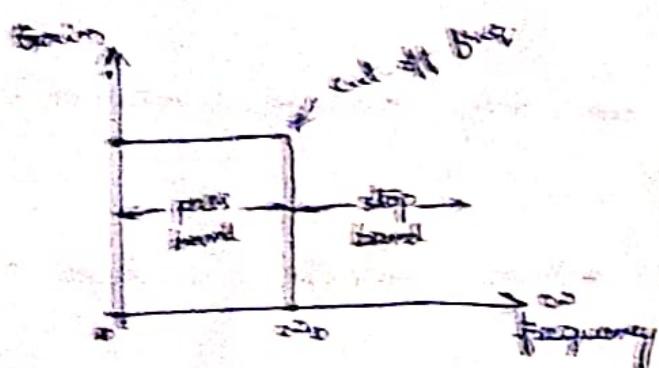
- (i) Low Pass filter
- (ii) High pass filter
- (iii) Band pass filter
- (iv) Band Reject filter
- (v) All pass filter.

(i) Low pass filter:-

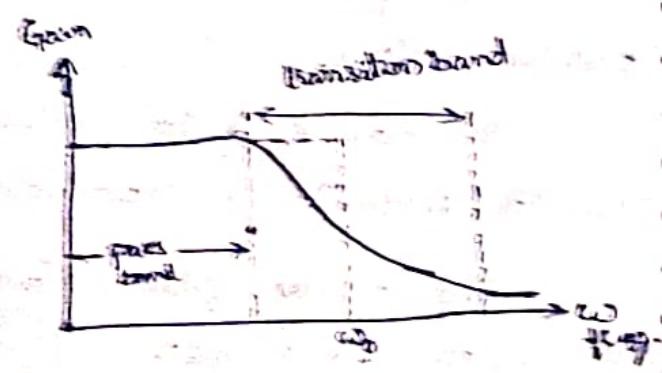
In low pass filter, the filter allows all the frequencies which are less than the cut-off frequency and reject remaining frequencies.

If ω_c is the cut-off frequency, $\omega < \omega_c$ is pass band & $\omega > \omega_c$ is stop band.

The ideal and practical frequency response for low pass filter is shown below.



Ideal freq response of LPF

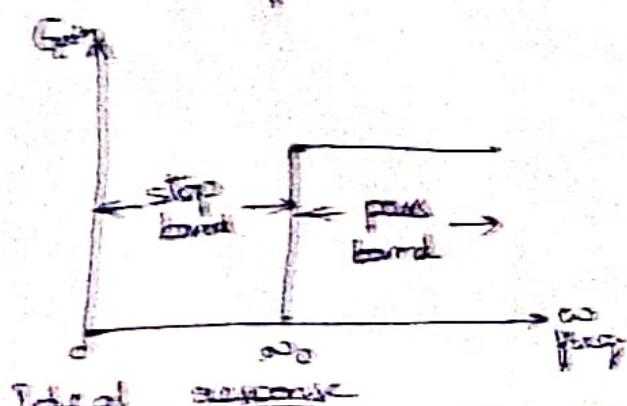


Practical freq response of LPF

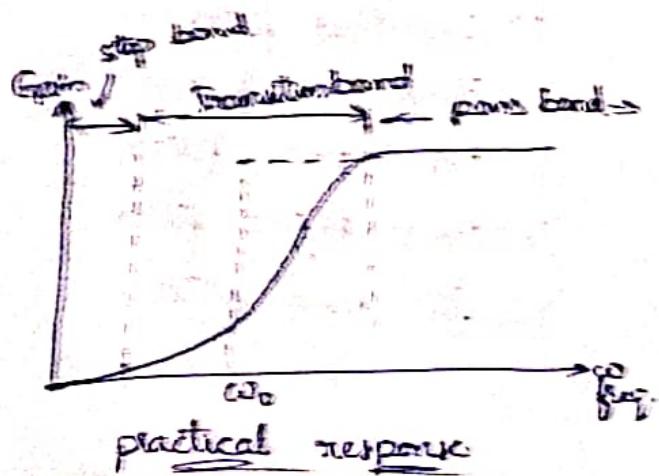
(ii) High pass filter:-

In high pass filter, the filter allows all the frequencies which are higher than cut-off frequency and reject remaining frequencies.

If ω_c is cut-off frequency, $\omega < \omega_c$ is pass band and $\omega > \omega_c$ is stop band.



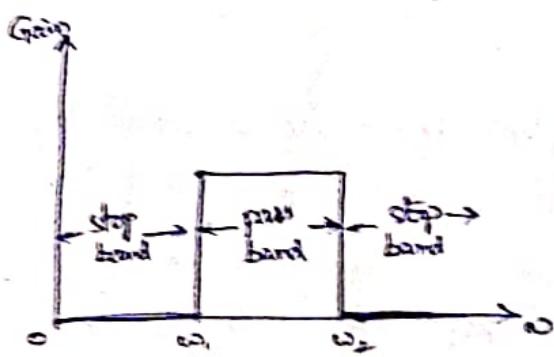
Ideal response



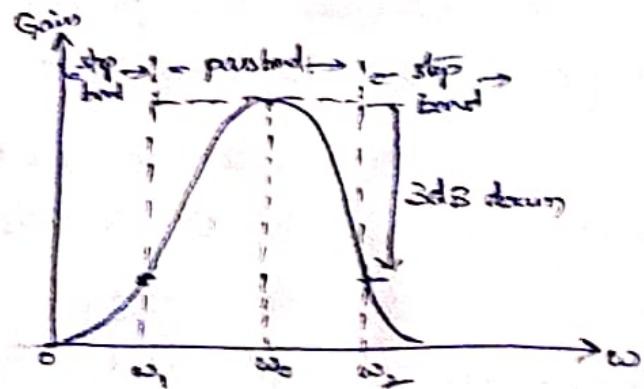
practical response

Band pass filter:-

- Band pass filter allows only particular band of frequencies to pass and reject remaining all frequencies.
- It has two cut-off frequencies and two stop bands & one pass band.
 - If ω_1, ω_2 are two cutoff frequencies, the pass band is $\omega_1 < \omega < \omega_2$, and stop bands are $0 < \omega < \omega_1$ & $\omega > \omega_2$.
 - The difference b/w ω_1 & ω_2 is called bandwidth = $\omega_2 - \omega_1$.
 - The freq. b/w ω_1 & ω_2 where gain attains max. value is called centre centre frequency, denoted as ω_c .



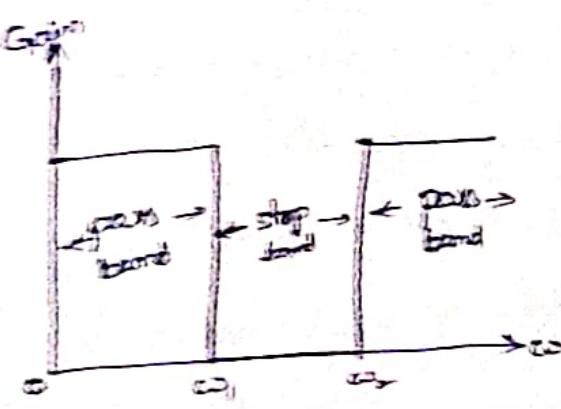
Ideal response



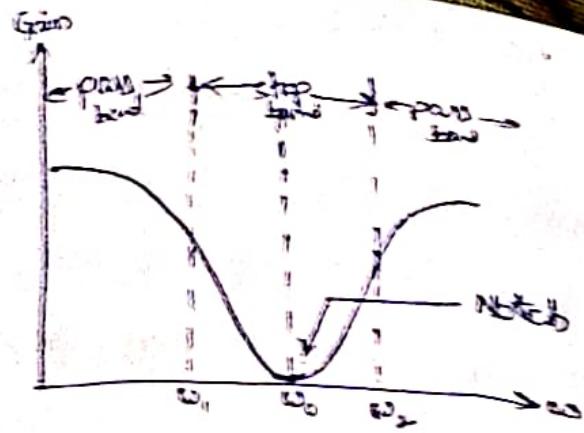
practical response

Band Reject filter (a) Band stop filter:-

- Band ^{stop} filter rejects only particular band of frequencies and allows remaining all frequencies to pass.
- Its characteristics are exactly opposite to band pass filter.
 - It has two cut off frequencies, one stop band & two pass bands.
 - If ω_1, ω_2 are the two cut-off frequencies, the stop band is $\omega_1 < \omega < \omega_2$ and pass bands are $0 < \omega < \omega_1$ & $\omega > \omega_2$.
 - The freq. at which the gain is minimum is called centre frequency, denoted as ω_c . The practical response shows a notch. Hence, this is also called a "notch filter".



Ideal response



Practical response

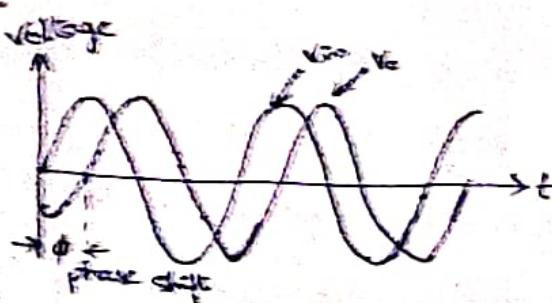
All pass filter :-

The all pass filter passes all the frequencies but it produces the phase shift between ip & op.

The filter which is used to control the phase response by adding a phase shift like ip & op signals is called all pass filter.

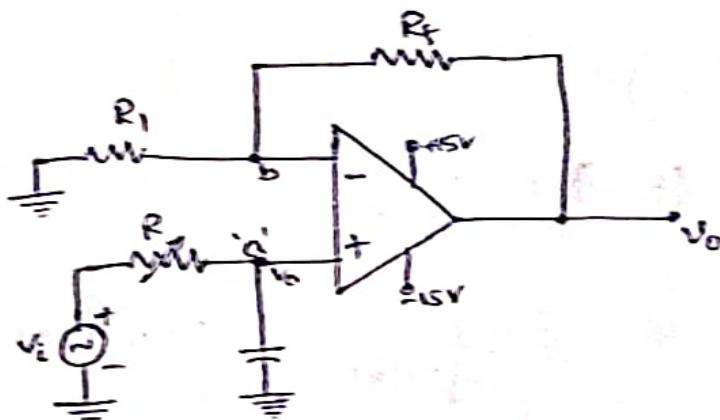
The ip & op voltage are equal in magnitudes for all the frequencies but with the phase shift b/w the two.

The frequency upto which the ip - op amplitudes remains same is decided by the Unity Gain Bandwidth (UGB) of the op-amp used.



First order low pass Butterworth filter :-

The first order low pass butterworth filter is realised by R-C circuit used along with an op-amp in non-inverting configuration. The circuit diagram is shown in below figure



This is also called one pole low pass butterworth filter.

The resistors R_f & R , decide the gain of the filter in the pass band.

Analysis:-

The voltage across the capacitor (v_a) voltage at node 'a' is, in s-domain, is

$$v_a \quad V_a(s) = \frac{V_{sc}}{R + V_{sc}} \cdot V_i(s)$$

$$\Rightarrow \frac{V_a(s)}{V_i(s)} = \frac{V_{sc}}{\frac{1+Rsc}{sc}}$$

$$\Rightarrow \frac{V_a(s)}{V_i(s)} = \frac{1}{1+Rcs} \quad -\textcircled{1}$$

where $V(s)$ is Laplace transform of 'v' in time domain.

Since, the op-amp is used in non-inverting configuration,

Its gain is, $A_B = \frac{V_o(s)}{V_a(s)} = 1 + \frac{R_f}{R_1} = \infty \quad -\textcircled{2}$

∴ Δ

So, the overall transfer function from eqn's ① & ② is

$$\frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_d(s)} \times \frac{V_d(s)}{V_i(s)}$$

$$\Rightarrow H(s) = A_0 \cdot \frac{1}{1+RCS}$$

At steady state, $s = j\omega$.

$$\therefore \text{Overall gain } A, (H(j\omega)) = \frac{A_0}{1+j\omega RC}$$

$$= \frac{A_0}{1+j2\pi f RC} \quad [\because \omega = 2\pi f]$$

$$A = \frac{A_0}{1+j(f/f_a)} \quad [\text{Let } f_a = \frac{1}{2\pi RC}]$$

Magnitude of gain,

$$|A| = \frac{A_0}{\sqrt{1+(f/f_a)^2}}$$

Case(i):- For frequencies below cut-off frequency.

$$f \ll f_a$$

$$|A| \approx A_0$$

Case(ii):- At $f = f_a$

$$|A| = \frac{A_0}{\sqrt{1+1}} = \frac{A_0}{\sqrt{2}}$$

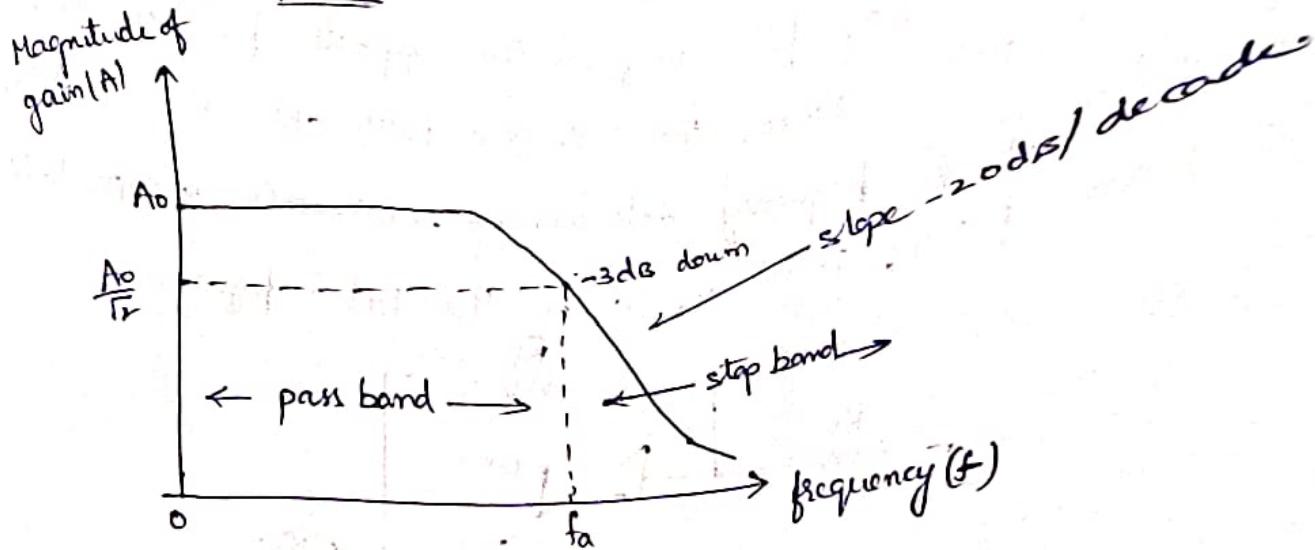
$$\Rightarrow |A| = 0.707 A_0 \quad [\text{at } f_a]$$

Case(iii):- At $f > f_a$

$$|A| = \frac{A_0}{\sqrt{1+(f/f_a)^2}}$$

$$|A| \approx 0$$

Frequency response of L.P.F. :-



First order high pass Butterworth filter :-

Design steps for low pass Butterworth filter :-

- i) Choose the cut-off frequency "f_a".
- ii) Choose capacitance 'c', usually b/w 0.001 & 1 μF. Generally, it is selected as 1 μF or less than that.
- iii) Now for the RC circuit,

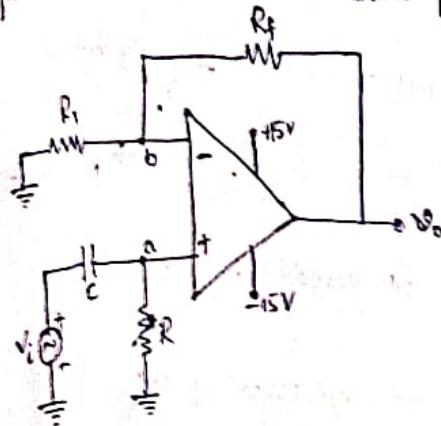
$$f_a = \frac{1}{2\pi RC}$$

- iv) Hence, f_a & c are known, calculate value of 'R'.
- v) The resistance R_f & R₁ can be selected depending on the required gain in the pass band.

$$A_o = 1 + \frac{R_f}{R_1}$$

first order high pass butterworth filter:-

A high pass filter performs the opposite function to that of low pass filter. Hence, the high pass filter ckt can be obtained by interchanging frequency determining resistance (R) & capacitor (C) in low pass filter, it is shown in the below figure.



Analysis:-

The voltage at node 'a' is in s-domain is,

$$V_a(s) = \frac{R}{R + \frac{1}{sC}} \cdot V_i(s)$$

$$V_a(s) = \frac{RSC}{RSC + 1} V_i(s)$$

$$\Rightarrow \frac{V_a(s)}{V_i(s)} = \frac{RSC}{RSC + 1} \quad \text{--- (1)}$$

Since, the op-amp is used in non-inverting configuration, transfer of op-amp is,

$$A_f = \frac{V_o(s)}{V_i(s)} = 1 + \frac{R_f}{R_1} \quad \text{--- (2)}$$

From eqn (2), the overall transfer function is,

$$\frac{V_o(s)}{V_i(s)} = \frac{V_a(s)}{V_i(s)} \cdot \frac{V_o(s)}{V_a(s)}$$

$$\begin{aligned} &\Rightarrow \text{gain} \\ &\Rightarrow A = \frac{A_0}{1 + j\omega RC} \\ &\Rightarrow A = \frac{A_0}{1 + j2\pi f RC} \\ &\Rightarrow A = \frac{A_0}{1 + j(\frac{f}{f_a})} \end{aligned}$$

the magnitude of

$$|A| = \frac{A_0}{\sqrt{1 + (\frac{f}{f_a})^2}}$$

case(i): for frequencies

$$|A| = \frac{A_0}{\sqrt{1 + (\frac{f}{f_a})^2}}$$

$$\text{case(ii): } f_a \ll f = f_a$$

$$|A| =$$

$$\text{case(iii): } f_a \ll f > \gg f_a$$

$$|A| =$$

$$\frac{sc}{sc+1} = A_0 \left[\frac{1}{\frac{RSC}{RSC+1} + \frac{1}{RSC}} \right]$$

$$[\text{Let } f_a = \frac{1}{2\pi RC}]$$

$$\left[s - \frac{1}{f_a} = -j \right]$$

gains,

$$\left[\frac{A_0}{\left(\frac{s}{f_a} \right)^2} \right]$$

where $f_a = \text{cut-off freq}$

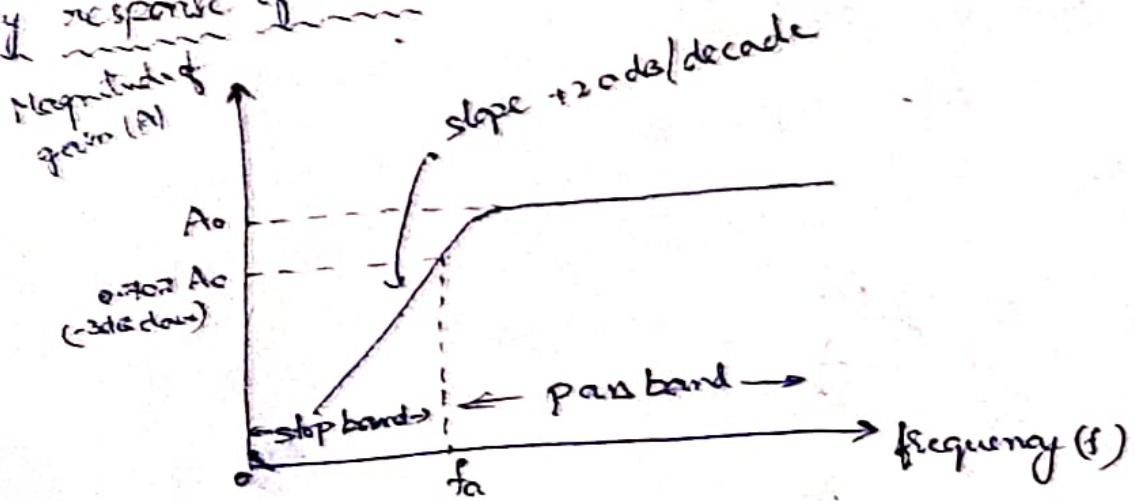
below cut-off frequency - $s < < f_a$

$$\frac{A_0}{\left(\frac{s}{f_a} \right)^2} \Rightarrow |A| \approx 0$$

$$\frac{A_0}{f_{crossover}} = \frac{A_0}{f_a} = 0.707 A_0 \quad (\pi - 3 \text{dB down})$$

$$\frac{\frac{A_0}{f_{crossover}}}{A_0} = \frac{1}{\sqrt{2}}$$

Frequency response of HIF :-

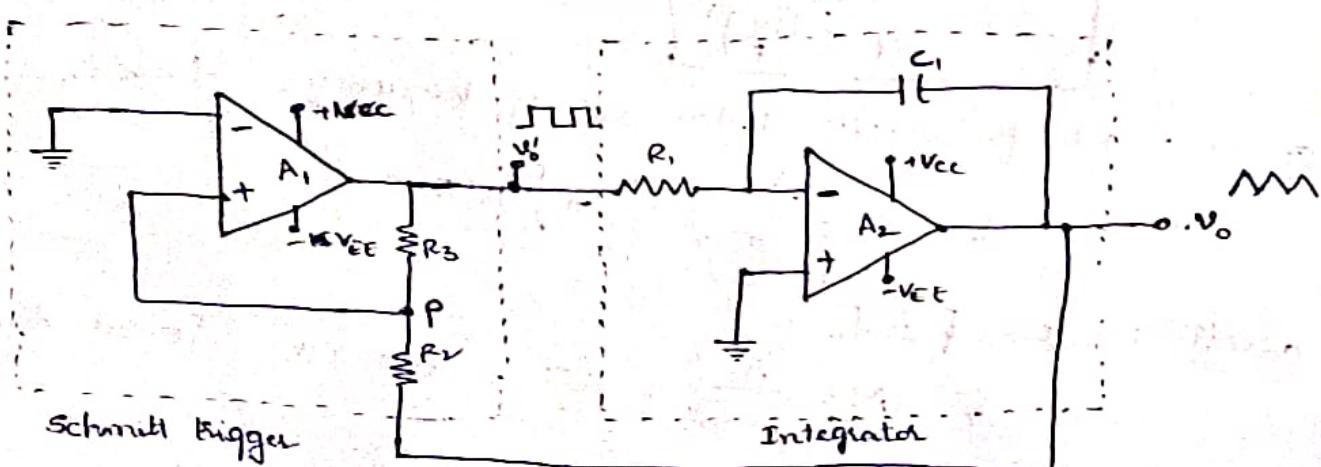


Waveform generators:- Triangular wave Generator :-

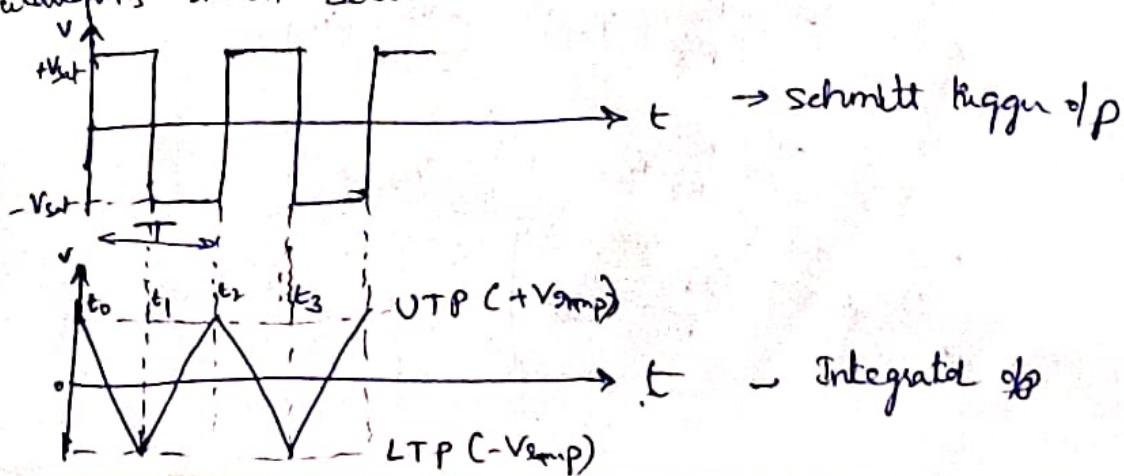
A triangular wave can be simply obtained by integrating a square wave. We know that; the o/p of a schmitt trigger is square wave for any input.

thus, if the o/p of schmitt trigger is applied to input of integrator and o/p of integrator is i/p to schmitt trigger, then the circuit works as a triangular/rectangular wave generator.

The below figure shows the ckt diagram of triangular wave generator.



- The op-amp A_1 in the ckt is schmitt trigger (a) comparator
op-amp A_2 is integrator.
 - The o/p of the schmitt trigger is rectangular wave of amplitude $\pm V_{sat}$ and is applied to inverting integrator.
 - Operation :-
 - Let the o/p of the schmitt trigger is $\pm V_{sat}$
 - This faces the current $\pm V_{sat}/R_i$ through C_1 , C_1 is charging with a positive polarity to left & negative to right.
 - This produces a negative going ramp at its o/p, for the time interval t_0 to t_1 .
 - At time ' t_1 ' when ramp voltage attains a value equal to $LTP \frac{Gv_{ramp}}{C_1}$ of schmitt trigger, the o/p voltage of schmitt trigger changes from $\pm V_{sat}$ to $-V_{sat}$.
 - Now direction of current through ' C_1 ' reversed. It discharges and reaches in opposite direction.
 - This produces positive going ramp at its o/p, for the time t_1 to t_2 .
 - At ' t_2 ', when ramp voltage attains a value equal to $UTP \frac{Gv_{ramp}}{C_1}$, the o/p of schmitt trigger changes from $-V_{sat}$ to $\pm V_{sat}$ and cycle continues.
- The waveforms shown below.



When schmitt trigger opamp is at $+V_{sat}$, the effective voltage at point 'P' is given by,

$$-V_{ramp} + \frac{R_2}{R_2+R_3} \left[+V_{sat} - (-V_{ramp}) \right] \quad \text{--- (1)}$$

When effective voltage at 'P' becomes zero, then above eqn can be written as

$$\begin{aligned} \frac{V_P - (V_{sat})}{R_3} + \frac{V_P - (-V_{ramp})}{R_2} &= 0 \\ V_P \left(\frac{1}{R_2} + \frac{1}{R_3} \right) &= \frac{-V_{sat}}{R_3} + \frac{-V_{ramp}}{R_2} \\ V_P = +V_{sat} \frac{R_2}{R_2+R_3} + \frac{-V_{ramp} R_3}{R_2+R_3} & \\ \Rightarrow 0 = " " & \\ \Rightarrow +V_{sat} \frac{R_2}{R_2+R_3} &= -\left(\frac{V_{ramp} R_3}{R_2+R_3} \right) \\ \Rightarrow -V_{ramp} &= -(V_{sat} \frac{R_3}{R_2}) \end{aligned}$$

$$-V_{ramp} + \frac{R_2}{R_2+R_3} \left[+V_{sat} - (-V_{ramp}) \right] = 0$$

$$-V_{ramp} + \left(\frac{R_2}{R_2+R_3} \right) V_{ramp} = -\left(\frac{R_2}{R_2+R_3} \right) V_{sat}$$

$$\Rightarrow \frac{R_2}{R_2+R_3} V_{ramp} = \frac{R_2}{R_2+R_3} V_{sat}$$

$$\Rightarrow -V_{ramp} = -\frac{R_2}{R_3} (+V_{sat}). \quad \text{--- (2)}$$

By, when schmitt trigger opamp is at $-V_{sat}$,

$$V_{ramp} = -\frac{R_2}{R_3} (-V_{sat}) \quad \text{--- (3)}$$

The peak-peak value of triangular wave can be given as

$$\begin{aligned} V_{o(P-P)} &= +V_{ramp} - (-V_{ramp}) \\ &= -\frac{R_2}{R_3} (-V_{sat}) - \left(-\frac{R_2}{R_3} \right) (+V_{sat}) \\ &= \frac{R_2}{R_3} V_{sat} + \frac{R_2}{R_3} V_{sat}. \end{aligned}$$

$$\boxed{V_{o(P-P)} = \frac{2R_2}{R_3} V_{sat}}$$

The time taken by the o/p to swing from $-V_{sat}$ to $+V_{sat}$ is "T/2".

The time can be calculated by integrator o/p.

$$V_o(p-p) = \frac{-1}{R_1 C_1} \int_0^{T/2} (-V_{sat}) dt$$

$$= \frac{V_{sat}}{R_1 C_1} (t) \Big|_0^{T/2} = \frac{V_{sat}}{R_1 C_1} \left(\frac{T}{2} \right)$$

$$\Rightarrow T = \frac{2 R_1 C_1 V_o(p-p)}{V_{sat}}$$

Sub. value $V_o(p-p)$, we get

$$T = \frac{2 R_1 C_1 \left(\frac{2 R_2}{R_3} V_{sat} \right)}{V_{sat}} \Rightarrow T = \frac{4 R_1 C_1 R_2}{R_3}$$

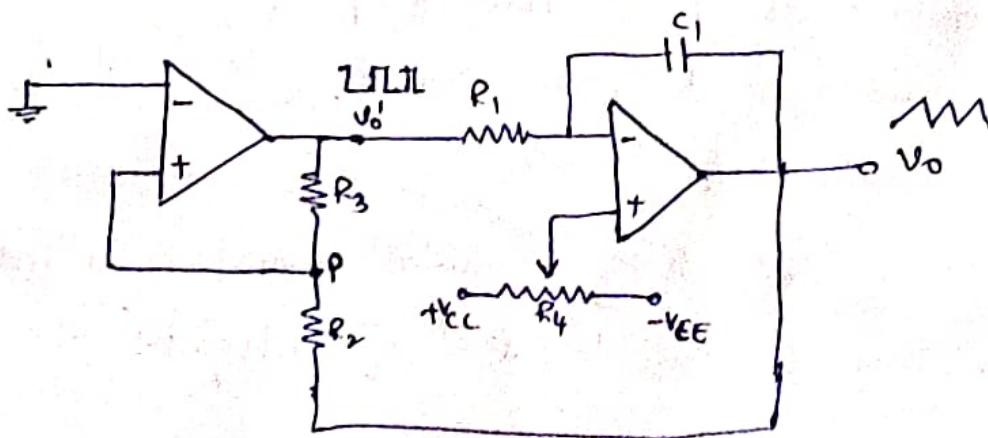
\therefore Frequency of oscillations is given by,

$$f_0 = \frac{1}{T} \Rightarrow f_0 = \frac{R_3}{4 R_1 C_1 R_2}$$

Sawtooth wave Generator :-

Unlike triangular wave, sawtooth wave has unequal rise time and fall time. That is, it may fall negatively many times faster than it rises positively or vice versa.

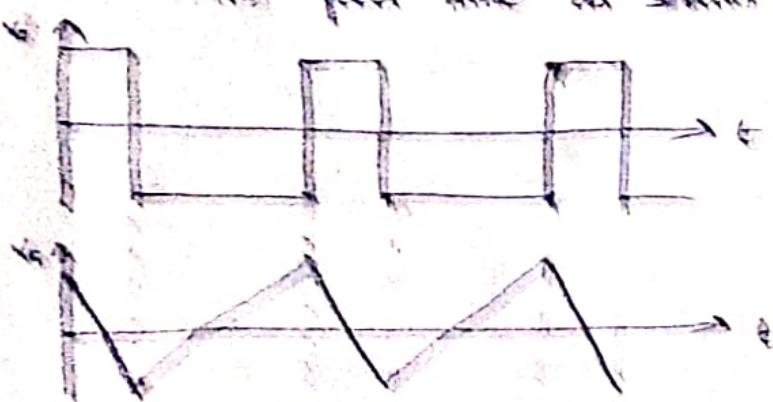
The sawtooth wave generator can be implemented by slightly modifying the triangular wave generator, as shown in below fig.



Here, the non-inverting terminal of the integrator is driven by the voltage set between $+V_{cc}$ to $-V_{ee}$ by the potentiometer. Depending on the 'Ri' setting, a certain d.c. level is added in the o/p of the integrator.

The o/p voltage of the integrator decides the effective voltage at point P, added d.c. level in the o/p of integrator will affect the duty cycle of the compared o/p.

When the voltage at the non-inverting terminal of the integrator is +ve, the duty cycle is less than 50%, resulting longer pulse time than fall time as shown in below fig.



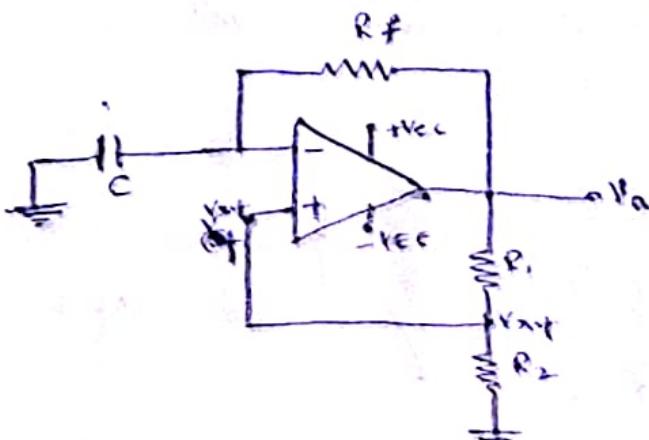
On the other hand, when the voltage at non-inverting terminal is -ve, the duty cycle is greater than 50% and pulse time is less than fall time.

It is important to note that freq. of switch waveform decreases when voltage at non-inverting terminal of integrator approaches to $(+V_{cc})$.

However, the amplitude of switch waveform is independent of setting of the terminal of integrator.

square wave generator:- (stable multivibrator).

A simple op-amp square wave generator is shown in below figure, also called as free running oscillator.



The principle of generation of square wave op is to force an op-amp to operate in saturation region.

The fraction of op voltage fed back to in terminal. Thus the reference voltage at the in terminal is $\left(\frac{R_2}{R_1+R_2}\right)V_o = \beta V_o$.

It may be $\beta V_o < -V_{sat}$ or $\beta V_o > +V_{sat}$.

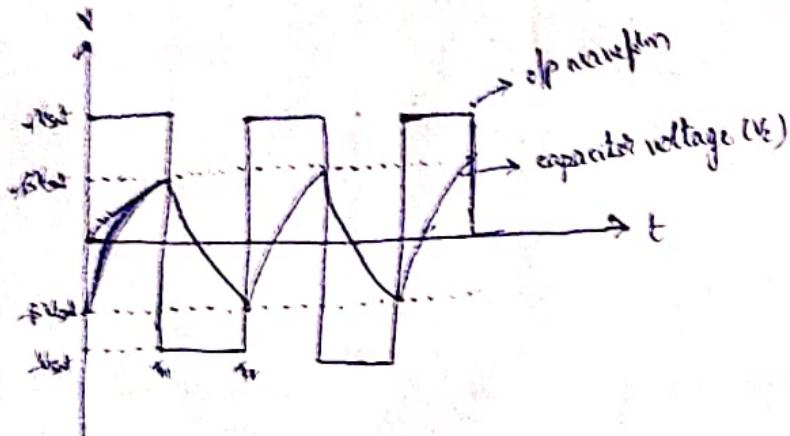
When power is turned 'on', V_o automatically swings either to +V_{sat} or to -V_{sat}. Since these are the only stable states allowed by the Schmidt trigger.

Assume V_o = +V_{sat}, then the capacitor starts charging towards -V_{sat} through feedback path provided by R₂ to the inverting in. As long as the capacitor voltage 'V' is less than "+V_{sat}", the op voltage remains at +V_{sat}.

Whenever 'V' changes to a value greater than "+V_{sat}", the op voltage switches from "+V_{sat}" to "-V_{sat}" and V_o = -V_{sat}. As V_o switches to -V_{sat}, the capacitor starts discharging via R₂ towards -V_{sat}.

If the capacitive voltage (V_c) becomes less than $-\beta V_{sat}$, the diode begins conductive to A_2 . So that the process is repeating.

Once the initial cycle is completed, the waveform becomes periodic. The diop waveform of capacitive voltage shown below.



This gives only

N.T.S. - P

The frequency of oscillation is determined by the time taken by capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa.

The voltage across capacitor as a function of time is given by,

$$V_c(t) = V_{final} (V_{max} - V_{final}) e^{-t/R_C} \rightarrow ①$$

where $V_{initial} = -\beta V_{sat}$ (Initial voltage)

$V_{final} = +\beta V_{sat}$ (voltage towards which capacitor is charging)

$$\therefore V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/R_C}$$

$$\Rightarrow V_c(t) = V_{sat} - V_{sat} (1 + \beta) e^{-t/R_C} \rightarrow ②$$

At $t = T_1$, the voltage across capacitor is $+\beta V_{sat}$

$$\therefore V_c(T_1) = \beta V_{sat}$$

$$\Rightarrow \beta V_{sat} = V_{sat} - V_{sat} (1 + \beta) e^{-T_1/R_C} \quad [\because \text{From } ②]$$

$$\Rightarrow \beta = 1 - (1 + \beta) e^{-T_1/R_C}$$

If $R_1 = R_2$,

∴ Frequency

$$(1+\beta) e^{-T_1/\tau_F} = 1 - \beta$$

$$e^{T_1/\tau_F} = \frac{1-\beta}{1+\beta}$$

$$e^{T_1/\tau_F} = \frac{1-\beta}{1-\beta}$$

$$\Rightarrow T_1/\tau_F = \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\Rightarrow T_1 = R_F \ln\left[\frac{1+\beta}{1-\beta}\right]$$

half period, the total time period (T) is,

$$T = 2T_1$$

$$\Rightarrow T = 2R_F \ln\left[\frac{1+\beta}{1-\beta}\right]$$

$$\beta = \frac{R_2}{R_1+R_2}$$

$$T = 2R_F C \ln\left[\frac{1 + \frac{R_2}{R_1+R_2}}{1 - \frac{R_2}{R_1+R_2}}\right]$$

$$T = 2R_F C \ln\left[\frac{R_1+R_2+R_2}{R_1+R_2-R_2}\right]$$

$$T = 2R_F C \ln\left[\frac{R_1+2R_2}{R_1}\right]$$

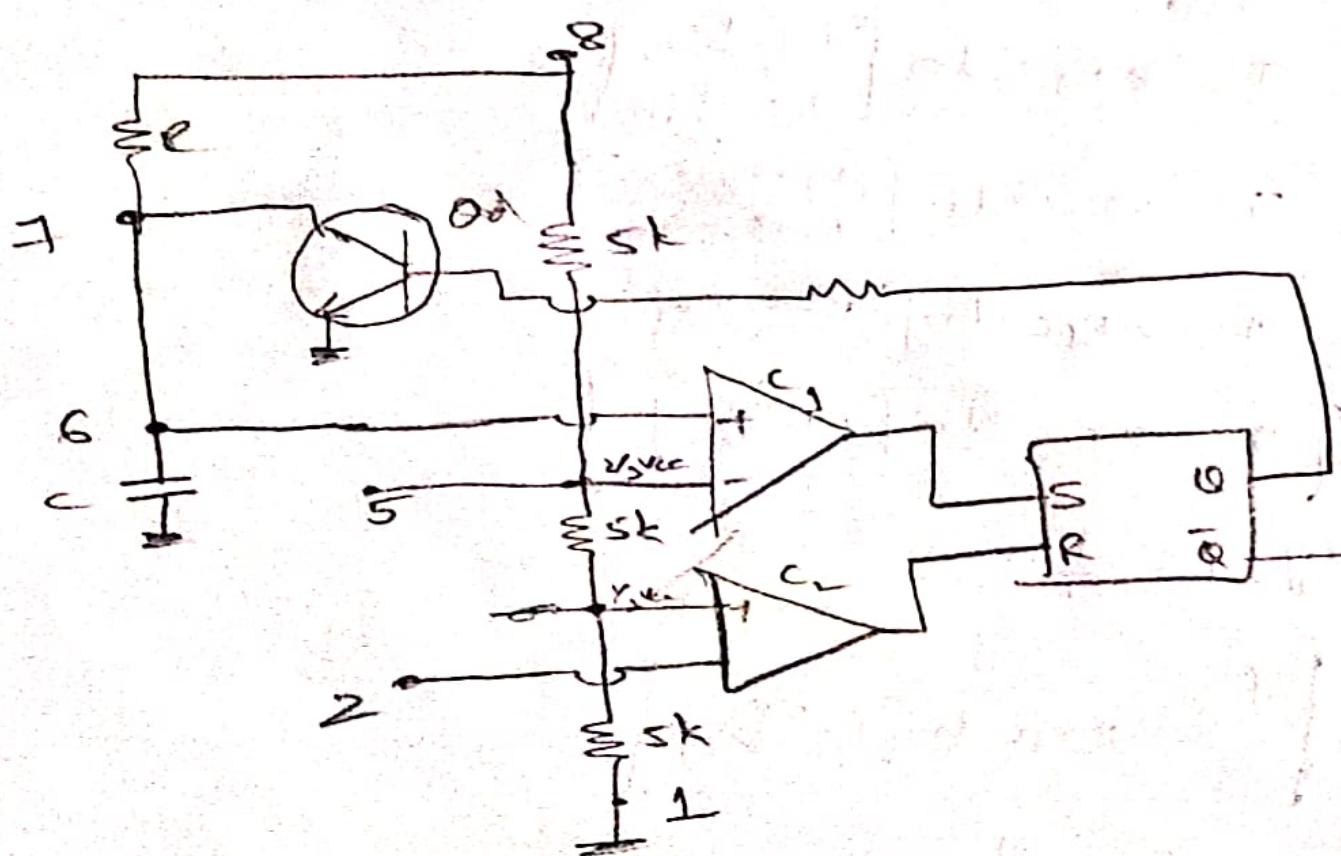
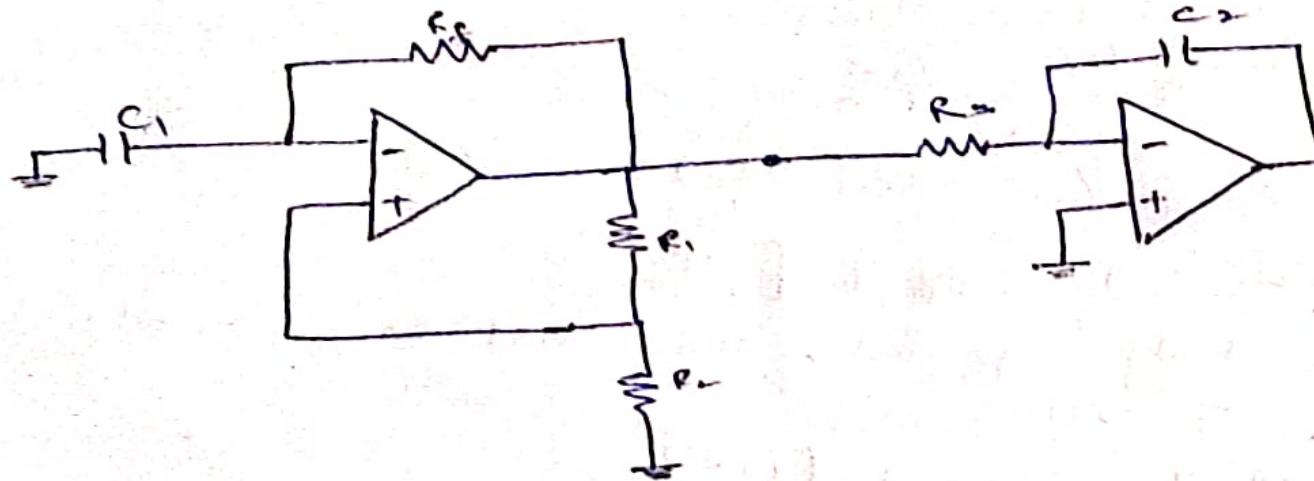
$$T = 2R_F C \ln\left[1 + \frac{2R_2}{R_1}\right]$$

$$\text{cy. } f = \frac{1}{T}$$

$$f = \frac{1}{2R_F C \ln\left[1 + \frac{2R_2}{R_1}\right]}$$

$$f = \frac{1}{2R_F C \ln(3)}$$

Triangular wave generator :-

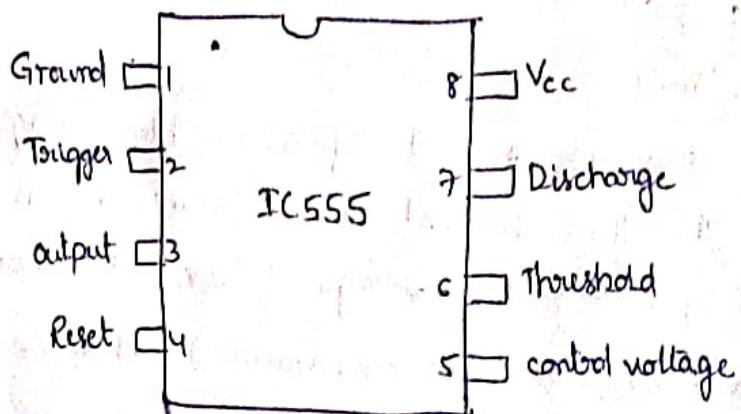


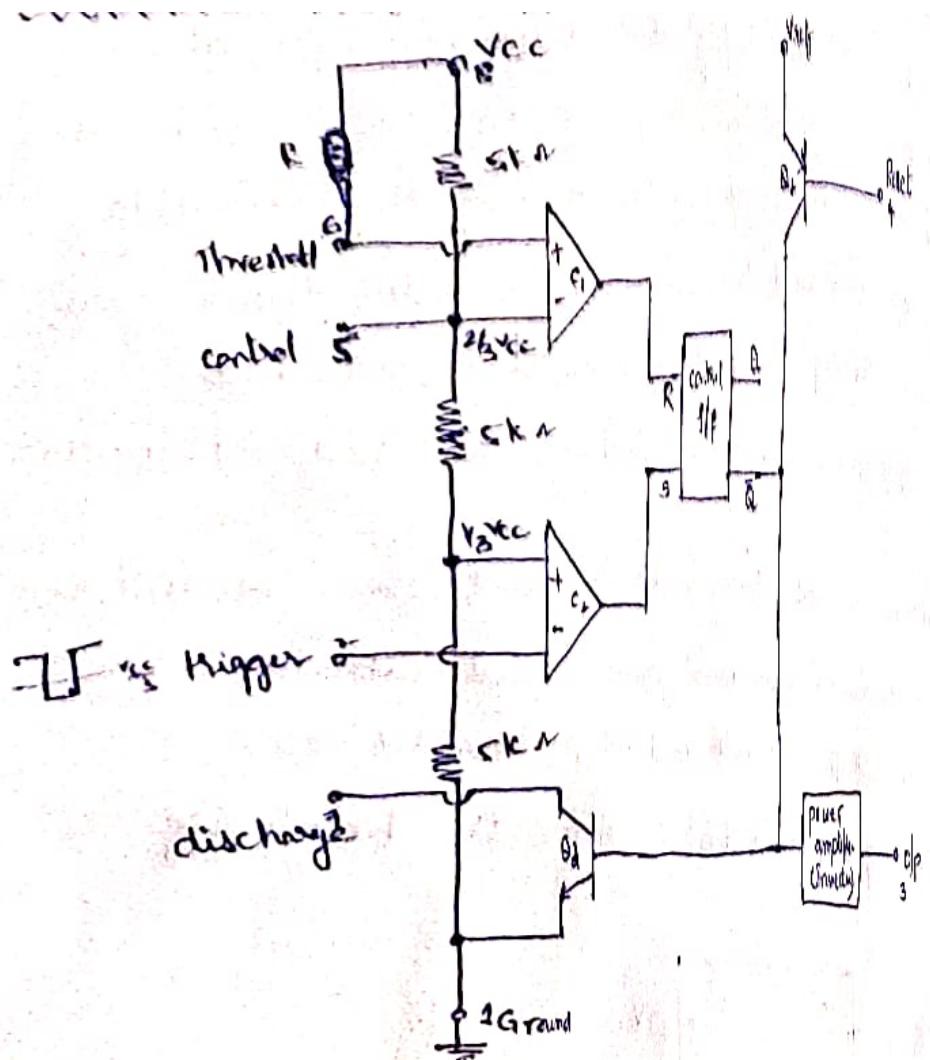
IC555 Timer:-

The 555 timer is a highly stable device for generating accurate time delay or oscillations. It is an 8-pin DIP IC, also available in 14-pin DIP. A single 555 timer can provide time delay ranging from micro seconds to hours, whereas a counter timer can have a max. timing range of days. It can be used with supply voltage of +5V to 18V. It is compatible with both TTL & CMOS circuits.

It is used in various timing applications such as oscillators, pulse generators, ramp & square wave generators, multivibrators, burglar alarm, traffic light control and voltage monitor etc.

The pin diagram of IC 555 timer is shown in below figure.





The above diagram shows the functional block diagram of IC 555 timer. The three internal resistors ($5k\Omega$) act as voltage divider, providing bias voltage of $\frac{2}{3}V_{cc}$ to upper comparator (C_1) and $\frac{1}{3}V_{cc}$ to lower comparator (C_2), where V_{cc} is the supply voltage. These two voltages fix the necessary compare threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically, by applying a modulation voltage to the controller control voltage (pin 5).

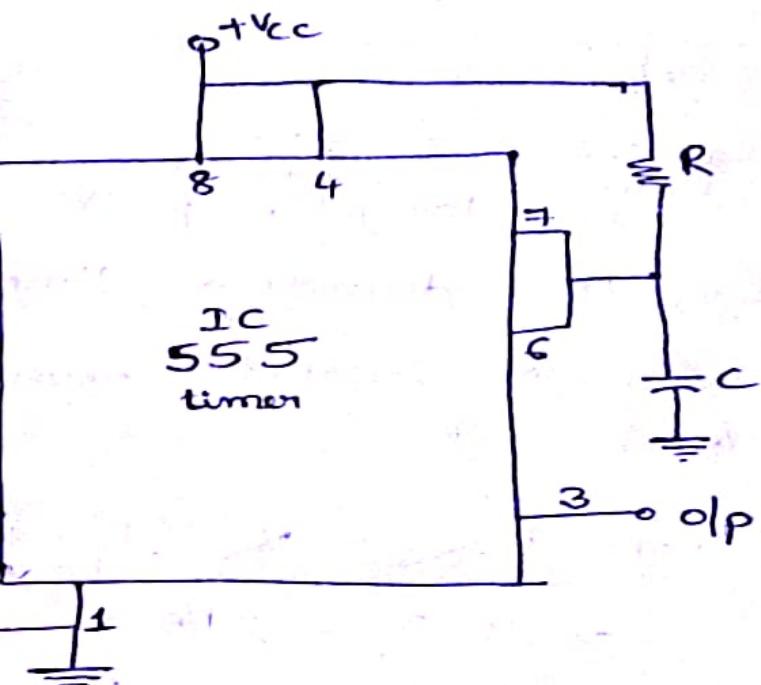
In stable state, the op \bar{Q} of Hf is high. This makes off low because power amplifier is basically inverter.

A 'low' going trigger pulse is applied and should have



triggered, the o/p of lower comparator goes high. This drives the flip-flop ($Q=1, \bar{Q}=0$). The low \bar{Q} makes Q_1 off. Due to this, there is no current through the timing capacitor 'C'. In the excursion, when threshold voltage passes through the o/p of upper comparator goes high, this negates Q_1 , $\bar{Q}=1$. Now, the output of the inverter stage (Q_1) goes high. The input provides a mechanism to reset the flip-flop. So, we can say:-

The timer can be operated as monostable multivibrator by connecting an external resistor and a capacitor as shown in the figure. This circuit has only one stable and one metastable state. When trigger is applied, it goes at the o/p and returns back to its

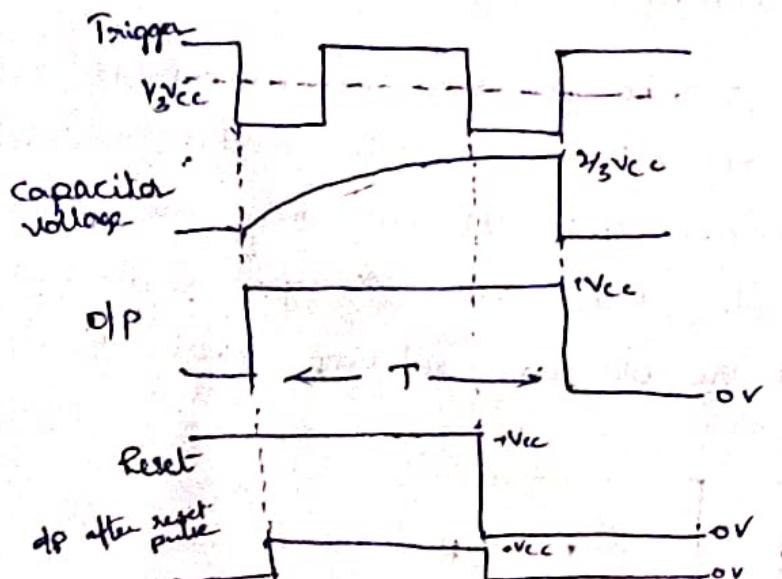


When the flip-flop is reset, \bar{Q} is high. This drives the inverter, thus clamping the external timing capacitor 'C' to ground. It remains at ground potential.

Now, the voltage across 'C' passes through $V_{cc}/2$, $\bar{Q}=0$. Due to this Q_1 gets on and the short circuit at capacitor 'C' is released.

The timing cycle now begins. Since 'C' is unclamped, voltage across it rises exponentially through 'R' towards V_{CC} with a time constant ' RC '.

After a time period ' T ', the capacitor voltage is just greater than $\frac{2}{3}V_{CC}$ and upper comparator reaches the flip. due to this $\bar{Q}=1$ & $Q=0$. thereby discharging capacitor 'C' rapidly to ground potential. The o/p returns to zero. as shown in below.



The pulse width of this rectangular pulse is controlled by the charging time of capacitor. This depends on time constant RC .

The voltage across capacitor increases exponentially and is given by, $V_C = V_{CC}(1 - e^{-t/RC})$

$$\text{at time } T \text{ if } V_C = \frac{2}{3}V_{CC}, \text{ then } \frac{2}{3}V_{CC} = V_{CC}(1 - e^{-T/RC})$$

$$\Rightarrow 1 - \frac{2}{3} = e^{-T/RC}$$

$$\Rightarrow -T/RC = \ln\left(\frac{1}{3}\right)$$

$$\Rightarrow -T/RC = -1.0986$$

$$\Rightarrow t = 1.0986RC$$

$$\Rightarrow t = 1.1RC$$

\therefore pulse width = $1.1RC$

Applications of Monostable multivibrator:-

From the above equation it is noted that timing interval is independent of supply voltage. Once the ckt is triggered, the o/p remains high until time 'T' elapses, which depends only on R & C. Any additional trigger pulse coming during this time will not change the o/p state. However, a negative going reset pulse at pin-4 can change o/p.

Applications of monostable multivibrator:-

(i) Frequency divider:-

The monostable multivibrator ckt can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of triggering i/p signal.

The monostable multivibrator will be triggered by the first negative going edge of trigger i/p, which will make o/p to go to its high state.

The o/p will remain high for the period equal to "timing - interval". As timing interval is greater than time period of the trigger i/p, o/p will still be high when the second negative going pulse occurs.

The monostable will, however, be retriggered on the third negative-going pulse.

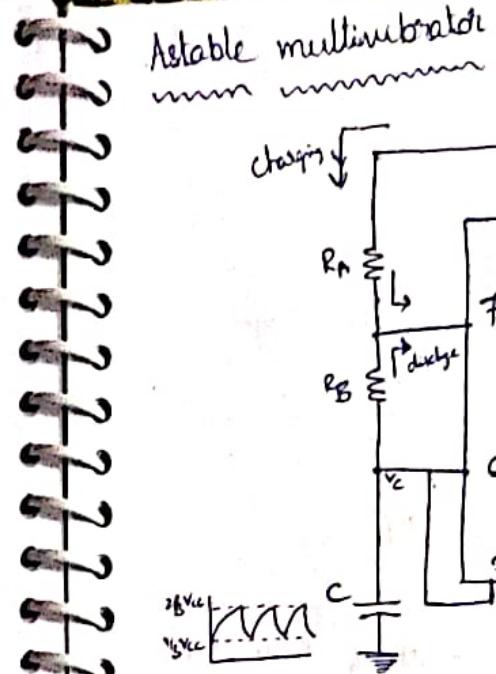
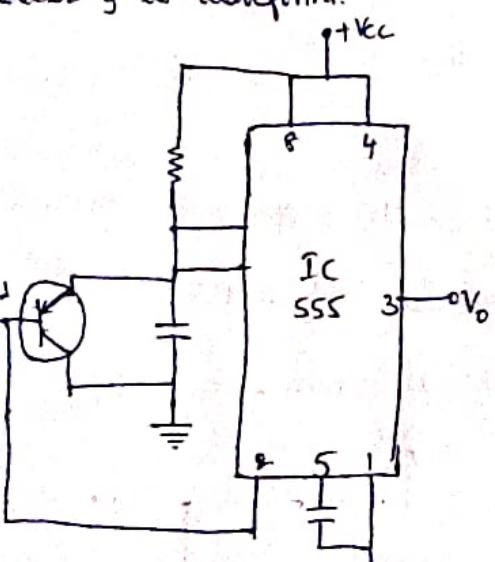
Therefore, monostable triggers on every other pulse of the trigger i/p, so there is only one o/p for every two i/p pulses, thus trigger sig is divided by '2'.

The current ' I_C ', charges the capacitor 'C' at a constant rate towards $+V_{CC}$. But, when, voltage at pin-6 (i.e. V_C) becomes $\frac{2}{3}V_{CC}$, the comparator makes internal transistor ' Q_1 '-ON with no time.

But while discharging when V_C becomes $\frac{1}{3}V_{CC}$, the second comparator makes Q_2 -OFF and C starts charging.

~~Multivibrator~~ (iv) Missing Pulse Detector :-

the below figure shows the missing pulse detector & its waveform.



the above figure
multivibrator. The three
the circuit contains two
This circuit has no start
automatically. Hence,
non-sinusoidal oscillation.

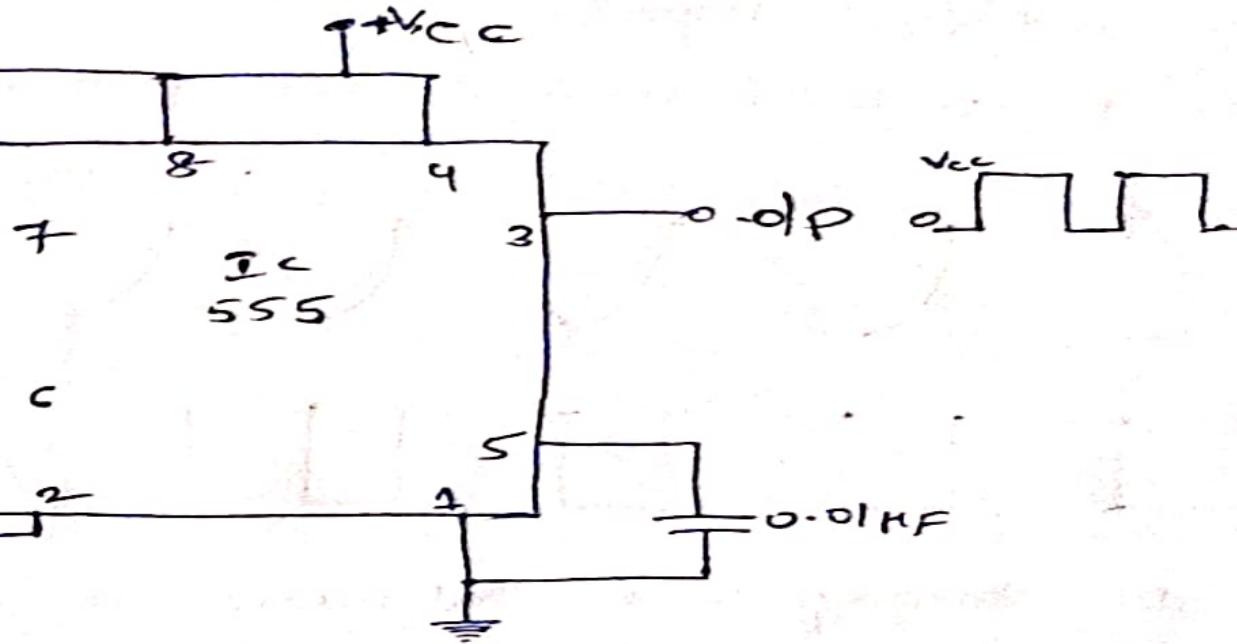
~~Operation :-~~

When power supply is given, capacitor 'C' charges through resistor R_p . During this time off.

When capacitor 'C' charges, the control flip-flop ' Q_1 ' turns ON. 'C' starts discharging with a constant $R_p \cdot C$.

During the discharge, the lower comparator high level uncamps the upper com-

using IC 555 :-



shows the IC 555 connected as an astable multivibrator. o/p is connected to the trigger input. and no external resistors R_A, R_B and a capacitor 'c'. It has two stable states. The circuit changes its state periodically. The operation is also called 'free running oscillator'.

When supply V_{CC} is connected, the external timing capacitor 'c' starts charging towards V_{CC} with time constant (R_A+R_B)·C. When o/p is high (at V_{CC})

or voltage equals to ($\frac{2}{3}V_{CC}$), the upper comparator goes high so that $\bar{Q}=1$. This makes Q₁-on and capacitor 'c' starts discharging towards ground through R_B & Q₁, with time

constant (R_B·C). When o/p is low (at $\frac{1}{3}V_{CC}$) the lower comparator goes high so that $\bar{Q}=0$. This makes Q₁-off and capacitor 'c' starts charging again with time constant (R_A+R_B)·C.

The capacitor 'c' thus periodically charged and discharged below $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$ respectively. The below fig. shows the d/p wave of capacitor voltage wave form.



The capacitor charging time that means the length of time the d/p remains high is calculated as follows.

The capacitor voltage V_c is given by,

$$V_c = V_{CC} \left(1 - e^{-t/RC} \right) \quad \text{[since lowpass RC circuit subjected to a step input]}.$$

The capacitor charges to max. voltage of $V_c = \frac{2}{3}V_{CC}$ at that time t_1 .
and the time t_1 taken to charge from 0 to $\frac{2}{3}V_{CC}$ is

$$\therefore \frac{2}{3}V_{CC} = V_{CC} \left[1 - e^{-t_1/RC} \right]$$

$$\Rightarrow \frac{2}{3} = 1 - e^{-t_1/RC}$$

$$\Rightarrow e^{-t_1/RC} = 1 - \frac{2}{3}$$

$$\Rightarrow t_1 = 1.09RC$$

The time t_2 taken to charge to $\frac{1}{3}V_{CC}$ is,

$$\frac{1}{3}V_{CC} = V_{CC} \left(1 - e^{t_2/RC} \right)$$

$$\Rightarrow t_2 = 0.405RC$$

So, the time taken to charge $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$ is

$$t_{\text{high}} = t_1 - t_2$$

$$= 1.09RC - 0.405RC = 0.69RC$$

$$\therefore [t_{\text{high}} = 0.69(R_{A,B})C]$$

The d.p. is low while the capacitor C is charged and the voltage across capacitor is given as

$$V_{RC} = \frac{1}{2} V_{DC} e^{-t/RC}$$

$$\Rightarrow \frac{1}{2} = e^{-t/RC} \Rightarrow -t/RC = \ln(\frac{1}{2})$$

$$\Rightarrow t_{low} = 0.69 RC$$

For astable M.V. $t_{low} = 0.69 R_B C$

\therefore The total time is

$$T = t_{high} + t_{low}$$

$$= 0.69 (R_A + R_B) C + 0.69 R_B C$$

$$\boxed{T = 0.69 (R_A + 2R_B) C}$$

The freq. of oscillation is given by

$$f = \frac{1}{T} \Rightarrow f = \frac{1}{0.69 (R_A + 2R_B) C}$$

$$\boxed{f = \frac{1.45}{(R_A + 2R_B) C}}$$

Duty cycle (D) \rightarrow It is the ratio of ON time to the total period.

$$D = \frac{t_{on}}{T}$$

$$\% D = \frac{0.69 (R_A + R_B) C}{0.69 (R_A + 2R_B) C} \times 100$$

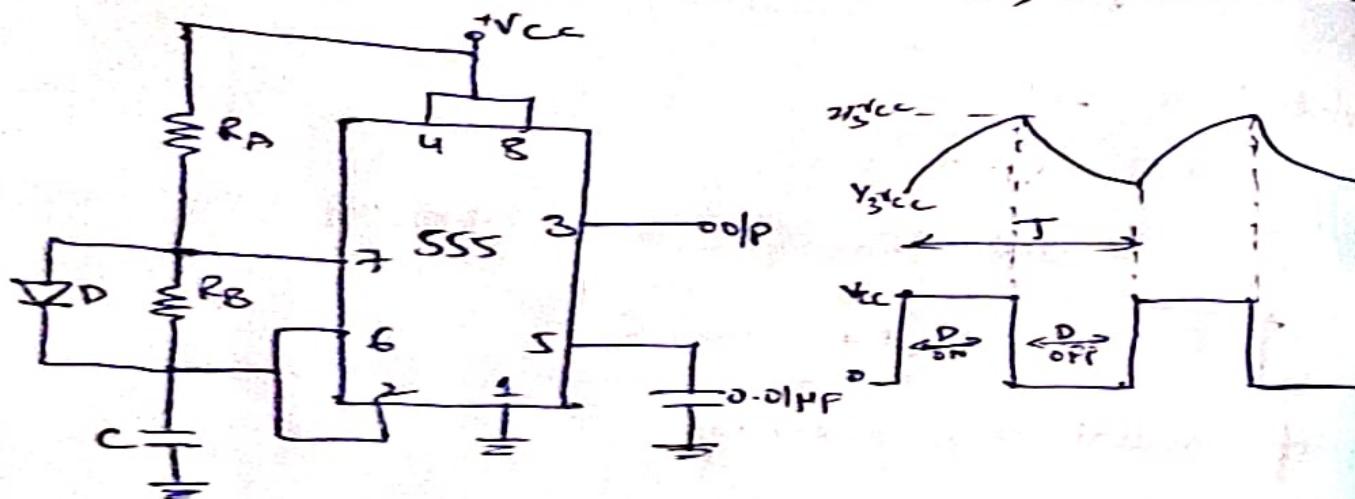
$$\Rightarrow \% D = \frac{(R_A + R_B)}{2(R_A + 2R_B)} \times 100$$

Applications of astable multivibrator :-

(i) Square Wave Generator :-

It can be observed from the expression of duty cycle that exact 50% duty cycle is not possible.

To get exactly 50% duty cycle i.e., square wave necessary to modify the astable timer ckt, as shown in



In the modified ckt, the capacitor 'C' charges through diode 'D' and discharges through 'RB'. To get 50% duty cycle adjusted such that it is equal to the sum of $R_A + R_B$ of diode 'D'. Usually potentiometer is used for exact resistors.

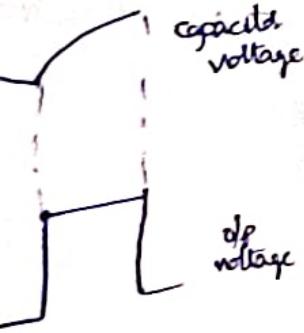
(ii) Voltage controlled oscillator (VCO) :-

The fig. shows VCO. It is basically an astable multivibrator ckt with variable control voltage.

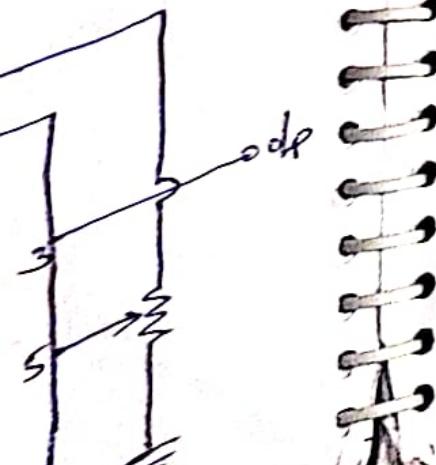
In this ckt, the control voltage is externally set by the potentiometer.

With change in the control voltage the threshold voltage changes and thus the upper threshold voltage changes and thus required to charge & discharge capacitor changes.

cycle. that, is
possible to achieve
wave o/p, it is
as below.



through R_A and
cycle, R_S is
forward resistance
& adjustments of



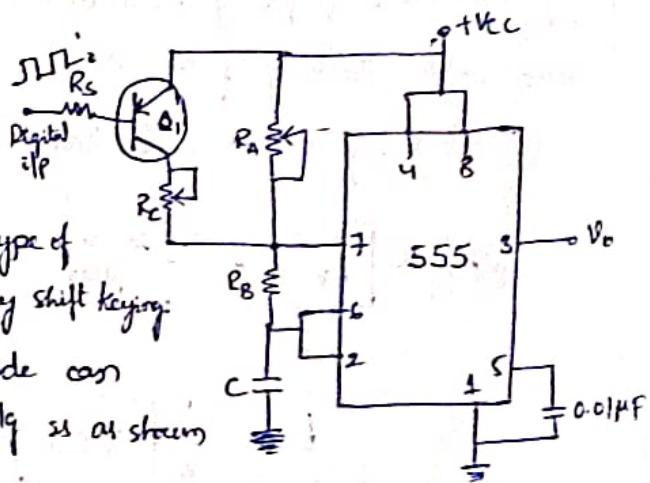
As a result, the freq. of the o/p voltage changes. If the control voltage is increased, the capacitor will take more time to charge and discharge and therefore freq. will decrease. On the other hand, if control voltage is decreased, the freq. will increase. Thus, by varying control voltage, we can change the freq. Hence it is called V.C.D.

P(iii) FSK Generator:-

In digital data comm.,
binary code is transmitted by
shifting a carrier freq. by two

for preset frequencies. This type of
transmission is called frequency shift keying.

A 555 timer in astable mode can
be used to generate FSK sig. as shown
in figure.



When digital i/p is HIGH, the transistor 'Q1' is OFF and 555 timer
works in a normal astable mode. The freq. of o/p waveform can be given

as,

$$f_o = \frac{1.45}{(R_A + 2R_B)C}$$

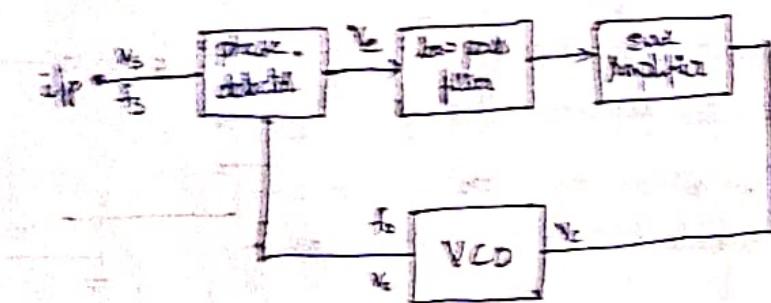
When i/p is LOW, the transistor 'Q1' is ON and connects
resistance R_C in parallel with R_A . The o/p freq. is now given by.

$$f_o = \frac{1.45}{(R_{A||R_C} + 2R_B)C}$$

Phase locked loop (PLL) :-

PLL is an equivalent block of linear system. A PLL is basically a closed loop system designed to lock the output frequency and phase to the frequency and phase of an input signal. It is used in the applications such as frequency synthesis, frequency translation/demodulation, AM detector, FSK demodulation, tracking filter etc.

The below figure shows the basic block diagram of PLL.



It consists of :-

- phase detector
- low pass filter
- summing junction
- voltage controlled oscillator.

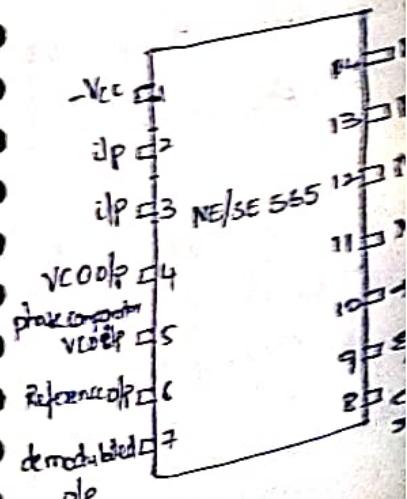
The phase detector compares the input freq. and op freq. and generates the difference and sig. The o/p of phase detector is applied to LPF to remove high freq noise from the dc voltage. The o/p of LPF is referred to as control voltage for VCO.

A voltage controlled oscillator is an oscillator circuit in which freq. of oscillations can be controlled by an externally applied voltage. It provides linear relationship b/w applied voltage and the oscillation frequency. When control voltage is zero, VCO is in free running mode and its o/p frequency is called center freq.f_c.

the error signal
given by $f = f_c + \Delta f$
the voltage control
charge is o/p $\frac{d\theta}{dt}$
o/p of o/p frequency
in this action is
the o/p frequency of
Once the two freq.
locked. Once locked,
then o/p goes into
and phase lock.

IC 565 PLL :-

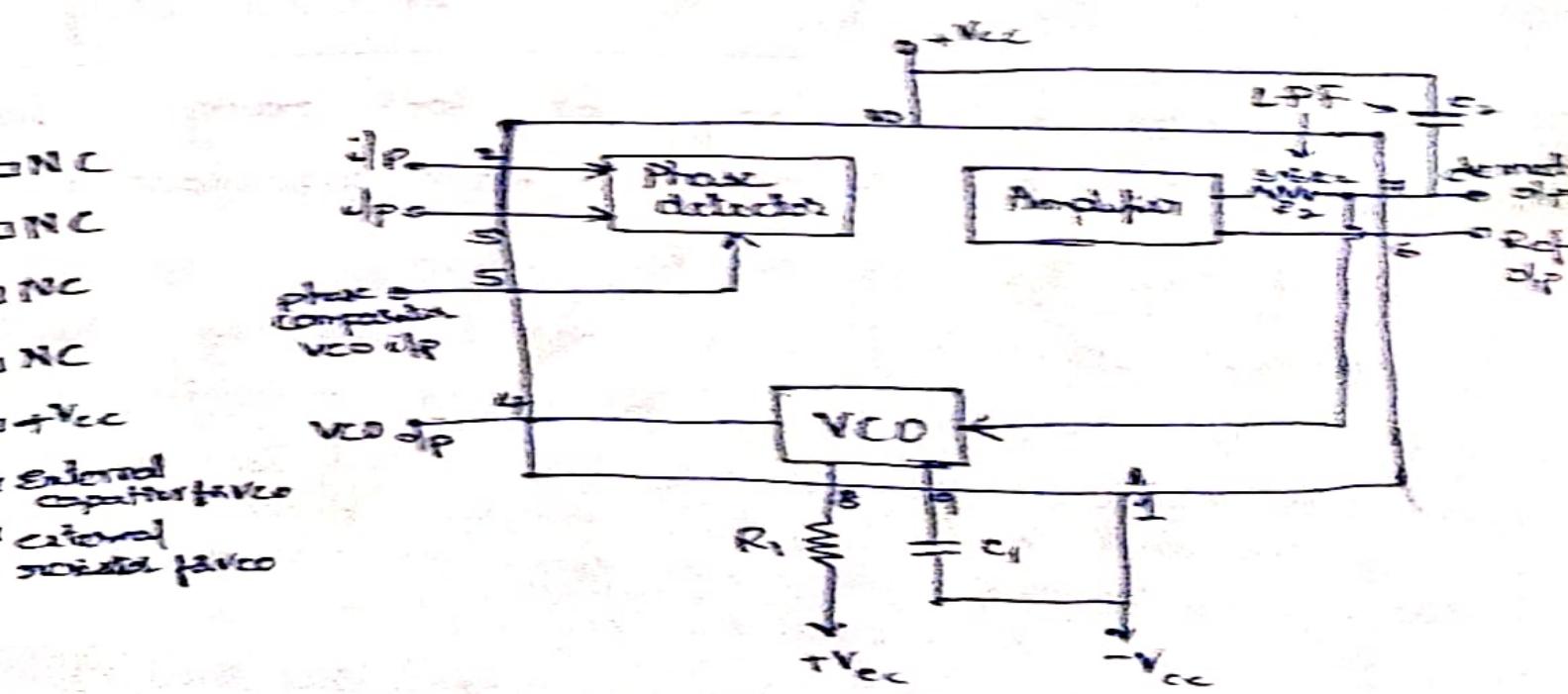
IC 565 is available
in package.
The pin configuration
below figure.



local voltage results in a shift in the VCO frequency. Since the local voltage - frequency coefficient is same as that of VCO, bias the VCO in the direction that reduces the difference between them.

This is commonly known as capturing. continues till VCO is same as the local signal frequency. Once they are same, the circuit is said to be locked. PLL tracks the frequency changes of the local signal through three states: free running, capture

Table in 14-pin DIP package and 10-pin metal can & block diagram of IC 565 PLL is shown in figure 4.



The centre frequency of the PLL is determined by the free-running freq. of the VCO and it is given as,

$$f_0 = \frac{0.25}{R_1 C_1} \text{ Hz} \quad -①$$

Where R_1 & C_1 are an external resistor and a capacitor connected to pin-8 & 9 respectively. The value of R_1 is selected in between $2k\Omega$ & $20k\Omega$. The VCO free running freq. is adjusted with R_1 & C_1 . A capacitor ' C_2 ' connected b/w pin-1 & positive supply forms a LPF with internal resistance of $3.6k\Omega$. A shunt ext b/w pin 14 & 5 connects the VCO o/p to phase comparator so as to compare it with V_s .

The lock range and capture range for 20565 PLL are given by the following eqns.

$$f_L = \pm \frac{8f_0}{V} \text{ Hz} \quad -②$$

Where, f_0 = free running freq. of VCO in Hz.

$$\Delta V = (+V_s) - (-V_s) \text{ volts.}$$

$$f_c = \pm \left[\frac{f_L}{2\pi(2.6)(10^3)(C_2)} \right]^{1/2} \quad -③$$

From eqn ②, we can say that, lock range increases with increase in i/p voltage but decreases with increase in supply voltage.

Important Definitions related to PLL:-

Lock range:- When PLL is locked, it can track freq. changes in the incoming sig. The range of frequencies over which the PLL can maintain lock with incoming sig is called lock range or tracking range. It is usually expressed as a % of f_0 , the VCO freq.

Capture range:- The range of frequencies over which the PLL can acquire lock with an i/p signal is called the capture range. It is also expressed as % of f_0 .

Pull-in time:- The total time taken by the PLL to establish a lock is called pull-in time. This depends on the initial phase and freq. differences b/w the two sig's as well as on the overall loop gain & B.W. of the low pass filter.

Phase detector:-

The phase detector is a component used in the PLL system. The phase detector compares the feedback frequency with the reference frequency to determine the phase difference between them.

There are two types of phase detectors:

(1) Analog phase detector

There are two types of analog phase detectors: switch type and balanced switch type.



(a)

The switch 's' is open as shown in above fig(a). The output V_o is zero.

When $\phi = 0^\circ$, i.e., when the o/p will be positive.

When $\phi = 90^\circ$, the o/p will be half of the cycle.

When $\phi = 180^\circ$: the o/p

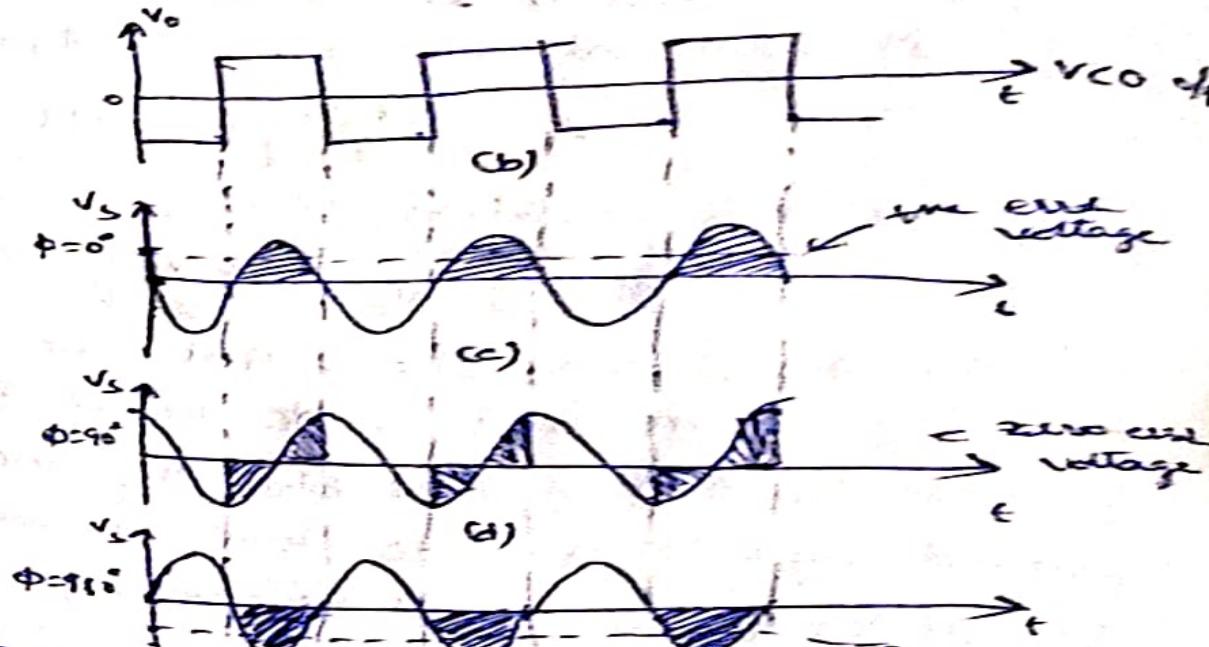
detection is the most important part of the phase detector compares the ilp frequency 'n' with f_{fo} and generates an op signal which is the sum of the two ilp signals.

Types of phase detectors - They are (i) Analog P.D. or :-

Types of analog phase detectors. They are:-
Balanced modulator type.

vector :-

$v_{\text{c o}}$

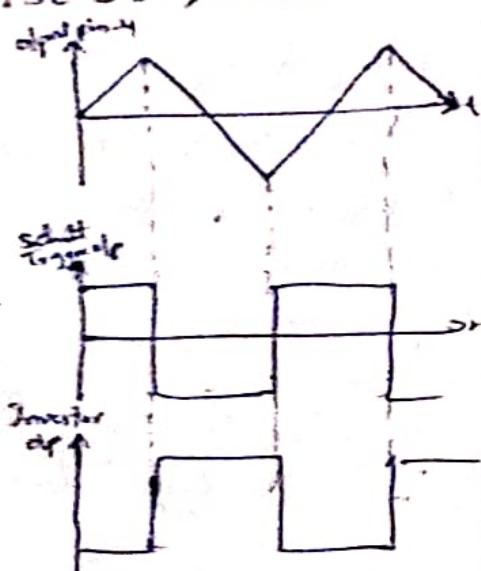
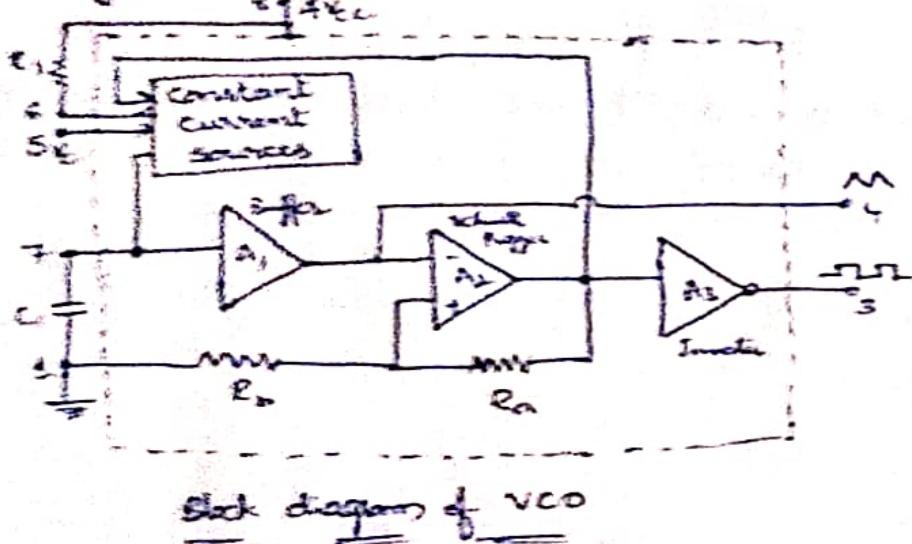


+ closed switch's. is closed by the sig coming from vco. as for the vco o/p, and otherwise the half ilp signal v_s is in phase with vco o/p v_o , one full cycle as shown in fig(c)

is fig(d), contains half portion of one cycle, will be the half cycle as shown in fig(e).

Voltage Controlled Oscillator (VCO):-

A VCO is an oscillator circuit in which frequency of oscillator can be controlled by externally applied voltage. The VCO provides linear relationship b/w the applied voltage and the oscillation frequency. Applied voltage is called control voltage. The control of frequency with the help of voltage is also called voltage to freq. conversion. Hence, it is also called as voltage to frequency converter. Practically, it is available in IC form as NE/SE 566, LM566 etc.



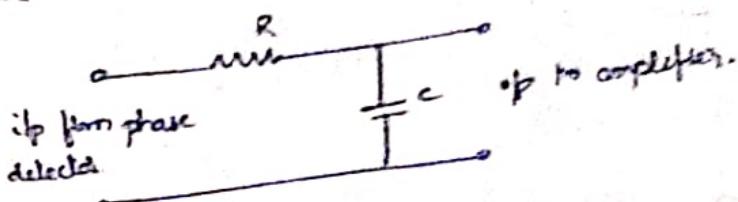
The op-amp A_1 is used as a buffer, $\frac{1}{A_2}$ is used as schmitt trigger & $\frac{1}{A_3}$ is used as inverter. Control voltage is applied at pin-5. The capacitor ' C_1 ' is linearly charged or discharged by a constant current source. The charging current can be controlled by controlling the voltage ' V_c ' at pin-5 set by varying ' R_1 '. This charging/discharging levels are determined by schmitt trigger.

Thus a triangular wave is generated due to alternate charging/discharging of the capacitor ' C_1 ' in linear manner. The triangular wave is applied to schmitt trigger circuit & it generates a square wave op. The square wave is fed to inverter & inverter output is fed back to the tri-state. The freq. of oscillations is given by,

$$f_o = \frac{2(V_{cc} - V_c)}{R_1 C_1 (\ln 2)}$$

Low pass filter :-

Here, the low pass filter not only removes the high freq. components and noise, but also controls the dynamic characteristics of the PLL. These char. include capture range, lock range, B.W. & transient response.

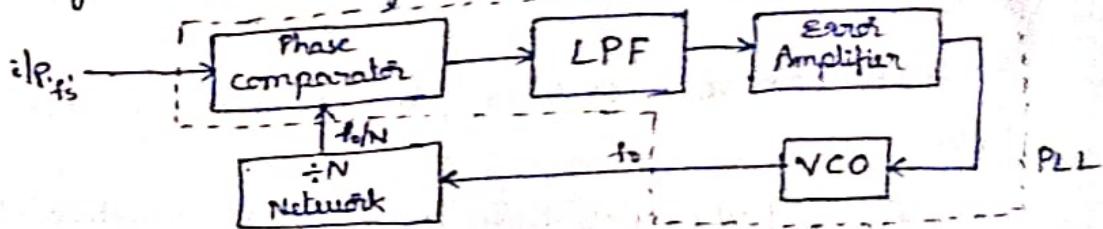


PLL Applications :-

A PLL may be used in many applications. Some of them are:-

(i) Frequency multiplier :-

The below diagram shows the block diagram of frequency multiplier using PLL 565.



Here, a $\div N$ n/w is inserted bw the VCO o/p and phase comparator i/p. since, the o/p of the divider is locked to the ifp frequency f_i , the VCO is actually running at a multiple of the ifp frequency. In the locked state, the VCO o/p freq. f_o is given by,

$$f_o = N f_i$$

By selecting proper divider by N n/w, we can obtain desired multiplication. For example, to obtain o/p frequency $f_o = 6 f_i$, a divide by N n/w should be equal to '6'.