Unit-II

Non-Linear Wave Shaping

The circuits for which the o/ps are non-sinusoidal for sinusoidal inputs are called nonlinear wave shaping circuits. e.g. clipping & clamping ckts.

* Clippers:

It means cutting and removing a part.

Clipping circuits are referred as voltage (or current) limiters, amplitude selectors or slicers.

Following configurations are possible.

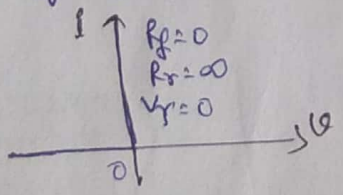
(i) a series combination of a diode, resistor and reference supply.

(ii) a n/w consisting of several diodes, resistor & ref. vge.

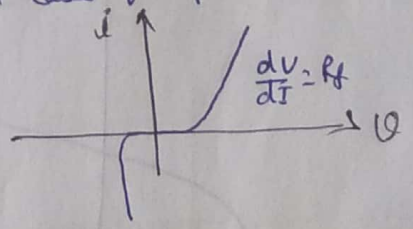
(iii) two emitter-coupled transistors operated as saturated difference amplifiers.

* Diode Clippers:

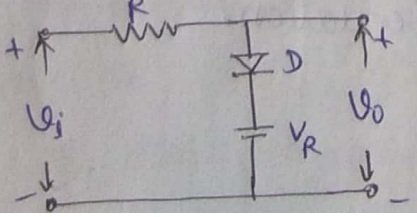
In case of an ideal diode



In case of practical diode.



The diode characteristics curve is piecewise linear and continuous. The pt of discontinuity occurs at the voltage V_γ, this pt of slope discontinuity is known as break.

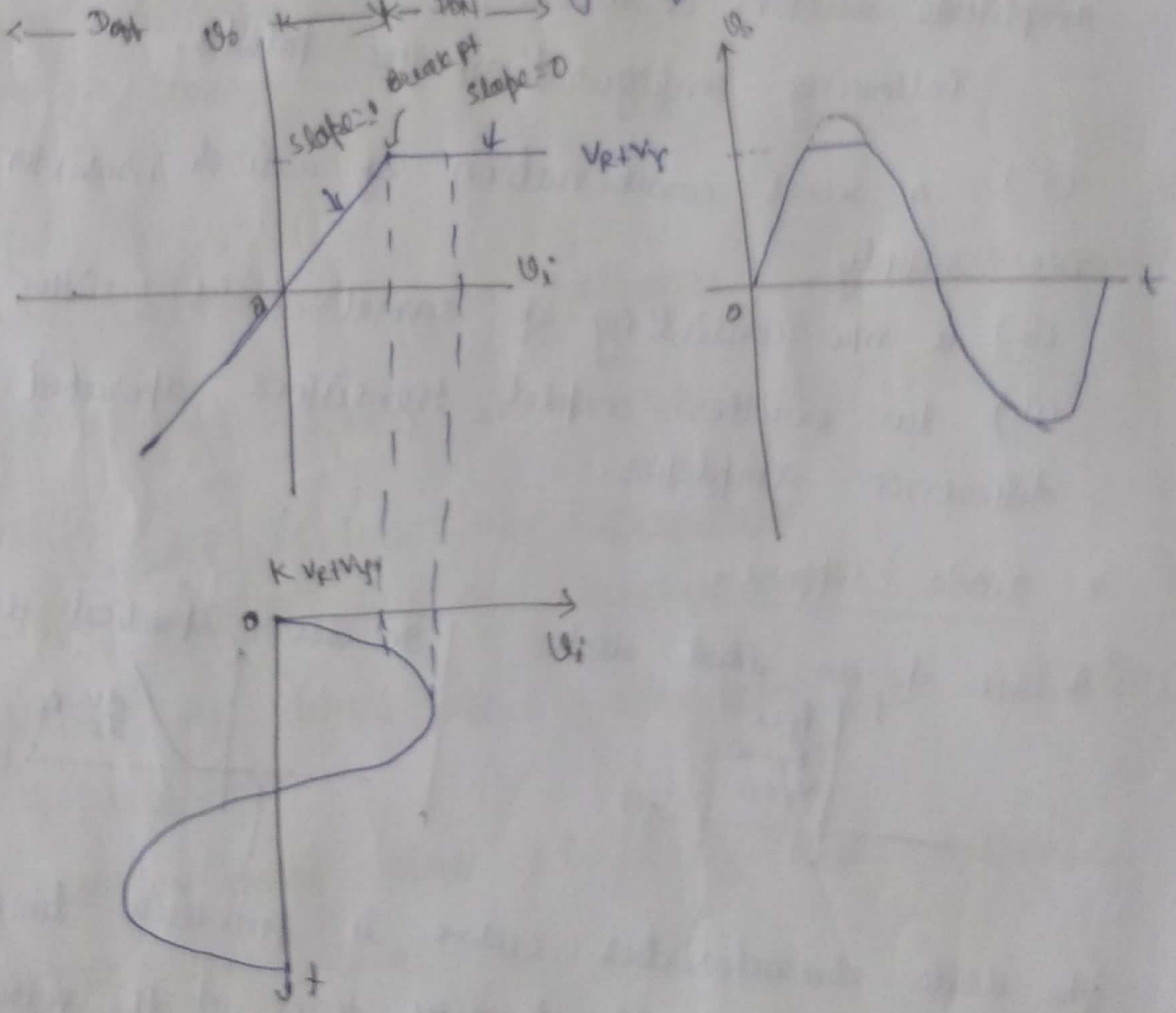


⇒ A break pt occurs at voltage $V_R + V_\gamma$. The left of the break pt, diode is reversed biased (OFF). ie for $v_i(t) < V_R + V_\gamma$. Here signal $v_i(t)$ is transmitted directly to the o/p.

→ The right of break pt., increment $\Delta v_i(t)$ in the i/p are attenuated and appear at the o/p as increments.

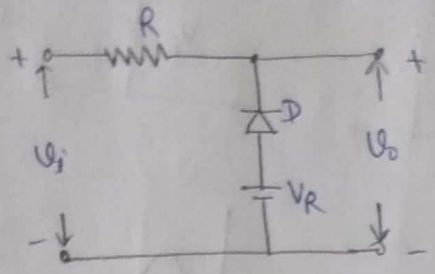
$$\Delta v_o(t) = \frac{\Delta v_i(t) \cdot R_f}{R_f + R}$$ where, R_f → diode forward resistance

→ The o/p appear as clipped off or sliced off. Normally, $V_R \gg V_\gamma$, so, V_R itself is limiting reference voltage.

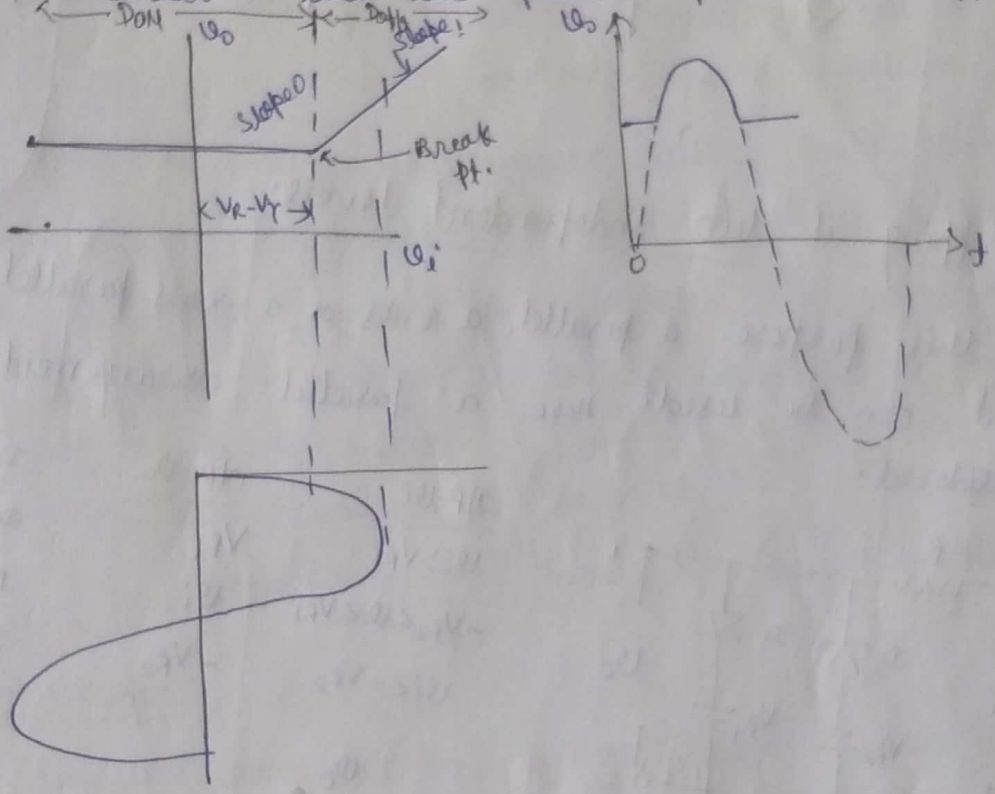


→ The voltage above $V_R + V_\gamma$ is attenuated. Below that level is transmitted without attenuation.

→ In other case direction of the diode is reversed.



The portion of waveform more than $V_R - V_\gamma$ is transmitted without attenuation but less positive portion is suppressed.



*→ Break region:

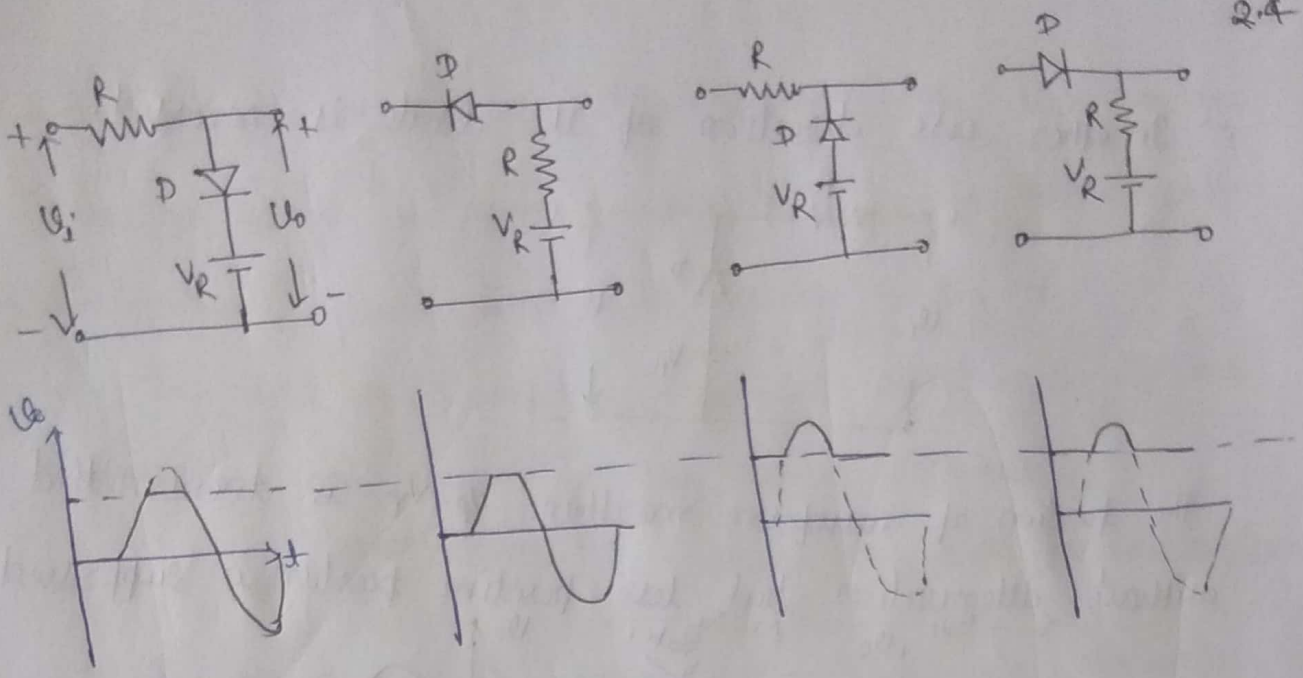
It is region of transition from unattenuated to attenuated transmission.

The diode current eqn is given as,

$$I = I_0(e^{V/\eta V_T} - 1)$$

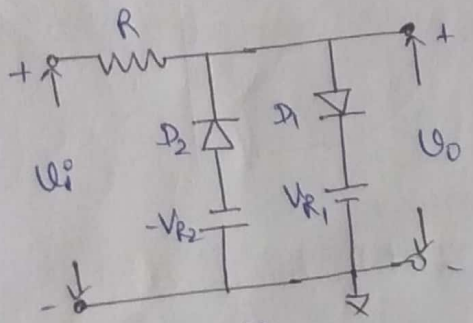
Beyond the break pt, current is large, which can be given as $I = I_0 e^{V/\eta V_T}$

& diode dynamic resistance, $r = \frac{\eta V_T}{I}$, $V_T = \frac{T}{11600}$

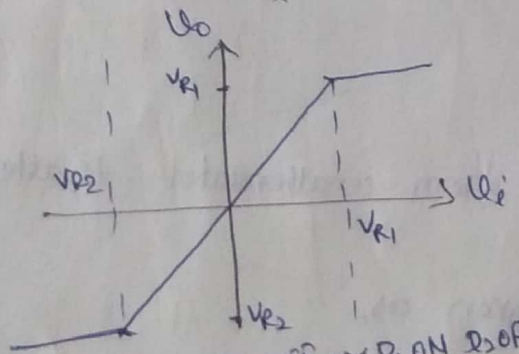


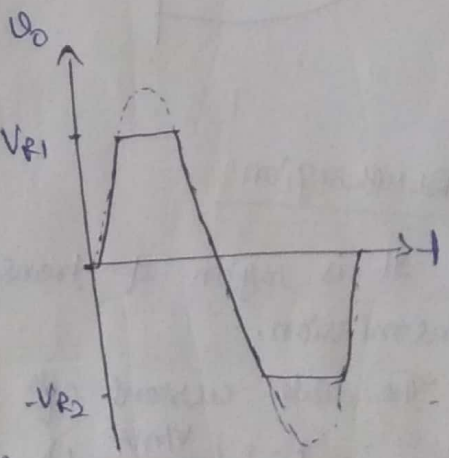
* Clipping at two independent levels:

For this purpose a parallel, a series or a series-parallel arrangement can be used. Here a parallel arrangement is considered.



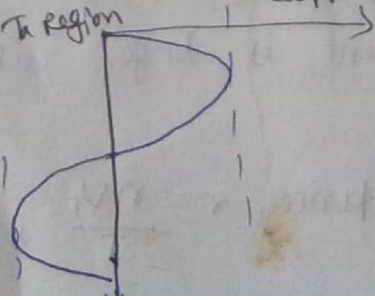
I/P, V_i	O/P, V_o	Diode
$V_i > V_{R1}$	V_{R1}	D_1 ON, D_2 OFF
$-V_{R2} < V_i < V_{R1}$	V_i	D_1 OFF, D_2 OFF
$V_i < -V_{R2}$	$-V_{R2}$	D_1 OFF, D_2 ON



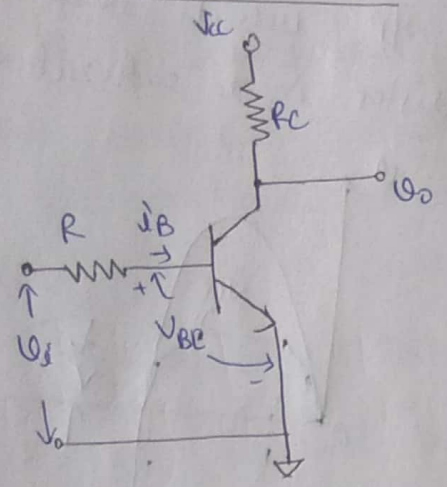


Clipping region → ~~D_1 off D_2 off~~ → D_1 ON D_2 off → Clipping region

D_1 OFF
D_2 ON



* Transistor as clipper:



The nonlinearities of transistor is used for clipping purposes.

→ It occur when transistor crosses from cut-off into active region.

→ Again it occur, when crosses from active region to saturation region.

So, clipping operation will be performed at boundary during transition.

→ The portion of the i/p of waveform, which keeps transistor in active region, will appear without distortion. So, input current is required rather than voltage. The resistance R should be large in compare to the I/p resistance of transistor, to keep it in active region.

→ The I/p base current is given as,

$i_B(t) \propto \{ v_i(t) - V_\gamma \}$, where V_γ → base to emitter cut in Vge.

→ **Cut in Region:**

The transistor come out of cut-off region around 0.1 V reverse bias at Ge or 0V for silicon. The emitter current is zero. So, collector current becomes equal to I_{CBO}, which flow into base lead.

The collector current starts to increase after forward bias the transistor. The change in collector current by 10μA brings the transition into active region.

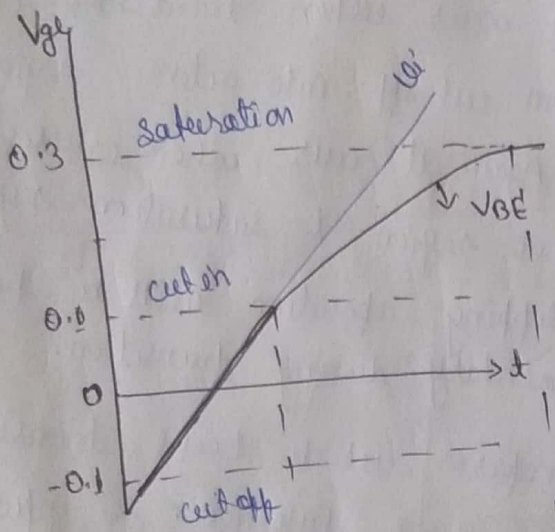
→ **Input resistance:**

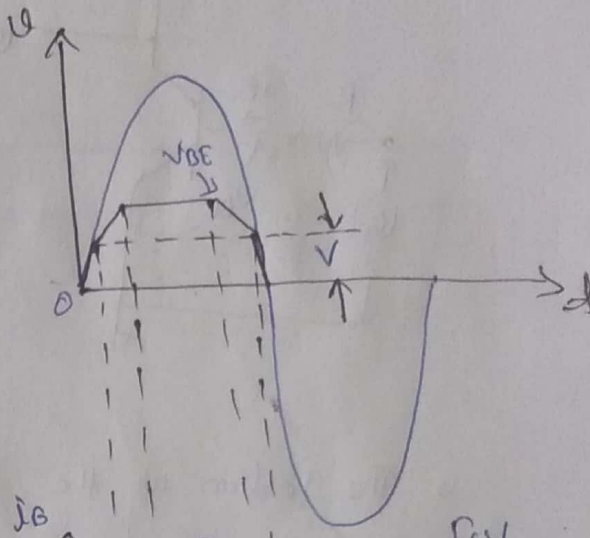
The incremental resistance b/w base and emitter is important.

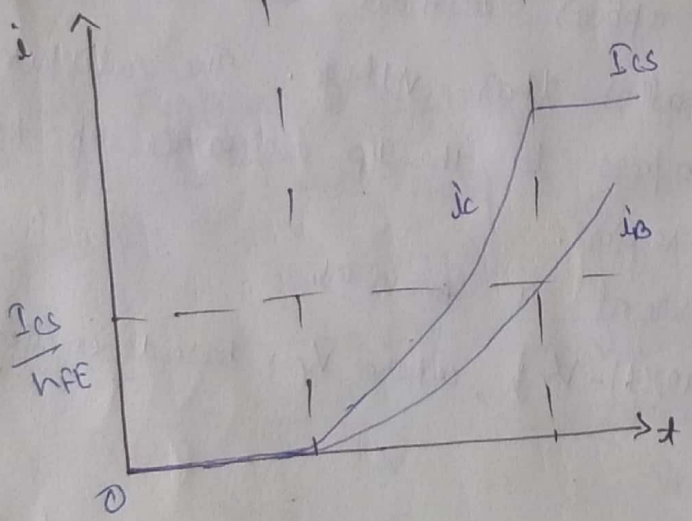
$$h_{ie} = r_{bb'} + r_{b'e} \approx r_{bb'} + \frac{h_{fe}}{g_m}$$

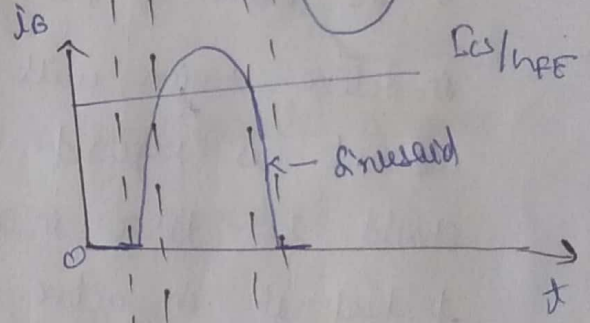
Waveforms:

→ When ramp signal is given as i/p, which starts at V_{BE} below cut-off and carries transister in to saturation.

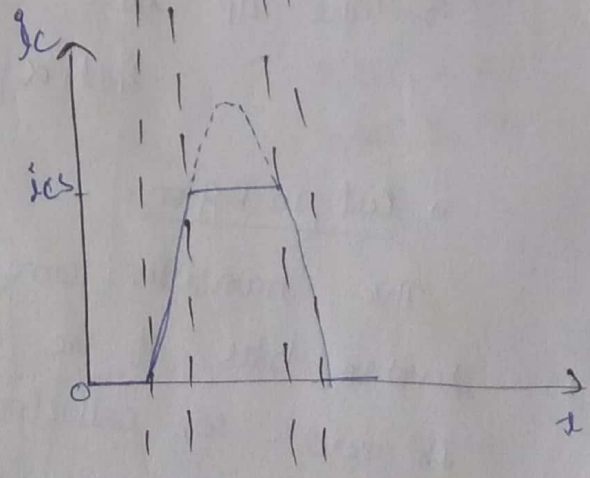


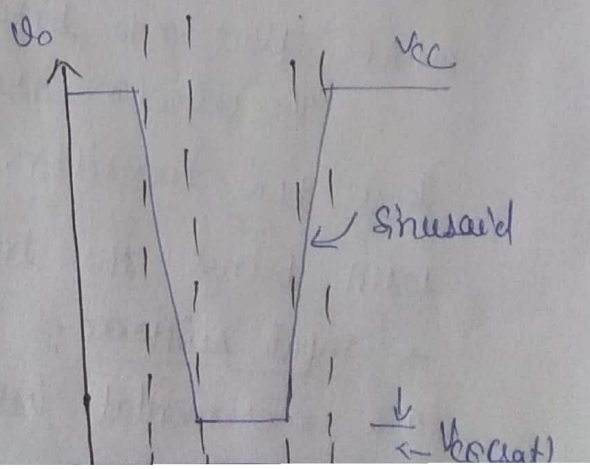






→ When sinusoidal signal is given as i/p. The base circuit is biased so, that cut-in occurs when V_{BE} reaches to the voltage V.





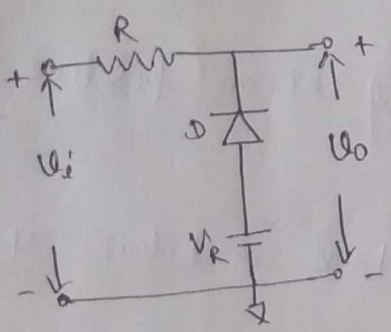
* Comparators :

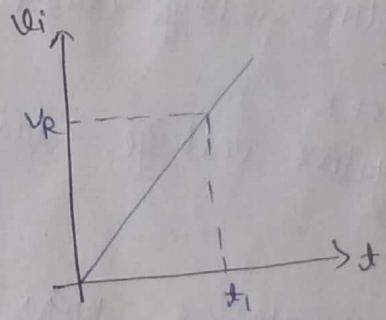
It is circuit, which may be used to mark the instant when waveform attains some reference level.

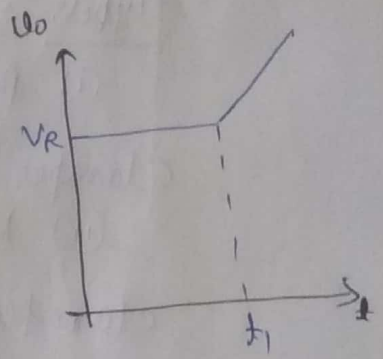
The non-linear circuits which perform clipping may be used to perform comparison.

→ In comparators there is no interest to reproduce a part of signal without distortion. Its o/p may be sharp pulse when signal and reference are equal.

→ Comparators may be non-regenerative or regenerative but clipping ckts fall in to category of non-regenerative comparators.







When $V_i < V_R$, diode is ON and o/p is equal to V_R.
When $V_i > V_R$, diode is OFF and o/p follows i/p.
The breaks occur at $V_i = V_R$ at time $t = t_1$.

→ In regenerative comparators, positive fb is used to obtain unity loop gain. eg. schmitt trigger & blocking oscillator
↓ generates step ↓ generates pulse.

→ Applications of voltage comparators :

(i) In accurate time measurement
(ii) In pulse time modulation
(iii) As timing markers generated from sine wave
(iv) In phase meters
(v) In amplitude distribution analyzer
(vi) To obtain square wave from a sine wave
(vii) In analog to digital converters.

* clamping operation:

Clamping ckts are used to clamp or fix to some constant reference level V_R. It may be one way or two way clamp.

The clamping ckt may be used to introduce d.c. component. During transmission dc component is stopped by capacitive n/w. So, it is called as dc restorer or dc reinserter.

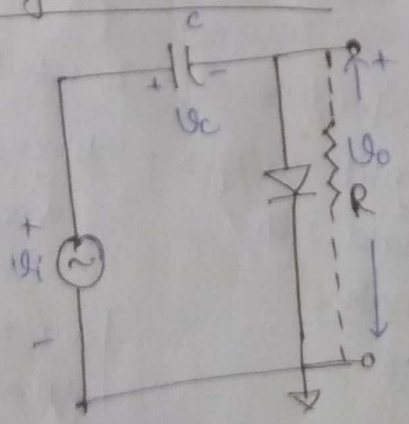
Types:

(i) Positive - voltage clamping ckt or negative peak clamper ckt.

(ii) Negative voltage clamping ckt or positive peak clamper.

→ The entire waveform appear above or below the reference voltage.

→ Negative clamper:



An ideal diode is considered in which $R_f = 0$ or $V_\gamma = 0$ V.

The capacitor 'C' is uncharged at $t = 0$.

→ For the 1st quarter cycle i/p signal rises from zero to max^m value V_m. During this time diode is ON and capacitor is charged to max^m value.

i.e. $V_c = V_m$.

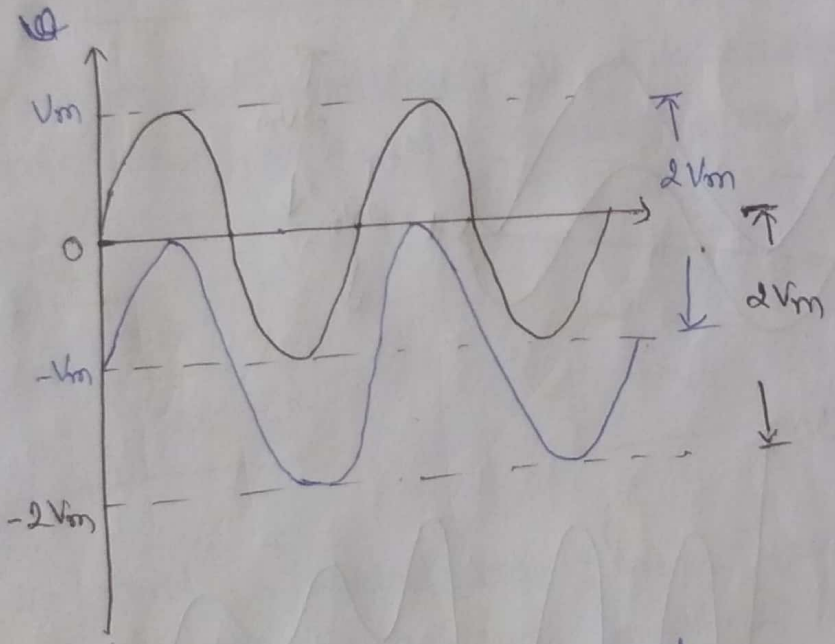
→ After 1st quarter cycle, I/P signal starts to fall, so, voltage V_c is not able to follow the I/P. Since there is no path to discharge. The ~~v~~ge across capacitor remains at $V_c = V_m$. It act as voltage source. The o/p is given as, $V_o = V_i - V_m$.

→ During succeeding cycles, the signal will be clamped to zero.

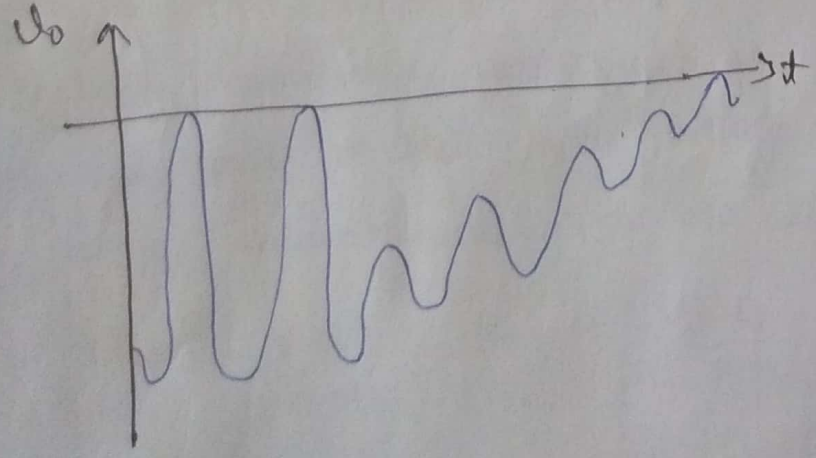
ie. $V_i = 0$, $V_o = -V_m$

$V_c = V_m$, $V_o = 0$

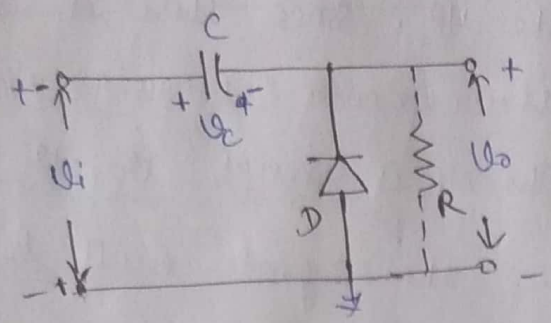
& $V_i = -V_m$, $V_o = -2V_m$.



→ When steady state will be achieved then again capacitor has to discharge. For the resistance R should be connected either shunt with capacitor or diode.



→ Positive clamper:

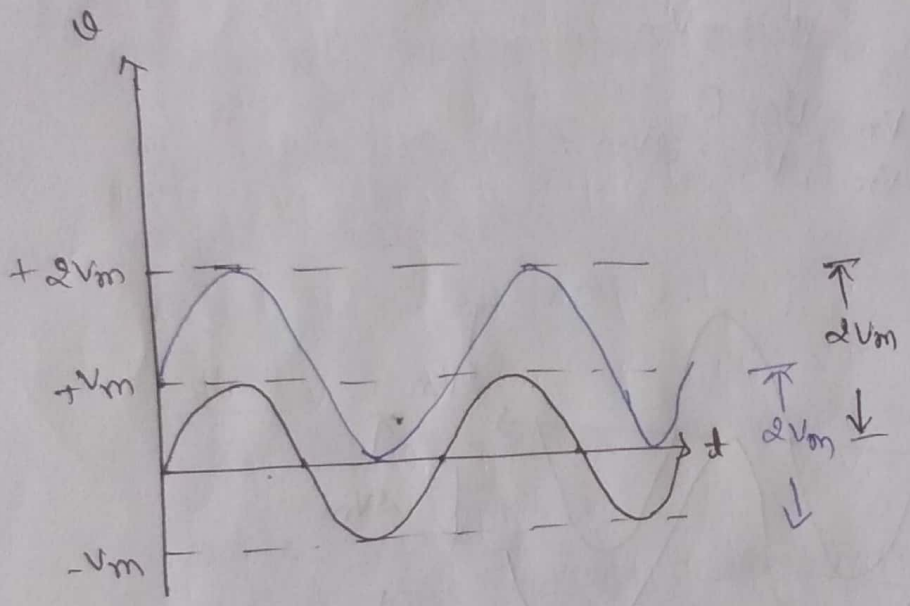


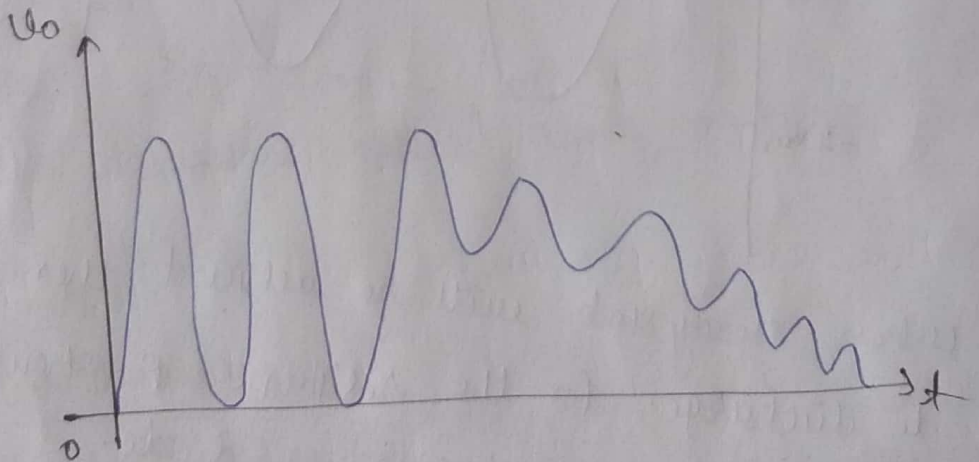
$v_o = v_i - (-V_m) = v_i + V_m$

when $v_i = 0$, $v_o = V_m$

$v_i = V_m$, $v_o = 2V_m$

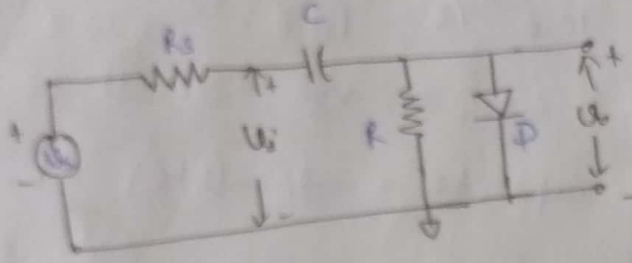
$v_i = -V_m$, $v_o = 0$



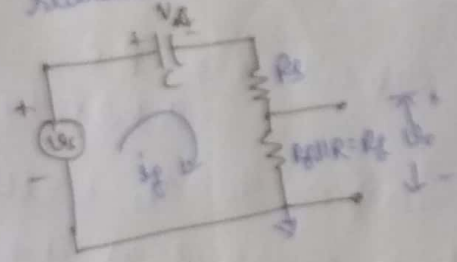


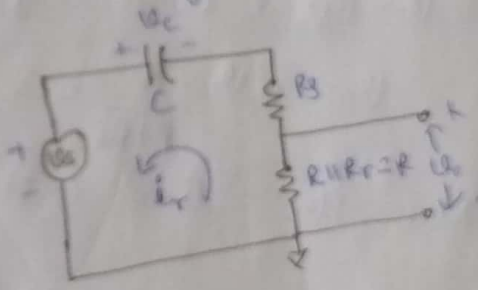
* Clamping circuit taking source and diode resistance into account.

Here source resistance R_s and diode resistance are considered. R_f lie in the range of 10 to 100 Ω. R_s may be negligible or considered as 1 kΩ, it depend up on source. Here $V_\gamma = 0$.



→ when diode is conducting then its resistance is considered as R_f and when it is not conducting then as R_r. So, circuit is redrawn as;





when i/p signal is applied then after few cycles, the steady state condition is achieved. In which positive peak has clamped to zero.

e.g. $R_s = R_f = 50\,\Omega$, $R = 20\,k\Omega$ & $C = 2\,\mu F$. A symmetrical square signal of amplitude 20V and freq. 5 kHz is applied at $t = 0$.

→ Initially capacitor is uncharged. At $t = 0$, i/p jumps to +20V and diode conducts. The voltage across capacitor can't change instantaneously. So O/P will be given as,

$$20 \times \frac{50}{50+50} = 10\,V \quad \left(\frac{V_{in} \cdot R_f}{R_s + R_f}\right).$$

The period of I/P signal, $T = \frac{1}{5\,kHz} = 200\,\mu sec$.

The time constant of the capacitor, $\tau = (R_s + R_f)C = (50+50)\times 2\times 10^{-6}$
$= 200\,\mu sec$.

The capacitor 'C' will charge in the interval $0 < t < T/2$.

So, O/P at $t = T/2 = 100\,\mu sec$ is given as,

$$V_o = 10e^{-T_2/\tau} = 10e^{-100/200} = 10e^{-0.5} = \underline{6V}.$$

i.e. Vgs across R_f is 6V, so, Vgs across R_s is also 6V.

Hence Vgs across capacitor $= 20 - (6+6) = \underline{8V}$.

At $t = T/2$ I/P drops to zero. The diode is off.

i.e. $V_c = 8V$ & $V_s = 0$. So, O/P Vgs is given as,

$$V_o = -V_c \cdot \frac{R}{R+R_s} = -V_c = \underline{-8V}.$$

Now the time constant of capacitor is $\tau = R.C$
$= 20\,k\Omega \times 2\,\mu F = 40\,msec$

which is much larger in compare to $T/2 = 100\,\mu sec$.

So, decay is negligible. So, it is considered as straight line.

At $t = T$, the voltage across capacitor is still 8V.

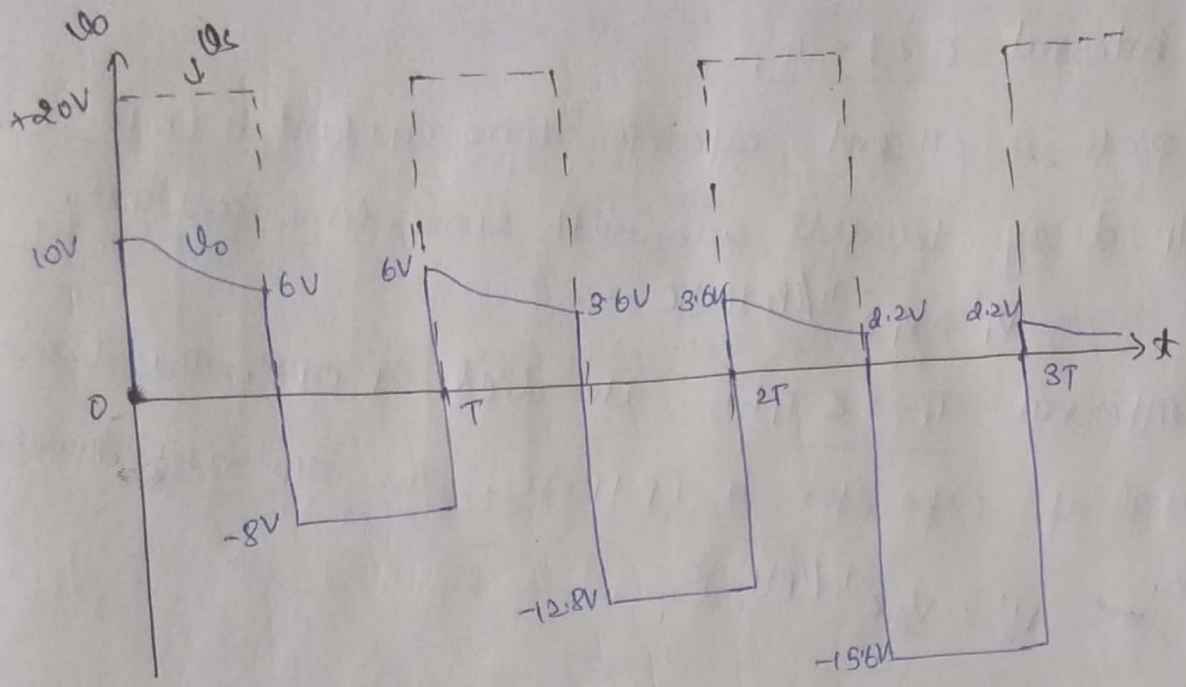
So, O/P returns to $\underline{+6V}$.

$$\text{O/P Vgs} = (V_{in} - V_c)\times \frac{R_f}{R_f+R_s} = (20-8)\frac{\times 50}{50+50} = +6V.$$

Again for interval $T < t < 3T/2$, O/P decay towards zero.

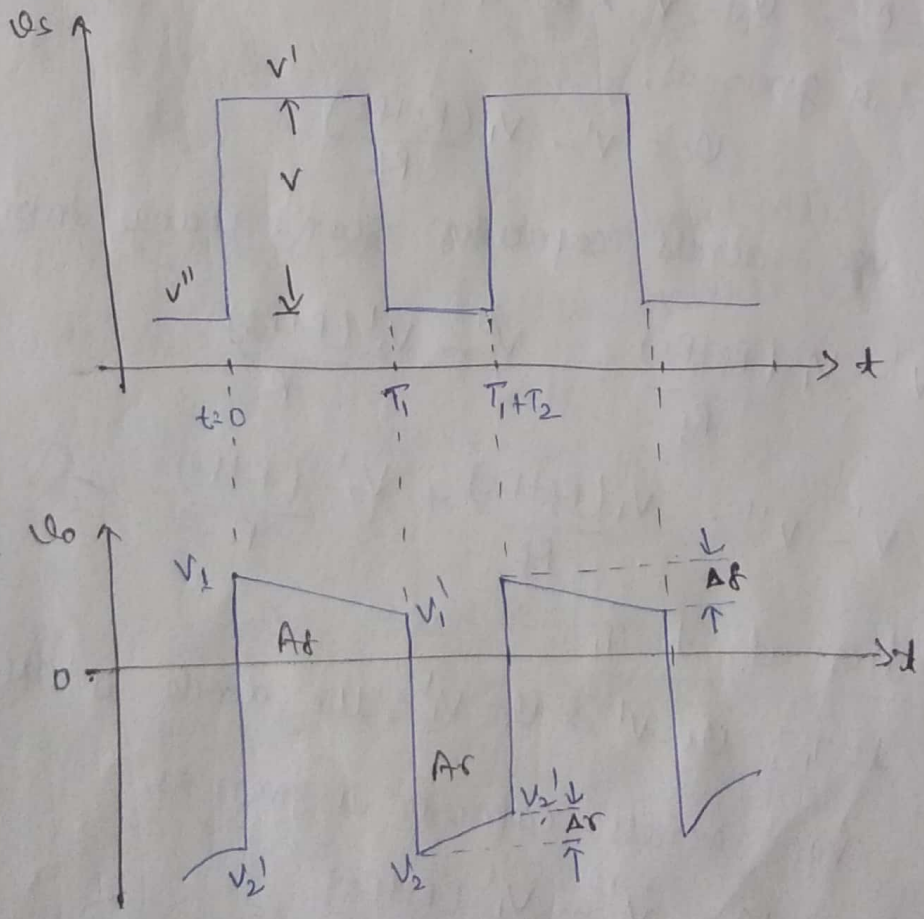
So, O/P at $t = 3T/2$, $V_o = 6\cdot e^{-1/2} = \underline{3.6V}$

Same process will be repeated.



→ steady state o/p waveform for a square wave input

Consider the square wave as i/p to the clamping ckt. and o/p waveform will appear as:



In interval $0 < t < T_1$,

Diode is ON, and capacitor time constant is $(R_f + R_s)C$. The o/p decay towards zero with same time constant.

$$V_1' = V_1 e^{-T_1/(R_f+R_s)C}$$

In interval $T_1 < t < T_1 + T_2$, the diode is OFF. The time constant of capacitor is $(R+R_s)C$. The o/p rises towards zero.

$$V_2' = V_2 e^{-T_2/(R+R_s)C}$$

Condition at $t=0$

At $t = 0^-$, $v_s = V'$ & $v_o = V_2'$, diode is OFF.

The vge across capacitor is given as,

$$v_c = V'' - V_2' \frac{(R+R_s)}{R}$$

At $t = 0^+$ $v_s = V'$ & $v_o = V_1$, diode is ON. The vge across capacitor is given as,

$$v_c = V' - V_1 \frac{(R_f+R_s)}{R_f}$$

The vge across capacitor can't change immediately,

so, $$V' - V_1 \frac{(R_f+R_s)}{R_f} = V'' - V_2' \frac{(R+R_s)}{R}$$

$$\Rightarrow V' - V'' = V_1 \frac{(R_f+R_s)}{R_f} - V_2' \frac{(R+R_s)}{R} \quad -(1)$$

Condition at $t = T_1$

At $t = T_1^-$, $v_s = V'$ & $v_o = V_1'$, the diode is ON.

The vge across capacitor is given as,

$$v_c = V' - V_1' \frac{(R_s+R_f)}{R_f}$$

at $t = T_1'$, $v_s = V''$ & $v_o = V_2$, the diode is off. So, v_{ss} across capacitor is given as,

$$v_c = V'' - \frac{V_2(R+R_s)}{R}$$

The voltage across capacitor will not change immediately,

So,

$$V' - V_1' \frac{(R_f+R_s)}{R_f} = V'' - \frac{V_2(R+R_s)}{R}$$

$$\Rightarrow V' - V'' = V_1' \frac{(R_f+R_s)}{R_f} - \frac{V_2(R+R_s)}{R} \quad (2)$$

If $R_s = 0$, the jumps in i/p & o/p voltage would be equal.

ie $V_1 - V_2' = V_1' - V_2 = V$.

By subtracting eqn (2) from eqn (1), we get,

$$\frac{R_f+R_s}{R_f}(V_1 - V_1') - \frac{R+R_s}{R}(V_2' - V_2) = 0$$

where, $V_1 - V_1' = \Delta_f \rightarrow$ tilt in the forward dirn

$V_2' - V_2 = \Delta_r \rightarrow$ tilt in the reverse dirn.

$$\therefore \Delta_f = \frac{R_f}{R_f+R_s} \times \frac{R+R_s}{R} \cdot \Delta_r$$

Since R_s is smaller than R, so tilt Δ_f is always less than Δ_r. When $R_s \ll R_f$ then $\Delta_f \approx \Delta_r$.

* Clamping circuit theorem:

In the steady state, the ratio of area under the o/p vge curve in forward dirn to that in the reverse dirn is equal to R_f/R.

i.e. $$\frac{A_f}{A_r} = \frac{R_f}{R}.$$

If $v_f(t)$ is the o/p waveform in the forward direction, then capacitor charging current is equal to $i_f(t) = v_f(t)/R_f$.

So, charge acquired by capacitor is given as,

$$\int_0^T i_f(t)\,dt = \frac{1}{R_f}\int_0^T v_f(t)\,dt = A_f/R_f \quad -(1)$$

Similarly, if $v_r(t)$ is o/p vge in reverse dirn, then current which discharges the capacitor is, $i_r(t) = v_r(t)/R$.

So, total charge lost $= \int_{T_1}^{T_1+T_2} i_r(t)\,dt = \frac{1}{R}\int_{T_1}^{T_1+T_2} v_r(t)\,dt = A_r/R$. $-(2)$

In steady state, we can equate eqn (1) & (2),

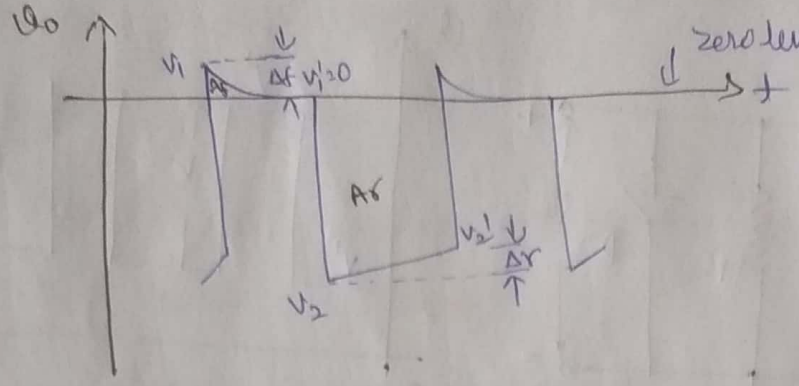
So, $$\boxed{\frac{A_f}{A_r} = R_f/R}$$

* Practical clamping circuits:

Perfect flatness of the +ve & -ve peaks of square wave can be obtained only if C is very large. In clamping ckt we have, $(R_f+R)C << T_1$ and $(R+R_s)C >> T_2$. The capacitor discharge slowly, so tilt in the o/p will be small.

During charging, capacitor charge soon, so there is

Spikes of small magnitude. So, Δf is much smaller than Δr.



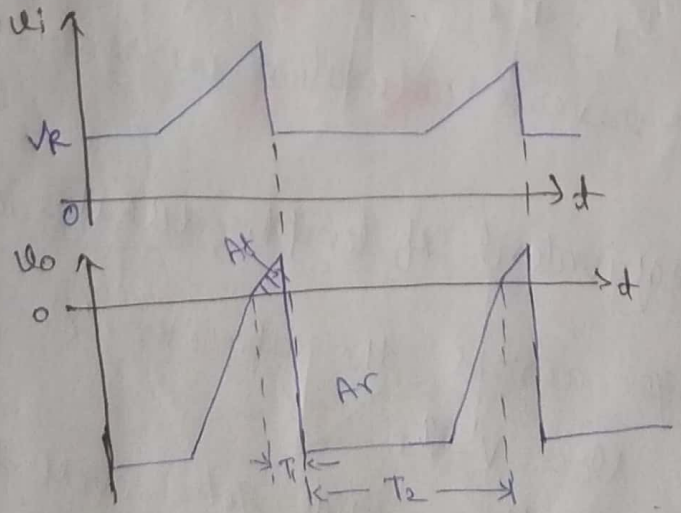
Here $V_1' = 0$, So, $V_2 = -V \cdot \frac{R}{R+R_s}$

$$V_2' = V_2 e^{-T_2/(R+R_s)C}, \quad \Delta r = V_2' - V_2$$

$$\Delta f = V_1 - V_1' = V_1 = \frac{R_f}{R_f+R_s} \times \frac{R+R_s}{R} \times \Delta r.$$

The o/p appear as multiple of $\frac{R_f}{R_f+R_s}$ or $\frac{R}{R+R_s}$. But $\frac{R}{R+R_s}$ is much closer to unity.

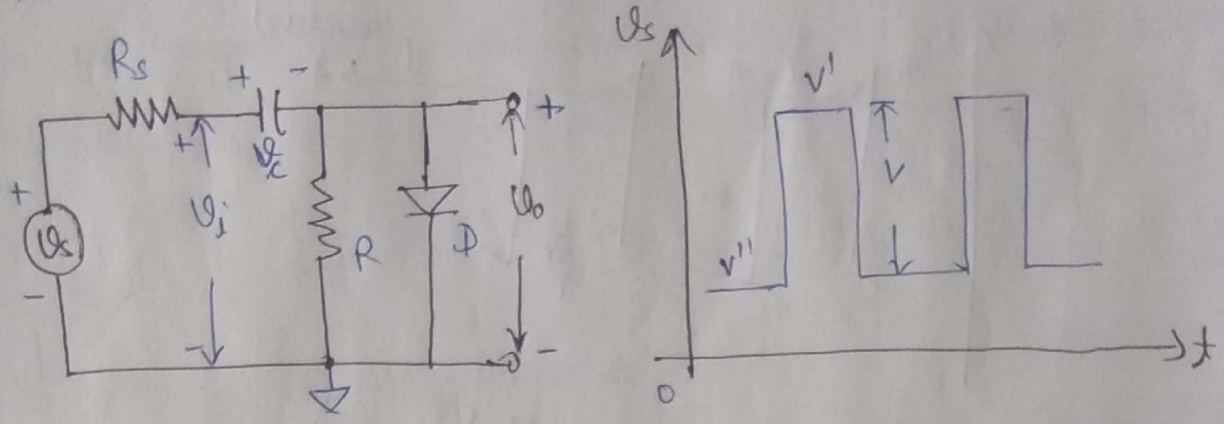
The distortion can be observed more clearly in case ramp signal as i/p.



→ When reference voltage V_R is connected in series with diode then it clamp the signal accordingly. If V_γ is not negligible then, clamping cct theorem is given as

$$\frac{A_f - (V_R + V_\gamma)T_1}{A_r} = R_f/R.$$

* Effect of diode characteristics on clamping voltage:



The practical diode is considered. The i/p square wave has peak to peak amplitude as V. The capacitor 'C' is considered as large, so that o/p waveform across the diode is same as similar to square wave. The Rs is considered as zero.

During the interval when i/p signal is high at V', the diode clamps the o/p at some clamping vge V_{d1}. So, corresponding current eqn is given as,

$$I_{D1} = I_0 e^{V_{d1}/\eta V_T}$$

where I_0 → reverse saturation current; $\eta = 1$ for Ge & $\eta = 2$ for Si

V_T → volt equivalent of temp., which is taken as 26mV.

The voltage across the capacitor 'C' is given as,

$$V_C = V' - V_{d1}$$

when i/p drops, then diode gets reversed bias and capacitor discharge through 'R'.

The vge across 'R' is given as,

$$V_R = V_C - V'' = V' - V'' - V_{d1} = V - V_{d1} \quad [\because V' - V'' = V]$$

Generally $V_{c1} << V$, so $V - V_{c1} \simeq V$.

So, Vge across capacit resistan 'R' is V. Hence discharge current of capacitor = V/R.

Since i/p is symmetrical Square wave, so, net accumulation of charge is zero.

Hence charging current = discharging current

$$\text{i.e. } I_{C1} = \frac{V}{R} = I_0 e^{V_{c1}/\eta V_T}.$$

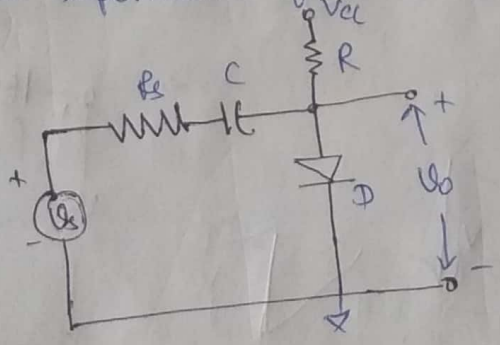
$$\Rightarrow \frac{V}{I_0 R} = e^{V_{c1}/\eta V_T} \Rightarrow V_{c1} = \eta V_T \ln \frac{V}{I_0 R}$$

After taking differential, we get

$$dV_{c1} = \eta V_T \frac{dV}{I_0 R}$$

It shows how clamping voltage varies with amplitude of an i/p signal.

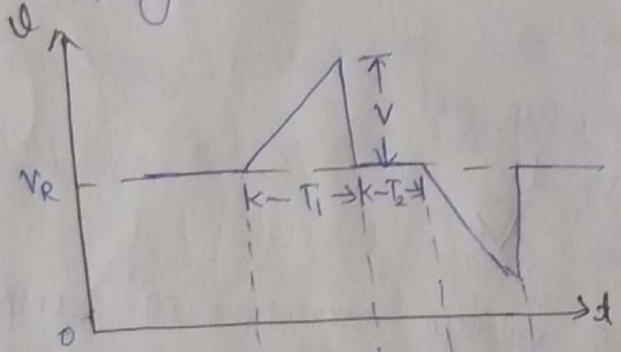
The clamping ckt is modified to improve stability, and to reduce dependence of V_{c1} on V.



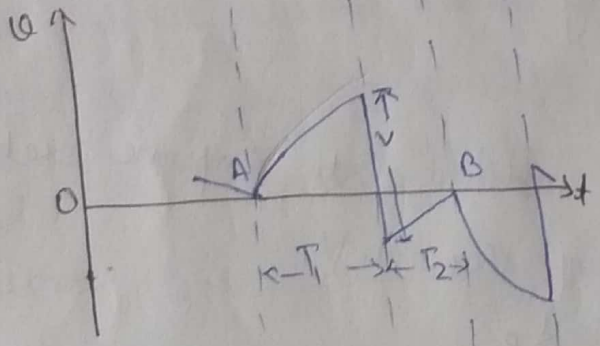
The diode current equation in presence of square wave o/p is given as, $I_{C1} = \frac{2V_{cc} + V}{R}$.

* Synchronized clamping:

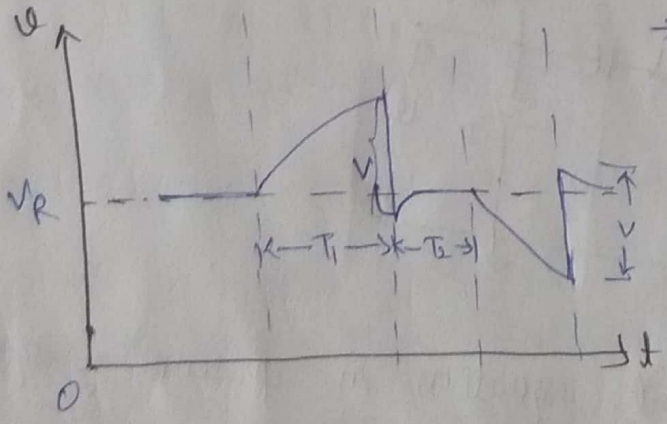
The dc restorers are examples of clamping circuit, in which time of clamping is controlled by signal itself. But when time of clamping is not determined by signal itself. Now it is done by using auxiliary voltage, which is called as control signal. This signal is synchronous with the signal. Such type of clamping is known as Synchronized clamping.



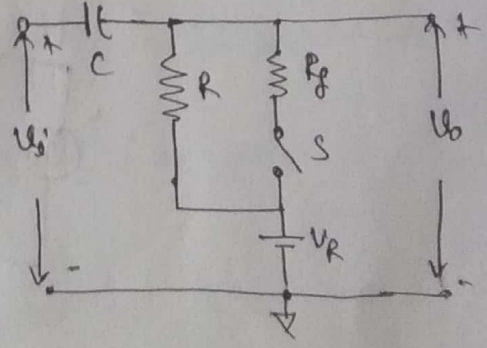
- SI is used to displace the beam of cathode ray tube.



→ Signal is transmitted through a.c. coupling n/w, whose has low freq. time constant is smaller than T_1. Displacement occurs at 'A' & 'B'. The d.c. level V_R has been lost.

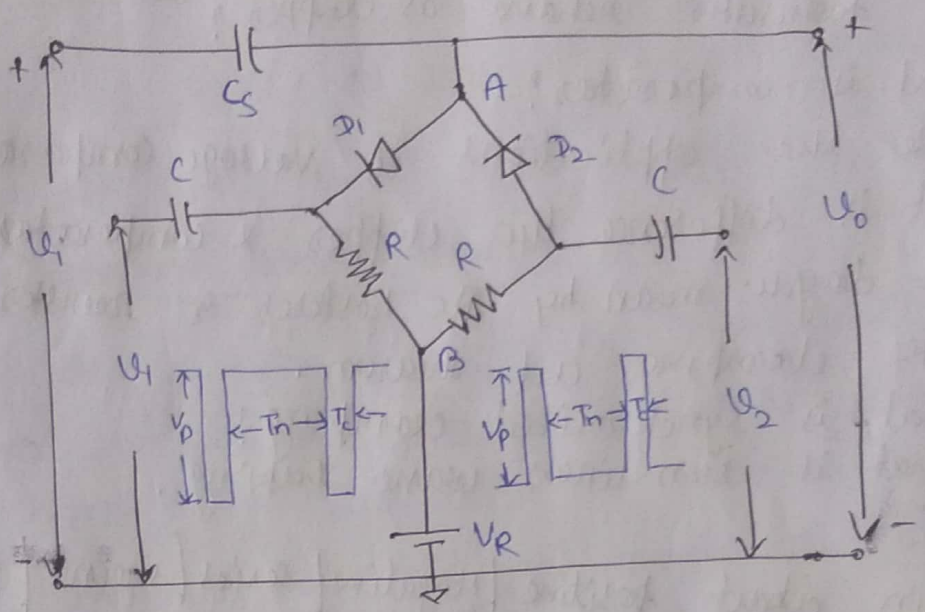


→



Switch is closed during T_2 and open during T_1. The pips which appear when voltage return to V_R, may appear as narrow spikes as R_f approaches zero.

It is not possible to use synchronized clamping with the signal of arbitrary waveform.



It is synchronous clamping ckt, in which signal is transmitted from i/p to o/p through C_s. Two diodes function as switch. Two control signal pulse $V_1(t)$ & $V_2(t)$ is required, which are identical but inverse of each other.

During time interval T_c diodes will conduct and voltage at A is same as B. During T_n both diodes are reverse biased and o/p is free to follow i/p.

Suppose at the end of T_n, Vge A is not equal to V_R. Then If $V_A > V_R$ then $V_A > V_R$ D_1 will conduct & discharging C_s in to C— until $V_A = V_R$.

If $V_A < V_R$, diode D_2 will conduct until $V_A = V_R$. For proper operation of ckt, $C >> C_s$ & $RC >> T_c$. It is also required that $C_s(R_f + R_s) << T_c$.