Riscduino-Dcore (ChipIgnite -2206Q)

Based on Chip Signature inside the design, this tape-out is corresponds to 07th Sept 2022 and this tape-out is similar to MPW-6 tape-out core : [Link](https://foss-eda-tools.googlesource.com/third_party/shuttle/sky130/mpw-006/slot-004)

Chip Received on 21st June 2023

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| --- | --- | --- |
| Test Name | Test Start/End Date | Remark |
| BTest0: Basic Risc-0/1 Boot with “Hello world message” at UART-0  Test Setup with : Caravel HAT + Inter connect Board + FPGA | 21st June 2023 to 28th June 2023 | Riscv boot not working with cache enabled, need to check any issue in SRAM memory. Cache access not working for both invert/non-invert SRAM write option.  In Non cache mode, test passed for both Riscv core at 10Mhz |
| BTest1: Configure the FPGA user memory through UART Master, If possible burn user flash though Arudino |  |  |

Test Date: 21st June to 28th June 2023

Bring-up Board Setup:

1. Caravel HAT

2. FPGA Interconnect board

3. numato Spartan-6 : [Link](https://numato.com/product/mimas-spartan-6-fpga-development-board/)

Test Sequence: Basic Riscv core Boot up and Riscv core write repeatably “hello world” into UART-0

Step-1: Since User SPI flash is not yet programmed or plug-in. We are programming user Flash data in FPGA.

1. User C code is available at : [link](https://github.com/dineshannayya/mpw_bringup/tree/main/2206Q/fpga/hello_world/hex)
2. Compile the code ( make ) and generate user\_uart.mem file
3. copy the uart.mem in to fpga rtl top file : [link](https://github.com/dineshannayya/mpw_bringup/blob/main/2206Q/fpga/hello_world/rtl/top/top.v)
4. Compile the FPGA core using project file : [link](https://github.com/dineshannayya/mpw_bringup/blob/main/2206Q/fpga/hello_world/hello_world.xise) and generate top.bin file
5. program the top.bin to fpga using numato executable : [link](https://productdata.numato.com/assets/downloads/fpga/mimas/mimasConfig.exe)

Step-2: Using the Caravel HAT to caravel flash memory,

A. Run setup : [Link](https://github.com/dineshannayya/mpw_bringup/tree/main/2206Q/tests/hello_world)

command: make clean flash

Step-3: Connect the logic analyzer at [IO-7] check the hello world

Note: During the debug process, I have monitor the User SPI Interface signal and 128 bit Debug bus

