CI2306 Silicon Status:

**Silicon Bug Report:**

1. Caravel Flashing issue: -

**Symptom:** Unable to program the caravel flash through their SPI interface.

**Root Cause:** During the tape-out process the default GPIO defaults did not get programmed.  It will power up with all GPIOs completely disabled.

**Workaround: We need pre-programed Caravel flash with GPIO[4:1] is configured as**

reg\_mprj\_io\_1 = GPIO\_MODE\_MGMT\_STD\_OUTPUT;

reg\_mprj\_io\_2 = GPIO\_MODE\_MGMT\_STD\_INPUT\_NOPULL;

reg\_mprj\_io\_3 = GPIO\_MODE\_MGMT\_STD\_INPUT\_NOPULL;

reg\_mprj\_io\_4 = GPIO\_MODE\_MGMT\_STD\_INPUT\_NOPULL;

Bug Analysis from Efabless Team : [Programming Flash Workaround for 2306 - Google Docs](https://docs.google.com/document/d/1HqE044Y88vLqtzXa0LtFz_QWH7eRt_70xq8t8jrvgq0/edit)

**Difference Between CI2206Q vs CI2306Q SOC**

**CI2206Q uses Sept 7 2022 (Rev 5.4), where as CI2306Q uses 14th June 2023 (Rev 6.11)** [**Riscduino Dcore**](https://github.com/dineshannayya/riscduino_dcore) **database. CI2306Q tapeout is done with better full timing closure, transition fixes and includes additional IP like AES,FPU,RTC**

|  |  |  |  |
| --- | --- | --- | --- |
|  | CI2206Q | CI2306Q | Remarks |
| Riscv Core | Dual core | Dual Core |  |
| QSPI | Available | Available |  |
| SSPI | Available | Available |  |
| Dual UART | Available | Available |  |
| I2C Master | Available | Available |  |
| ws281x | Four | Four |  |
| PWM | 6 | 3 | To add more IP, reduced the no of PWM in CI2306Q |
| USB Host | Available | Available |  |
| AES 128 bit | None | Available |  |
| SP FPU | None | Available |  |
| RTC | None | Available |  |
| Random Generator | None | Available |  |
| NEC IR Tx/Rx | None | Available | Infra Red transmitter and Receiver |
| Basic Stepper Motor | None | Available |  |

**Riscduino Health:**

1. In Previous CI2206Q chip, most of the chip were working around 1.6V, where as CI2306 shows device working in 1.6V to 2.0V.
2. In Previous CI2206Q chip, one in 10 chip showing working internal SRAM; in CI shows 7 in 10 showing working dache SRAM, 3 in 10 Showing working icache/dcache SRAM.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 2306Q Silicon Tracking Sheet | | | | | |
| Chip No | riscv ctrl | icache | dcache | Core voltage working range | Status |
| 1 | 0x04020000 | disabled | enabled | 1.6v – 2V |  |
| 2 |  |  |  |  | Caravel Boot fails |
| 3 | 0x04020000 | disabled | enabled | 1.6v – 2V |  |
| 3 | 0x00030000 | enabled | enabled | 1.6v – 2V |  |
| 4 | 0x04020000 | disabled | enabled | 1.6v – 2V |  |
| 5 | 0x04020000 | disabled | enabled | 1.6v – 2V |  |
| 6 | 0x04020000 | disabled | enabled | 1.6v – 2V |  |
| 6 | 0x00020000 | enabled | enabled | 1.7v – 1.9V |  |
| 7 | 0x00020000 | enabled | enabled | 1.7v – 1.9V |  |
| 8 | cvvcvvddaa | enabled | enabled | 1.7v – 1.9V |  |
| 9 | 0x0C000000 | disabled | disabled | 1.6v – 2V |  |
| 10 | 0x0C000000 | disabled | disabled | 1.6v – 2V |  |