1. **The state diagram of your FSM.**

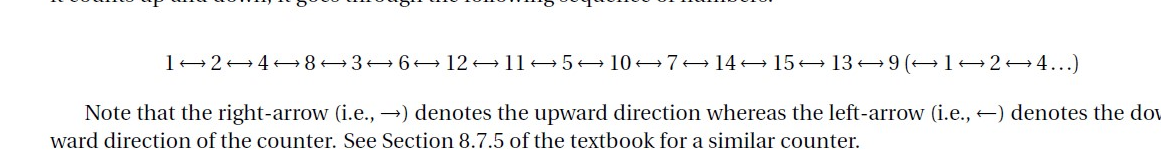


Figure 1: State Machine Possible States

The tests shown in the lab instructions are by figure 1. The each number can be represented by a letter which will be in alphabetical order, by convention. Thus, variable A represents 1, B represents 2 and so for.

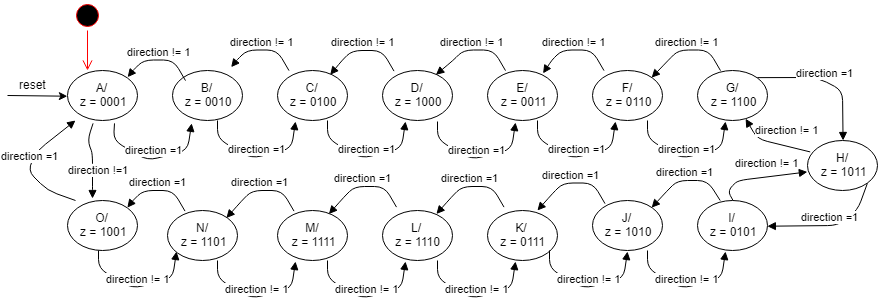


Figure 2: State Diagram

For our state diagram, A is the corresponding state from the instructions. Z is the binary representation of the value in that state. If the direction is 1, the state diagram will change to the next state. Consequently, if it is not 1, it will go to the previous state. For instance, if the current state is A, the next state is B if direction = 1 or it will be O if direction != 1. Also, the starting state (initiation) our state machine is at state A so as the reset.

1. **A description of the FSM circuit.**

The FSM circuit can be broken down into 3 parts.

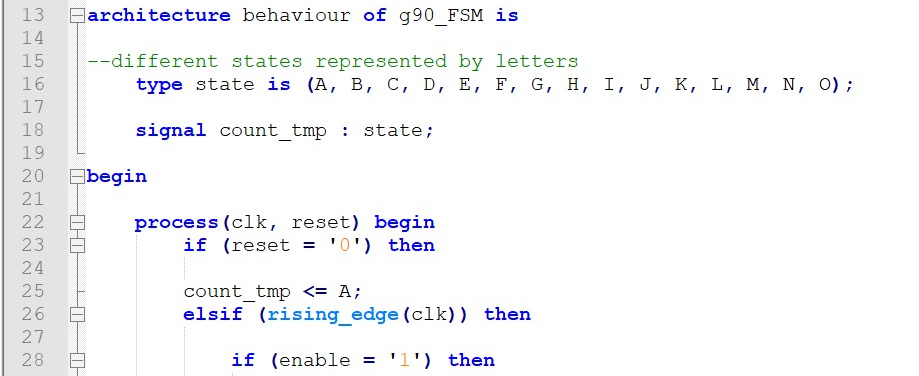


Figure 3: Part 1 of State Machine - Initialization of count and variables

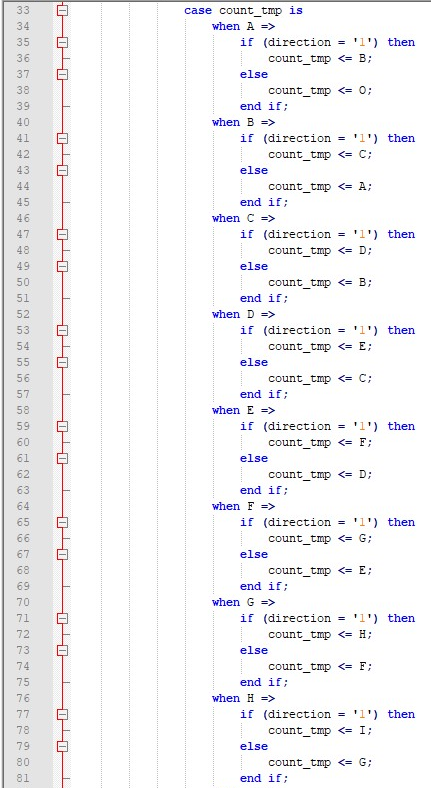
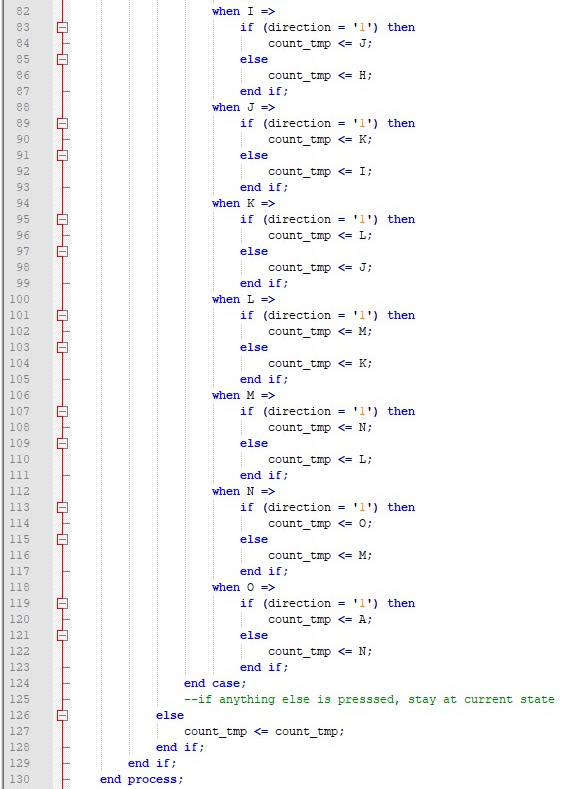


Figure 4.2: From State I to State O and other cases

Figure 4.1: From State A to State H

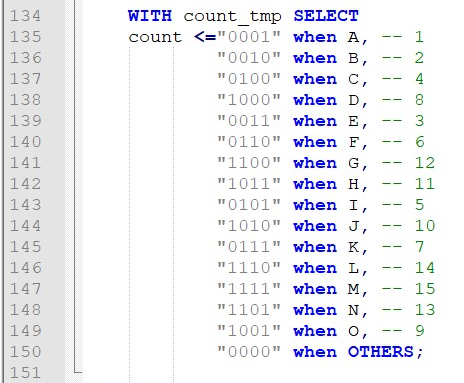


Figure 5: Conversion of States to Binary

1. **A discussion of how the FSM circuit was tested, showing representative simulation plots. How do you know that these circuits work correctly?**
2. **A description of the multi-mode counter circuit.**
3. **A discussion of how the multi-mode counter circuit was tested on the FPGA board.**
4. **A summary of the FPGA resource utilization (from the Compilation Report’s Flow Summary) and the RTL schematic diagram for the multi-mode counter circuit. Clearly specify which part of your code maps to which part of the schematic diagram**