CS 613200 Advanced Logic Synthesis
Final Project (2023, Spring)

111062684 林鼎勳

1. Design Flow

There are four stages of my design flow. In the first stage, I take the .kiss file as input and construct the state transition graph. In the second stage, I calculate the state probability and the weight of the connected edges and convert the graph into an undirected graph. In the third stage, I implement the algorithm in this paper: State assignment for Low Power Dissipation[1] and modify the constraints of the MLP problem. Then, we output the .blif file. In the last stage, I use SIS to evaluate my result.

2. Cost Function

The cost function of the edge between connected states is the same as in the paper mentioned above. If the state variable i, j between an edge is different, the weight of the edge will time 2.

3. Modified MLP Problem

As mentioned above, I modify the MLP problem. At each time of state variable assignment, I want to split each group at least one time. This will help to reduce the generation of useless state variables. Another constraint I add is in each round of state variable assignment, the number of 0s must be more than the number of 1s. The result of the synthesis tool shows that the power consumption is reduced.

4. Experimental Results

I use the command `state_assign` provided by SIS to produce the baselines and use them to compare with my results. Also, I try two kinds of state assignments: one is set as the number of 0s more than the number of 1s, and the other is set as the number of 0s less than the number of 1s.

Benchmark	# States	State Code Len.	SIS	# 0s ≥ # 1s	Diff. %	# 0s ≤ # 1s	Diff. %
bbara	7	3	388.2	427.5	10.12%	439.8	13.29%
bbsse	13	4	1092.9	1101.4	0.78%	1101.4	0.78%
bbtas	6	3	224.0	217.1	-3.08%	266.8	19.11%
beecount	4	2	303.5	329.9	8.70%	329.9	8.70%
cse	16	4	1973.8	2152.8	9.07%	2152.8	9.07%
dk14	7	3	1023.2	1223.8	19.61%	1223.8	19.61%
dk16	27	5	2433.0	2706.0	11.22%	2852.8	17.25%
ex1	18	5	2536.0	2491.5	-1.75%	2523.6	-0.49%
s27	5	3	292.1	377.1	29.10%	333.8	14.28%
snad	32	5	6867.9	6399.8	-6.82%	6538.2	-4.80%

From the results, we know that only one benchmark: s27, whose power consumption is less if the number of 0s is less than the number of 1s. Compared to the SIS baseline, three benchmarks have better results, while four benchmarks have more than 10% differences.

As for the length of the state code, it shows that the length is minimized. It is because the effect of the state code length is much more than the switching activity. Noted that the length of each state code produced by SIS is the same as my result.

[1] L. Benini and G. De Micheli, "State assignment for low power dissipation," in IEEE Journal of Solid-State Circuits, vol. 30, no. 3, pp. 258-268, March 1995.