CS6135 VLSI PDA HW3

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0) **My work in some testcases cannot meet the area constraint.** The bottleneck I encountered was in the SA part. I tried my best to find and adjust the parameter but still couldn't complete the work in 10 minutes and had constraint-violated results.

1) How to compile and execute your program, and give an execution example:

- Compile: Go into the directory "HW3/src/" and enter the command:

  ```
  $ make
  ```

  This will generate the executable file "hw3" in the directory "HW3/bin/".
- Execute: In the same directory ("HW3/src/") and enter the command:

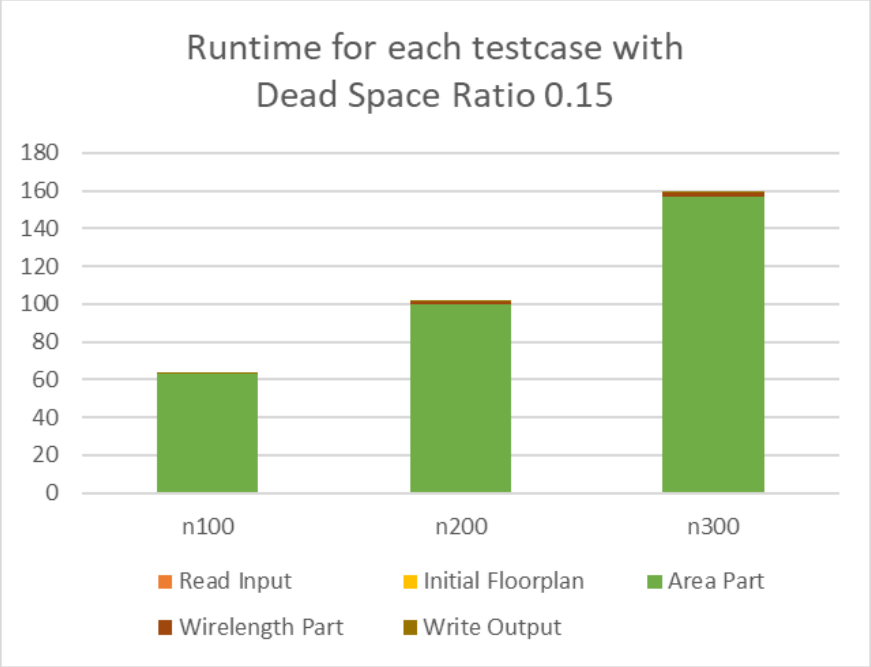
  ```
  $ make test
  ```

  Then, the terminal will let you enter the testcase (n100/n200/n300) and dead space ratio (0.1/0.15). After typing in the information, it will execute the corresponding testcase and write the result into the directory "../output/".

2) The wirelength and the runtime of each testcase with the dead space ratios 0.15 and 0.1, respectively:

Dead Space Ratio	0.15		
Testcase	n100	n200	n300
Read Input	0.00475	0.00474	0.00621
Initial Floorplan	0.00035	0.00070	0.00091
Area Part	62.909	100.024	156.779
Wirelength Part	0.315	1.331	2.481
Write Output	0.00091	0.00138	0.00178
Wirelength	304055	564237	843743
Runtime (sec.)	63.230	101.361	159.269

The graph below shows the timing in each part.



Dead Space Ratio	0.10		
Testcase	n100	n200	n300
Read Input	0.00379	0.00502	0.00541
Initial Floorplan	0.00027	0.00042	0.00070
Area Part	LTE	LTE	LTE
Wirelength Part	-	-	-
Write Output	-	-	-
Wirelength	-	-	-
Runtime (sec.)	-	-	-

Because the running time in the area part is LTE, I use "-" to represent the remaining part. Also, I skip the graph representation because of incomplete runtime information.

3) Please show that how small the dead space ratio could be for your program to produce a legal result in 10 minutes:

Because my results cannot meet the constraint with dead space ratio 0.1, I try to find out the minimum dead space ratio of each testcase. The table shows the result.

Teatcase	n100	n200	n300
Minimum Dead Space Ratio	0.12	0.15	0.14

4) The details of your implementation. If there is anything different between your implementation and the algorithm in the DAC-86 paper, please reveal the difference(s) and explain the reasons:
Most of my work follows the concept in the DAC-86 paper. But I still make some changes in my code. There are two differences between my work and the DAC-86 paper. First, the initial floorplan of the paper is to arrange all blocks into one line. But in my work, I insert "H" rather than "V" when the width of a row of blocks is larger than the boundary (the width under dead space ratio constraint). The reason for this change is that compared to the method in the paper, I think my way can reach the solution under dead space ratio constraints faster. Second, when calculating the cost function, I first consider the area. After finding a feasible solution, then consider both area and wirelength. In the first part, I use the difference between area constraint and my area as cost function. In the second part, I just consider wirelength as cost function. In each iteration, I only accept the floorplan whose width and height are under constraints.

5) What tricks did you do to speed up your program or to enhance your solution quality?
In the initial floorplan, I try to arrange blocks into square rather than just arrange them side by side vertically. This might help to reach a feasible solution faster.

6) Please compare your results with the previous top 3 students' results for the case where the dead space ratio is set to 0.15, and show your advantage either in runtime or in solution quality. Are your results better than theirs?

	Wirelength			Runtime (sec.)		
Rank	n100	n200	n300	n100	n200	n300
1	207309	367785	504903	13.97	84.54	263.33
2	209351	379674	521749	25.57	99.49	209.78
3	210220	392175	544879	37.45	105.83	486.73
Mine	304055	564237	843743	63.230	101.361	159.269

Obviously, my work is worse than theirs. After discussing it with my friends, I'm not really sure what the problems with my work are. Roughly guessing, I think the SA part can be improved. The design of the cost function might not good enough. Also, the probability of three different movements may have different weights.

7) What have you learned from this homework? What problem(s) have you encountered in this homework?

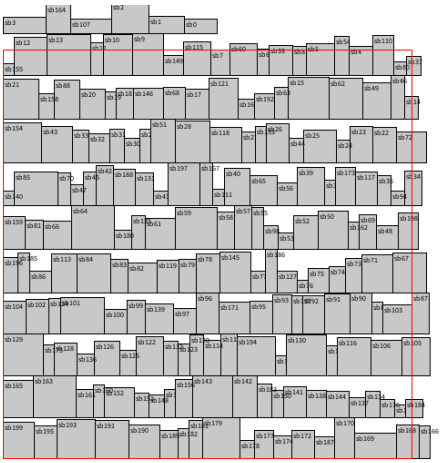
In this homework, I learned that the concept of producing a floorplan using simulated annealing was easy, but in practice, it is hard to find an ideal solution. Besides, we have to find the smallest rotation combination by using Stockmeyer's method, it takes time to find out a good way to store all the data. That is, the concepts of data structure and how to use them are important as well.

8) Floorplan for different stages

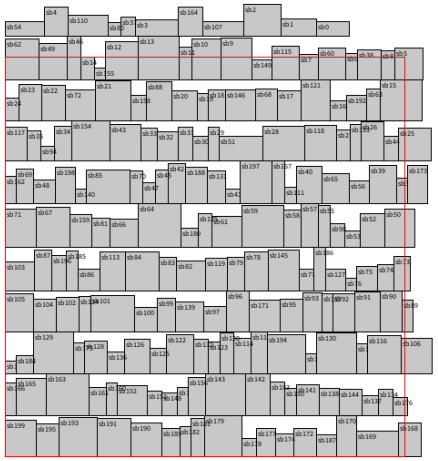
- Initial floorplan

n100 with dead space ratio 0.15

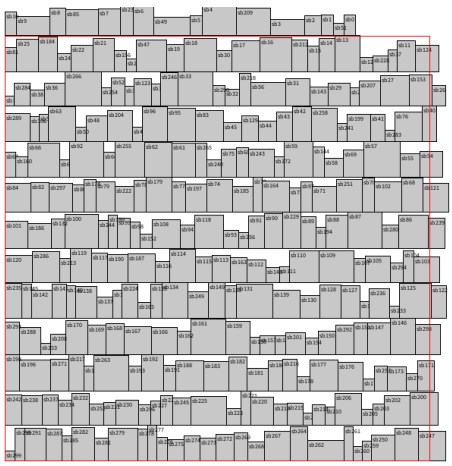
n100 with dead space ratio 0.10



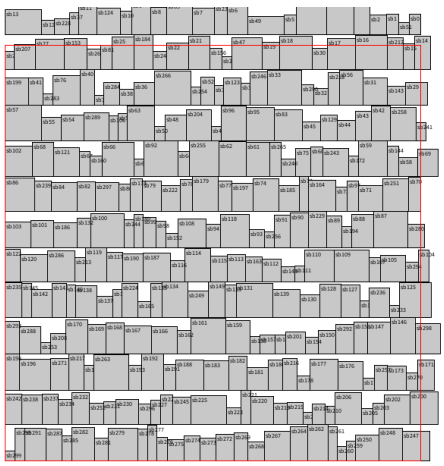
n200 with dead space ratio 0.15



n200 with dead space ratio 0.10

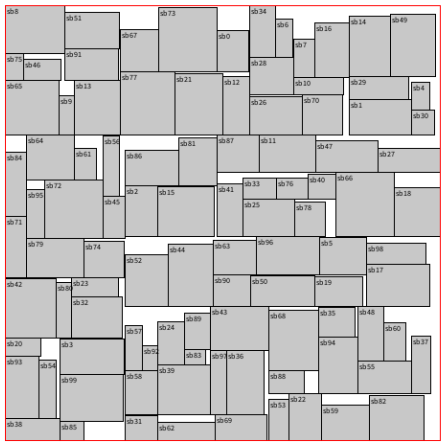


n300 + dead space ratio 0.15

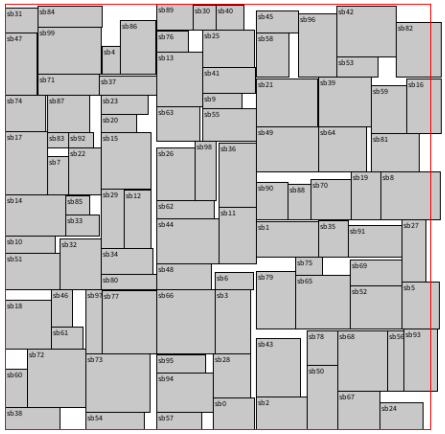


n300 + dead space ratio 0.10

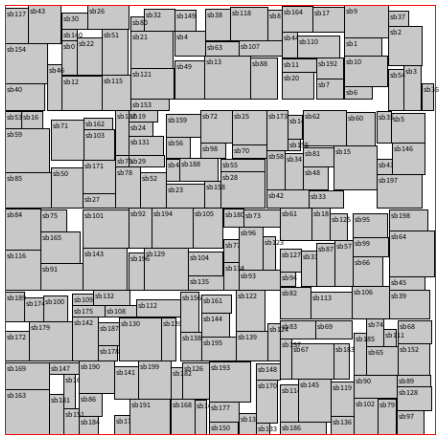
- Results (having some constraint-violated results)



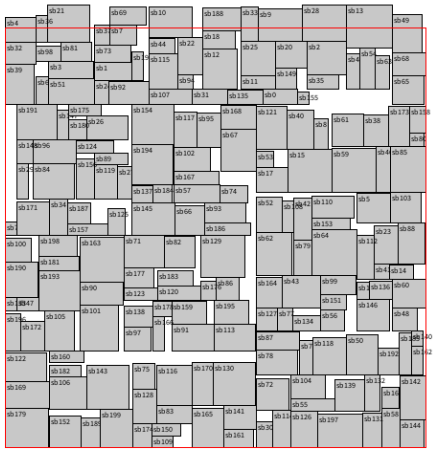
n100 + dead space ratio 0.15



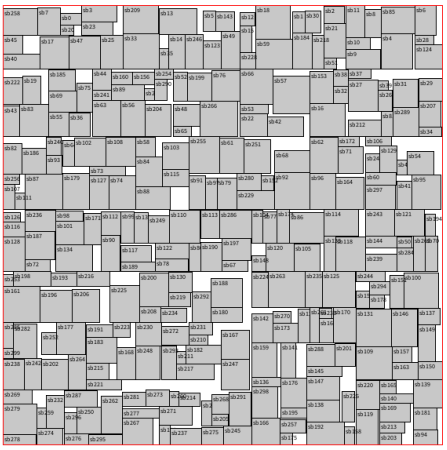
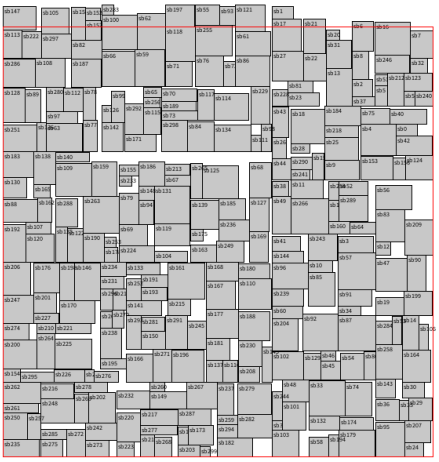
n100 + dead space ratio 0.10



n200 + dead space ratio 0.15



n200 + dead space ratio 0.10

	
n300 + dead space ratio 0.15	n300 + dead space ratio 0.10