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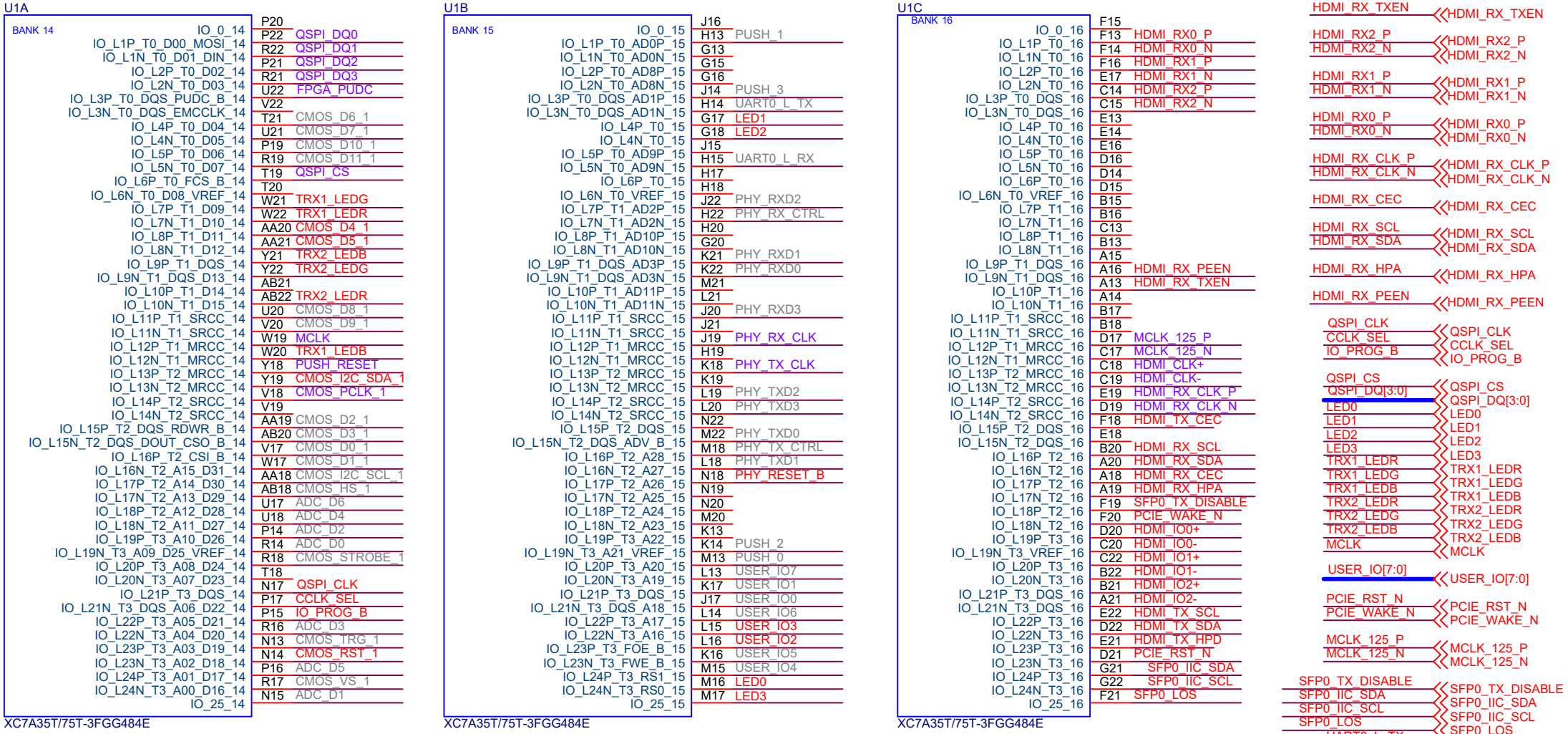
U1A
BANK 14
IO_0_14
IO_L1P_T0_D00_MOSI_14
IO_L1N_T0_D01_DIN_14
IO_L2P_T0_D02_14
IO_L2N_T0_D03_14
IO_L3P_T0_DQS_PUDC_B_14
IO_L3N_T0_DQS_EMCCLK_14
IO_L4P_T0_D04_14
IO_L4N_T0_D05_14
IO_L5P_T0_D06_14
IO_L5N_T0_D07_14
IO_L6P_T0_FCS_B_14
IO_L6N_T0_D08_VREF_14
IO_L7P_T1_D09_14
IO_L7N_T1_D10_14
IO_L8P_T1_D11_14
IO_L8N_T1_D12_14
IO_L9P_T1_DQS_14
IO_L9N_T1_DQS_D13_14
IO_L10P_T1_D14_14
IO_L10N_T1_D15_14
IO_L11P_T1_SRCC_14
IO_L11N_T1_SRCC_14
IO_L12P_T1_MRCC_14
IO_L12N_T1_MRCC_14
IO_L13P_T2_MRCC_14
IO_L13N_T2_MRCC_14
IO_L14P_T2_SRCC_14
IO_L14N_T2_SRCC_14
IO_L15P_T2_DQS_RDWR_B_14
IO_L15N_T2_DQS_DOUT_CSO_B_14
IO_L16P_T2_CSI_B_14
IO_L16N_T2_A15_D31_14
IO_L17P_T2_A14_D30_14
IO_L17N_T2_A13_D29_14
IO_L18P_T2_A12_D28_14
IO_L18N_T2_A11_D27_14
IO_L19P_T3_A10_D26_14
IO_L19N_T3_A09_D25_VREF_14
IO_L20P_T3_A08_D24_14
IO_L20N_T3_A07_D23_14
IO_L21P_T3_DQS_14
IO_L21N_T3_DQS_A06_D22_14
IO_L22P_T3_A05_D21_14
IO_L22N_T3_A04_D20_14
IO_L23P_T3_A03_D19_14
IO_L23N_T3_A02_D18_14
IO_L24P_T3_A01_D17_14
IO_L24N_T3_A00_D16_14
IO_25_14
P20
P22 QSPI_DQ0
R22 QSPI_DQ1
P21 QSPI_DQ2
R21 QSPI_DQ3
U22 FPGA_PUDC
V22
T21 CMOS_D6_1
U21 CMOS_D7_1
P19 CMOS_D10_1
R19 CMOS_D11_1
T19 QSPI_CS
T20
W21 TRX1_LEDG
W22 TRX1_LEDR
AA20 CMOS_D4_1
AA21 CMOS_D5_1
Y21 TRX2_LEDB
Y22 TRX2_LEDG
AB21
AB22 TRX2_LEDR
U20 CMOS_D8_1
V20 CMOS_D9_1
W19 MCLK
W20 TRX1_LEDB
Y18 PUSH_RESET
Y19 CMOS_I2C_SDA_1
V18 CMOS_PCLK_1
V19
AA19 CMOS_D2_1
AB20 CMOS_D3_1
V17 CMOS_D0_1
W17 CMOS_D1_1
AA18 CMOS_I2C_SCL_1
AB18 CMOS_HS_1
U17 ADC_D6
U18 ADC_D4
P14 ADC_D2
R14 ADC_D0
R18 CMOS_STROBE_1
T18
N17 QSPI_CLK
P17 CCLK_SEL
P15 IO_PROG_B
R16 ADC_D3
N13 CMOS_TRG_1
N14 CMOS_RST_1
P16 ADC_D5
R17 CMOS_VS_1
N15 ADC_D1
XC7A35T/75T-3FGG484E
U1B
BANK 15
IO_0_15
IO_L1P_T0_AD0P_15
IO_L1N_T0_AD0N_15
IO_L2P_T0_AD8P_15
IO_L2N_T0_AD8N_15
IO_L3P_T0_DQS_AD1P_15
IO_L3N_T0_DQS_AD1N_15
IO_L4P_T0_15
IO_L4N_T0_15
IO_L5P_T0_AD9P_15
IO_L5N_T0_AD9N_15
IO_L6P_T0_15
IO_L6N_T0_VREF_15
IO_L7P_T1_AD2P_15
IO_L7N_T1_AD2N_15
IO_L8P_T1_AD10P_15
IO_L8N_T1_AD10N_15
IO_L9P_T1_DQS_AD3P_15
IO_L9N_T1_DQS_AD3N_15
IO_L10P_T1_AD11P_15
IO_L10N_T1_AD11N_15
IO_L11P_T1_SRCC_15
IO_L11N_T1_SRCC_15
IO_L12P_T1_MRCC_15
IO_L12N_T1_MRCC_15
IO_L13P_T2_MRCC_15
IO_L13N_T2_MRCC_15
IO_L14P_T2_SRCC_15
IO_L14N_T2_SRCC_15
IO_L15P_T2_DQS_15
IO_L15N_T2_DQS_ADV_B_15
IO_L16P_T2_A28_15
IO_L16N_T2_A27_15
IO_L17P_T2_A26_15
IO_L17N_T2_A25_15
IO_L18P_T2_A24_15
IO_L18N_T2_A23_15
IO_L19P_T3_A22_15
IO_L19N_T3_A21_VREF_15
IO_L20P_T3_A20_15
IO_L20N_T3_A19_15
IO_L21P_T3_DQS_15
IO_L21N_T3_DQS_A18_15
IO_L22P_T3_A17_15
IO_L22N_T3_A16_15
IO_L23P_T3_FOE_B_15
IO_L23N_T3_FWE_B_15
IO_L24P_T3_RS1_15
IO_L24N_T3_RS0_15
IO_25_15
J16
H13 PUSH_1
G13
G15
G16
J14 PUSH_3
H14 UART0_L_TX
G17 LED1
G18 LED2
J15
H15 UART0_L_RX
H17
H18
J22 PHY_RXD2
H22 PHY_RX_CTRL
H20
G20
K21 PHY_RXD1
K22 PHY_RXD0
M21
L21
J20 PHY_RXD3
J21
J19 PHY_RX_CLK
H19
K18 PHY_TX_CLK
K19
L19 PHY_TXD2
L20 PHY_TXD3
N22
M22 PHY_TXD0
M18 PHY_TX_CTRL
L18 PHY_TXD1
N18 PHY_RESET_B
N19
N20
M20
K13
K14 PUSH_2
M13 PUSH_0
L13 USER_IO7
K17 USER_IO1
J17 USER_IO0
L14 USER_IO6
L15 USER_IO3
L16 USER_IO2
K16 USER_IO5
M15 USER_IO4
M16 LED0
M17 LED3
XC7A35T/75T-3FGG484E
U1C
BANK 16
IO_0_16
IO_L1P_T0_16
IO_L1N_T0_16
IO_L2P_T0_16
IO_L2N_T0_16
IO_L3P_T0_DQS_16
IO_L3N_T0_DQS_16
IO_L4P_T0_16
IO_L4N_T0_16
IO_L5P_T0_16
IO_L5N_T0_16
IO_L6P_T0_16
IO_L6N_T0_VREF_16
IO_L7P_T1_16
IO_L7N_T1_16
IO_L8P_T1_16
IO_L8N_T1_16
IO_L9P_T1_DQS_16
IO_L9N_T1_DQS_16
IO_L10P_T1_16
IO_L10N_T1_16
IO_L11P_T1_SRCC_16
IO_L11N_T1_SRCC_16
IO_L12P_T1_MRCC_16
IO_L12N_T1_MRCC_16
IO_L13P_T2_MRCC_16
IO_L13N_T2_MRCC_16
IO_L14P_T2_SRCC_16
IO_L14N_T2_SRCC_16
IO_L15P_T2_DQS_16
IO_L15N_T2_DQS_16
IO_L16P_T2_16
IO_L16N_T2_16
IO_L17P_T2_16
IO_L17N_T2_16
IO_L18P_T2_16
IO_L18N_T2_16
IO_L19P_T3_16
IO_L19N_T3_VREF_16
IO_L20P_T3_16
IO_L20N_T3_16
IO_L21P_T3_DQS_16
IO_L21N_T3_DQS_16
IO_L22P_T3_16
IO_L22N_T3_16
IO_L23P_T3_16
IO_L23N_T3_16
IO_L24P_T3_16
IO_L24N_T3_16
IO_25_16
F15
F13 HDMI_RX0_P
F14 HDMI_RX0_N
F16 HDMI_RX1_P
E17 HDMI_RX1_N
C14 HDMI_RX2_P
C15 HDMI_RX2_N
E13
E14
E16
D16
D14
D15
B15
B16
C13
B13
A15
A16 HDMI_RX_PEEN
A13 HDMI_RX_TXEN
A14
B17
B18
D17 MCLK_125_P
C17 MCLK_125_N
C18 HDMI_CLK+
C19 HDMI_CLK-
E19 HDMI_RX_CLK_P
D19 HDMI_RX_CLK_N
F18 HDMI_TX_CEC
E18
B20 HDMI_RX_SCL
A20 HDMI_RX_SDA
A18 HDMI_RX_CEC
A19 HDMI_RX_HPA
F19 SFP0_TX_DISABLE
F20 PCIE_WAKE_N
D20 HDMI_IO0+
C20 HDMI_IO0-
C22 HDMI_IO1+
B22 HDMI_IO1-
B21 HDMI_IO2+
A21 HDMI_IO2-
E22 HDMI_TX_SCL
D22 HDMI_TX_SDA
E21 HDMI_TX_HPD
D21 PCIE_RST_N
G21 SFP0_IIC_SDA
G22 SFP0_IIC_SCL
F21 SFP0_LOS
XC7A35T/75T-3FGG484E
FPGA_PUDC RF1 NC 3.3V
FPGA_PUDC RF2 4.7K DGND
CMOS_D0_1
CMOS_D1_1
CMOS_D0_1
CMOS_D1_1
CMOS_D2_1
CMOS_D3_1
CMOS_D2_1
CMOS_D3_1
CMOS_D4_1
CMOS_D5_1
CMOS_D4_1
CMOS_D5_1
CMOS_D6_1
CMOS_D7_1
CMOS_D6_1
CMOS_D7_1
CMOS_D8_1
CMOS_D9_1
CMOS_D8_1
CMOS_D9_1
CMOS_D10_1
CMOS_D11_1
CMOS_D10_1
CMOS_D11_1
CMOS_PCLK_1
CMOS_HS_1
CMOS_VS_1
CMOS_RST_1
CMOS_TRG_1
CMOS_STROBE_1
CMOS_I2C_SCL_1
CMOS_I2C_SDA_1
CMOS_PCLK_1
CMOS_HS_1
CMOS_VS_1
CMOS_RST_1
CMOS_TRG_1
CMOS_STROBE_1
CMOS_I2C_SCL_1
CMOS_I2C_SDA_1
ADC_D0
ADC_D1
ADC_D2
ADC_D3
ADC_D4
ADC_D5
ADC_D6
ADC_D0
ADC_D1
ADC_D2
ADC_D3
ADC_D4
ADC_D5
ADC_D6
PUSH_0
PUSH_1
PUSH_2
PUSH_3
PUSH_RESET
PHY_RXD[3:0]
PHY_TXD[3:0]
PHY_RX_CLK
PHY_TX_CLK
PHY_RX_CTRL
PHY_TX_CTRL
PHY_RESET_B
PUSH_0
PUSH_1
PUSH_2
PUSH_3
PUSH_RESET
PHY_RXD[3:0]
PHY_TXD[3:0]
PHY_RX_CLK
PHY_TX_CLK
PHY_RX_CTRL
PHY_TX_CTRL
PHY_RESET_B
HDMI_RX_TXEN
HDMI_RX_TXEN
HDMI_RX2_P
HDMI_RX2_N
HDMI_RX2_P
HDMI_RX2_N
HDMI_RX1_P
HDMI_RX1_N
HDMI_RX1_P
HDMI_RX1_N
HDMI_RX0_P
HDMI_RX0_N
HDMI_RX0_P
HDMI_RX0_N
HDMI_RX_CLK_P
HDMI_RX_CLK_N
HDMI_RX_CLK_P
HDMI_RX_CLK_N
HDMI_RX_CEC
HDMI_RX_CEC
HDMI_RX_SCL
HDMI_RX_SDA
HDMI_RX_SCL
HDMI_RX_SDA
HDMI_RX_HPA
HDMI_RX_HPA
HDMI_RX_PEEN
HDMI_RX_PEEN
QSPI_CLK
CCLK_SEL
IO_PROG_B
QSPI_CLK
CCLK_SEL
IO_PROG_B
QSPI_CS
QSPI_DQ[3:0]
QSPI_CS
QSPI_DQ[3:0]
LED0
LED1
LED2
LED3
TRX1_LEDR
TRX1_LEDG
TRX1_LEDB
TRX2_LEDR
TRX2_LEDG
TRX2_LEDB
MCLK
LED0
LED1
LED2
LED3
TRX1_LEDR
TRX1_LEDG
TRX1_LEDB
TRX2_LEDR
TRX2_LEDG
TRX2_LEDB
MCLK
USER_IO[7:0]
USER_IO[7:0]
PCIE_RST_N
PCIE_WAKE_N
PCIE_RST_N
PCIE_WAKE_N
MCLK_125_P
MCLK_125_N
MCLK_125_P
MCLK_125_N
SFP0_TX_DISABLE
SFP0_IIC_SDA
SFP0_IIC_SCL
SFP0_LOS
SFP0_TX_DISABLE
SFP0_IIC_SDA
SFP0_IIC_SCL
SFP0_LOS
UART0_L_TX
UART0_L_RX
HDMI_TX_HPD
HDMI_TX_CEC
UART0_L_TX
UART0_L_RX
HDMI_TX_HPD
HDMI_TX_CEC
HDMI_IO2+
HDMI_IO2-
HDMI_IO1+
HDMI_IO1-
HDMI_IO0+
HDMI_IO0-
HDMI_CLK+
HDMI_CLK-
HDMI_TX_SCL
HDMI_TX_SDA
HDMI_IO2+
HDMI_IO2-
HDMI_IO1+
HDMI_IO1-
HDMI_IO0+
HDMI_IO0-
HDMI_CLK+
HDMI_CLK-
HDMI_TX_SCL
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PS_DDR3_DQ[15:0]
PS_DDR3_DQ[15:0]
U1D
BANK 34
IO_0_34 T3
T1 PS_DDR3_A10
IO_L1P_T0_34 U1 PS_DDR3_RAS_B
IO_L1N_T0_34 U2 PS_DDR3_BA1
IO_L2P_T0_34 V2 PS_DDR3_CAS_B
IO_L2N_T0_34 R3 PS_DDR3_CLK_P
IO_L3P_T0_DQS_34 R2 PS_DDR3_CLK_N
IO_L3N_T0_DQS_34 W2 PS_DDR3_A1
IO_L4P_T0_34 Y2 PS_DDR3_A11
IO_L4N_T0_34 W1 PS_DDR3_A4
IO_L5P_T0_34 Y1 PS_DDR3_A6
IO_L5N_T0_34 U3 PS_DDR3_A12
IO_L6P_T0_34 V3 PS_DDR3_CS_B
IO_L6N_T0_VREF_34 AA1 PS_DDR3_A8
IO_L7P_T1_34 AB1 PS_DDR3_BA2
IO_L7N_T1_34 AB3 PS_DDR3_A2
IO_L8P_T1_34 AB2 PS_DDR3_A0
IO_L8N_T1_34 Y3 PS_DDR3_A3
IO_L9P_T1_DQS_34 AA3 PS_DDR3_A5
IO_L9N_T1_DQS_34 AA5 PS_DDR3_A9
IO_L10P_T1_34 AB5 PS_DDR3_A13
IO_L10N_T1_34 Y4 PS_DDR3_A14
IO_L11P_T1_SRCC_34 AA4 PS_DDR3_A7
IO_L11N_T1_SRCC_34 V4 PS_DDR3_WE_B
IO_L12P_T1_MRCC_34 W4 PS_DDR3_BA0
IO_L12N_T1_MRCC_34 R4
IO_L13P_T2_MRCC_34 T4
IO_L13N_T2_MRCC_34 T5
IO_L14P_T2_SRCC_34 U5
IO_L14N_T2_SRCC_34 W6 PS_DDR3_CKE
IO_L15P_T2_DQS_34 W5 PS_DDR3_ODT
IO_L15N_T2_DQS_34 U6
IO_L16P_T2_34 V5
IO_L16N_T2_34 R6
IO_L17P_T2_34 T6
IO_L17N_T2_34 Y6
IO_L18P_T2_34 AA6
IO_L18N_T2_34 V7
IO_L19P_T3_34 W7
IO_L19N_T3_VREF_34 AB7 VREF_DDR
IO_L20P_T3_34 AB6
IO_L20N_T3_34 V9
IO_L21P_T3_DQS_34 V8
IO_L21N_T3_DQS_34 AA8
IO_L22P_T3_34 AB8
IO_L22N_T3_34 Y8
IO_L23P_T3_34 Y7
IO_L23N_T3_34 W9
IO_L24P_T3_34 Y9
IO_L24N_T3_34 U7
IO_25_34
XC7A35T/75T-3FGG484E
U1E
BANK 35
IO_0_35 F4
B1 PS_DDR3_DM0
IO_L1P_T0_AD4P_35 A1 PS_DDR3_DQ0
IO_L1N_T0_AD4N_35 C2 PS_DDR3_DQ1
IO_L2P_T0_AD12P_35 B2 PS_DDR3_DQ2
IO_L2N_T0_AD12N_35 E1 PS_DDR3_DQS0_P
IO_L3P_T0_DQS_AD5P_35 D1 PS_DDR3_DQS0_N
IO_L3N_T0_DQS_AD5N_35 E2 PS_DDR3_DQ3
IO_L4P_T0_35 D2 PS_DDR3_DQ4
IO_L4N_T0_35 G1 PS_DDR3_DQ5
IO_L5P_T0_AD13P_35 F1 PS_DDR3_DQ6
IO_L5N_T0_AD13N_35 F3 PS_DDR3_DQ7
IO_L6P_T0_35 E3
IO_L6N_T0_VREF_35 K1 PS_DDR3_DM1
IO_L7P_T1_AD6P_35 J1 PS_DDR3_DQ8
IO_L7N_T1_AD6N_35 H2 PS_DDR3_DQ9
IO_L8P_T1_AD14P_35 G2 PS_DDR3_DQ10
IO_L8N_T1_AD14N_35 K2 PS_DDR3_DQS1_P
IO_L9P_T1_DQS_AD7P_35 J2 PS_DDR3_DQS1_N
IO_L9N_T1_DQS_AD7N_35 J5 PS_DDR3_DQ11
IO_L10P_T1_AD15P_35 H5 PS_DDR3_DQ12
IO_L10N_T1_AD15N_35 H3 PS_DDR3_DQ13
IO_L11P_T1_SRCC_35 G3 PS_DDR3_DQ14
IO_L11N_T1_SRCC_35 H4 PS_DDR3_DQ15
IO_L12P_T1_MRCC_35 G4 PS_DDR3_RESET_B
IO_L12N_T1_MRCC_35 K4
IO_L13P_T2_MRCC_35 J4
IO_L13N_T2_MRCC_35 L3
IO_L14P_T2_SRCC_35 K3
IO_L14N_T2_SRCC_35 M1
IO_L15P_T2_DQS_35 L1
IO_L15N_T2_DQS_35 M3
IO_L16P_T2_35 M2
IO_L16N_T2_35 K6
IO_L17P_T2_35 J6
IO_L17N_T2_35 L5
IO_L18P_T2_35 L4
IO_L18N_T2_35 N4
IO_L19P_T3_35 N3
IO_L19N_T3_VREF_35 R1 VREF_DDR
IO_L20P_T3_35 P1
IO_L20N_T3_35 P5
IO_L21P_T3_DQS_35 P4
IO_L21N_T3_DQS_35 P2
IO_L22P_T3_35 N2
IO_L22N_T3_35 M6
IO_L23P_T3_35 M5
IO_L23N_T3_35 P6
IO_L24P_T3_35 N5
IO_L24N_T3_35 L6
IO_25_35 L6
XC7A35T/75T-3FGG484E
PS_DDR3_DQS1_N
PS_DDR3_DQS1_P
PS_DDR3_DQS0_N
PS_DDR3_DQS0_P
PS_DDR3_DM[1:0]
PS_DDR3_DQS1_N
PS_DDR3_DQS1_P
PS_DDR3_DQS0_N
PS_DDR3_DQS0_P
PS_DDR3_DM[1:0]
PS_DDR3_RAS_B
PS_DDR3_CAS_B
PS_DDR3_WE_B
PS_DDR3_CKE
PS_DDR3_CS_B
PS_DDR3_ODT
PS_DDR3_CLK_N
PS_DDR3_CLK_P
PS_DDR3_RESET_B
PS_DDR3_RAS_B
PS_DDR3_CAS_B
PS_DDR3_WE_B
PS_DDR3_CKE
PS_DDR3_CS_B
PS_DDR3_ODT
PS_DDR3_CLK_N
PS_DDR3_CLK_P
PS_DDR3_RESET_B
PS_DDR3_BA[2:0]
PS_DDR3_A[14:0]
PS_DDR3_BA[2:0]
PS_DDR3_A[14:0]
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Size A4	Document Number 03 FPGA_BANK_MGT	Rev V2.0
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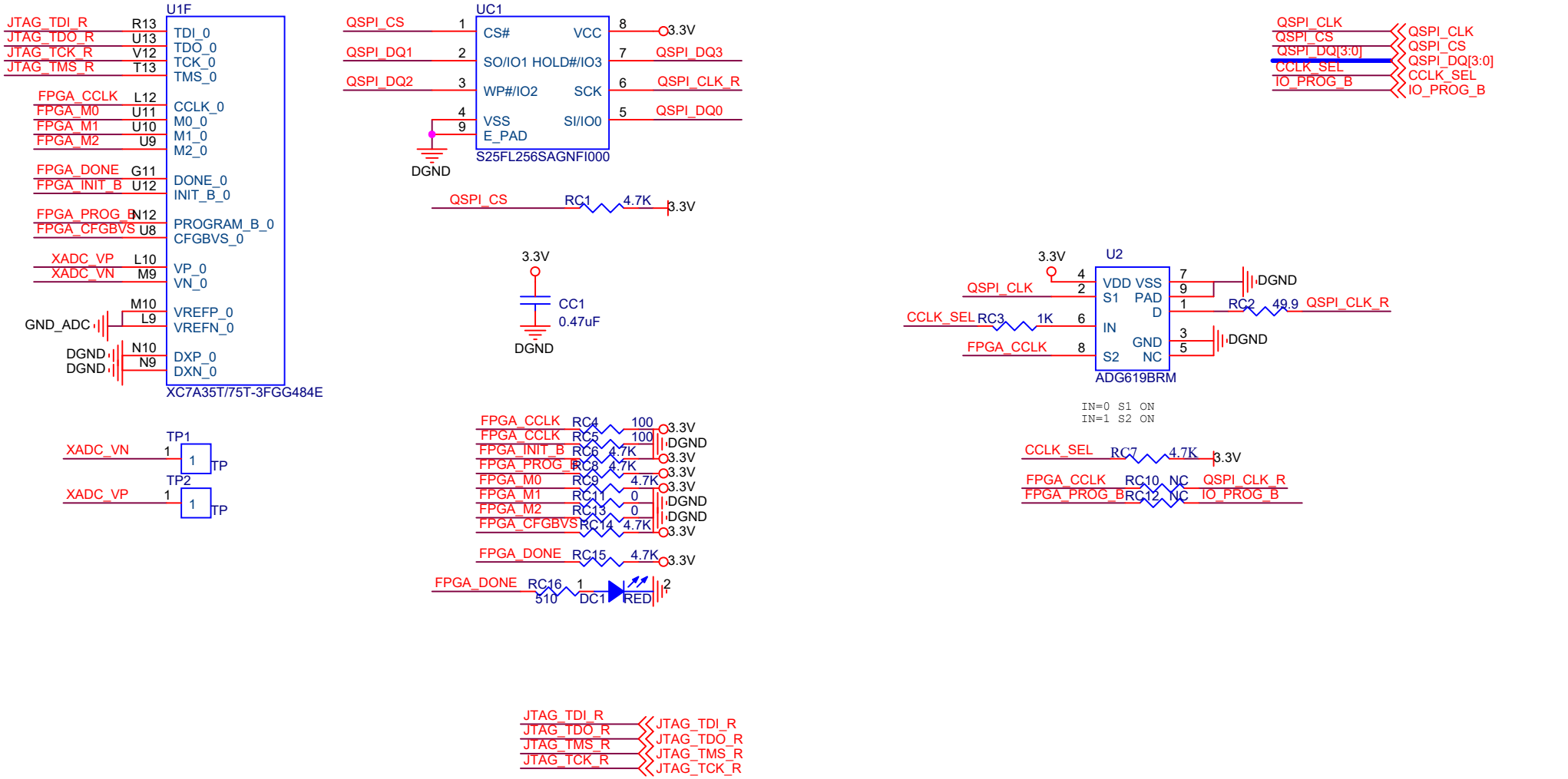
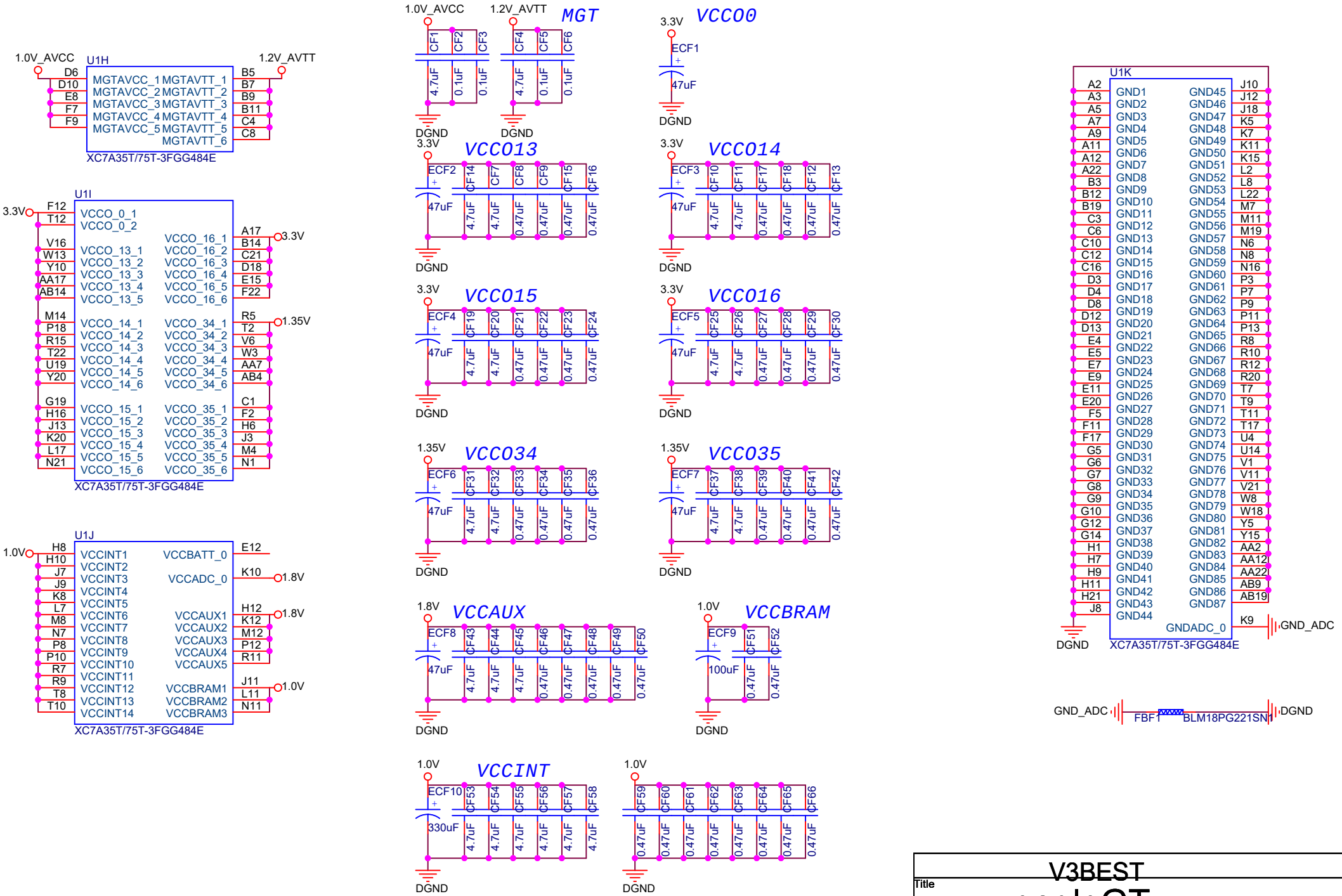


Title	V3BEST eagleGT	
Size A4	Document Number 04 FPGA_CONFIG	Rev V2.0
Date: Monday, April 22, 2019	Sheet 5 of 14	


1.0V_AVCC
1.2V_AVTT
MGT
U1H
MGTAVCC_1 MGTAVTT_1
MGTAVCC_2 MGTAVTT_2
MGTAVCC_3 MGTAVTT_3
MGTAVCC_4 MGTAVTT_4
MGTAVCC_5 MGTAVTT_5
MGTAVTT_6
XC7A35T/75T-3FGG484E
3.3V
VCCO0
ECF1
47uF
DGND
VCCO13
ECF2
VCCO14
ECF3
VCCO15
ECF4
VCCO16
ECF5
1.35V
VCCO34
ECF6
VCCO35
ECF7
1.8V
VCCAUX
ECF8
1.0V
VCCBRAM
ECF9
100uF
VCCINT
ECF10
330uF
U1I
VCCO_0_1
VCCO_0_2
VCCO_16_1
VCCO_16_2
VCCO_16_3
VCCO_16_4
VCCO_16_5
VCCO_16_6
VCCO_13_1
VCCO_13_2
VCCO_13_3
VCCO_13_4
VCCO_13_5
VCCO_14_1
VCCO_14_2
VCCO_14_3
VCCO_14_4
VCCO_14_5
VCCO_14_6
VCCO_34_1
VCCO_34_2
VCCO_34_3
VCCO_34_4
VCCO_34_5
VCCO_34_6
VCCO_15_1
VCCO_15_2
VCCO_15_3
VCCO_15_4
VCCO_15_5
VCCO_15_6
VCCO_35_1
VCCO_35_2
VCCO_35_3
VCCO_35_4
VCCO_35_5
VCCO_35_6
U1J
VCCINT1
VCCINT2
VCCINT3
VCCINT4
VCCINT5
VCCINT6
VCCINT7
VCCINT8
VCCINT9
VCCINT10
VCCINT11
VCCINT12
VCCINT13
VCCINT14
VCCBATT_0
VCCADC_0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCBRAM1
VCCBRAM2
VCCBRAM3
U1K
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18 GND19 GND20 GND21 GND22 GND23 GND24 GND25 GND26 GND27 GND28 GND29 GND30 GND31 GND32 GND33 GND34 GND35 GND36 GND37 GND38 GND39 GND40 GND41 GND42 GND43 GND44
GND45 GND46 GND47 GND48 GND49 GND50 GND51 GND52 GND53 GND54 GND55 GND56 GND57 GND58 GND59 GND60 GND61 GND62 GND63 GND64 GND65 GND66 GND67 GND68 GND69 GND70 GND71 GND72 GND73 GND74 GND75 GND76 GND77 GND78 GND79 GND80 GND81 GND82 GND83 GND84 GND85 GND86 GND87
GNDADC_0
GND_ADC
FBF1
BLM18PG221SN1
V3BEST
eagleGT
05 FPGA_POWER
Size A4
Document Number
Rev V2.0
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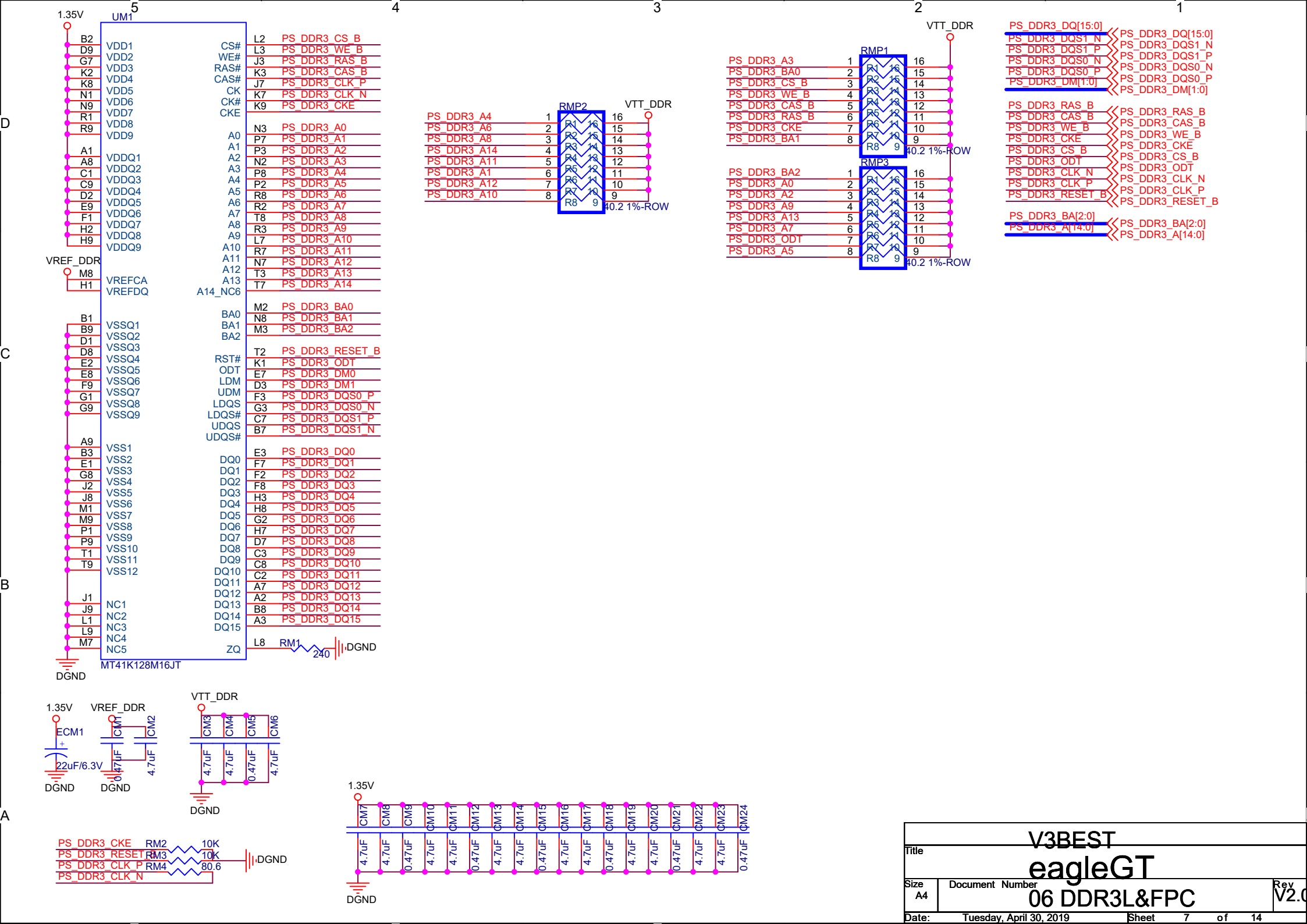
1.35V
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VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VREF_DDR
VREFCA
VREFDQ
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
VSSQ6
VSSQ7
VSSQ8
VSSQ9
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
NC1
NC2
NC3
NC4
NC5
DGND
MT41K128M16JT
CS#
WE#
RAS#
CAS#
CK
CK#
CKE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14_NC6
BA0
BA1
BA2
RST#
ODT
LDM
UDM
LDQS
LDQS#
UDQS
UDQS#
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
ZQ
PS_DDR3_CS_B
PS_DDR3_WE_B
PS_DDR3_RAS_B
PS_DDR3_CAS_B
PS_DDR3_CLK_P
PS_DDR3_CLK_N
PS_DDR3_CKE
PS_DDR3_A0
PS_DDR3_A1
PS_DDR3_A2
PS_DDR3_A3
PS_DDR3_A4
PS_DDR3_A5
PS_DDR3_A6
PS_DDR3_A7
PS_DDR3_A8
PS_DDR3_A9
PS_DDR3_A10
PS_DDR3_A11
PS_DDR3_A12
PS_DDR3_A13
PS_DDR3_A14
PS_DDR3_BA0
PS_DDR3_BA1
PS_DDR3_BA2
PS_DDR3_RESET_B
PS_DDR3_ODT
PS_DDR3_DM0
PS_DDR3_DM1
PS_DDR3_DQS0_P
PS_DDR3_DQS0_N
PS_DDR3_DQS1_P
PS_DDR3_DQS1_N
PS_DDR3_DQ0
PS_DDR3_DQ1
PS_DDR3_DQ2
PS_DDR3_DQ3
PS_DDR3_DQ4
PS_DDR3_DQ5
PS_DDR3_DQ6
PS_DDR3_DQ7
PS_DDR3_DQ8
PS_DDR3_DQ9
PS_DDR3_DQ10
PS_DDR3_DQ11
PS_DDR3_DQ12
PS_DDR3_DQ13
PS_DDR3_DQ14
PS_DDR3_DQ15
RM1
240
RMP2
VTT_DDR
40.2 1%-ROW
RMP1
RMP3
PS_DDR3_DQ[15:0]
PS_DDR3_DQS1_N
PS_DDR3_DQS1_P
PS_DDR3_DQS0_N
PS_DDR3_DQS0_P
PS_DDR3_DM[1:0]
PS_DDR3_RAS_B
PS_DDR3_CAS_B
PS_DDR3_WE_B
PS_DDR3_CKE
PS_DDR3_CS_B
PS_DDR3_ODT
PS_DDR3_CLK_N
PS_DDR3_CLK_P
PS_DDR3_RESET_B
PS_DDR3_BA[2:0]
PS_DDR3_A[14:0]
ECM1
22uF/6.3V
CM1
CM2
CM3
CM4
CM5
CM6
CM7
CM8
CM9
CM10
CM11
CM12
CM13
CM14
CM15
CM16
CM17
CM18
CM19
CM20
CM21
CM22
CM23
CM24
0.47uF
4.7uF
RM2
RM3
RM4
10K
80.6
V3BEST
eagleGT
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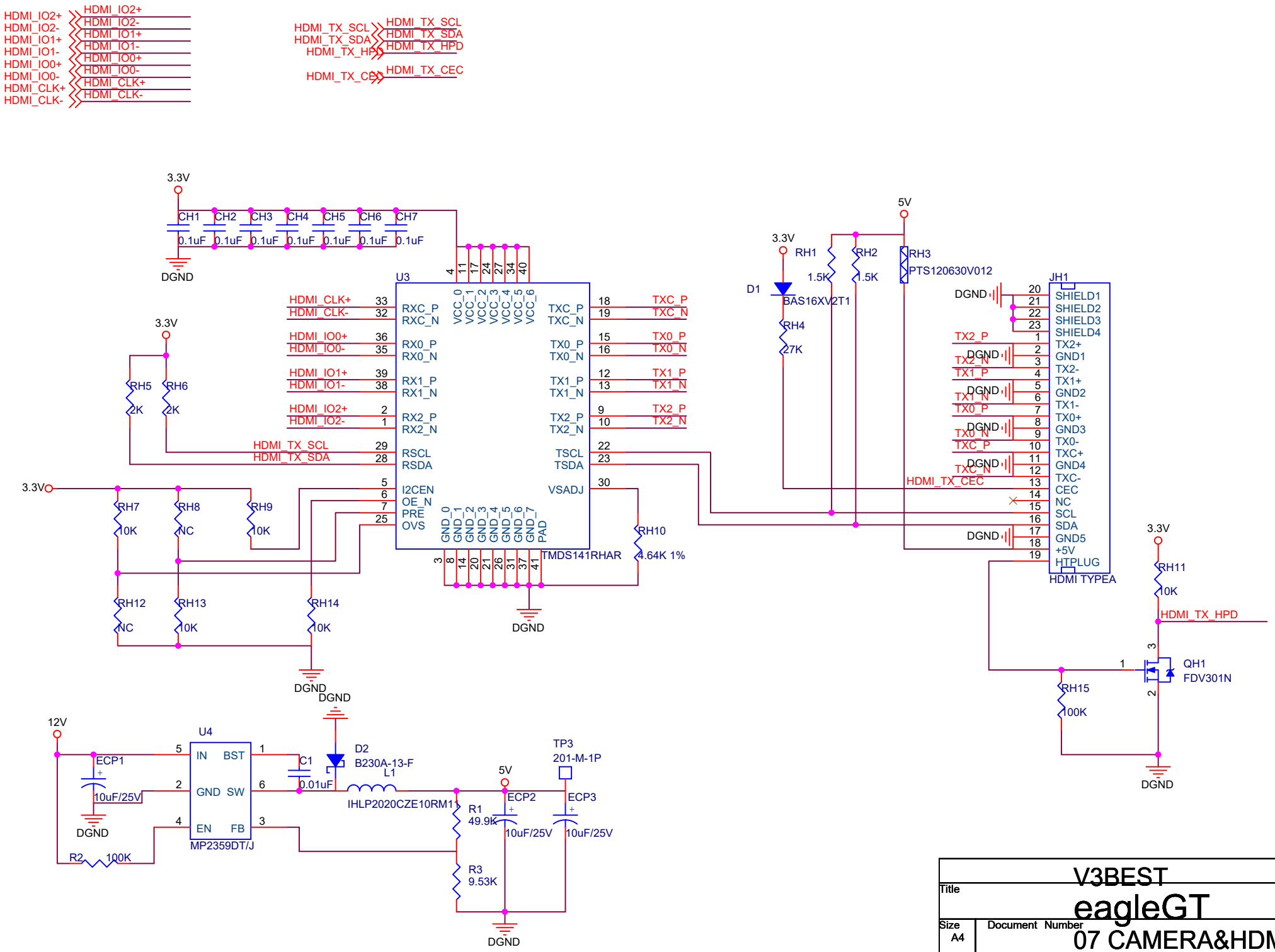
Size
A4
Document Number
Rev
V2.0
Date:
Tuesday, April 30, 2019
Sheet
7
of
14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HDMI_IO2-
HDMI_IO1+
HDMI_IO1-
HDMI_IO0+
HDMI_IO0-
HDMI_CLK+
HDMI_CLK-
HDMI_TX_SCL
HDMI_TX_SDA
HDMI_TX_HPD
HDMI_TX_CEC
3.3V
CH1 CH2 CH3 CH4 CH5 CH6 CH7
0.1uF
DGND
U3
HDMI_CLK+ 33
HDMI_CLK- 32
RXC_P
RXC_N
HDMI_IO0+ 36
HDMI_IO0- 35
RX0_P
RX0_N
HDMI_IO1+ 39
HDMI_IO1- 38
RX1_P
RX1_N
HDMI_IO2+ 2
HDMI_IO2- 1
RX2_P
RX2_N
HDMI_TX_SCL 29
HDMI_TX_SDA 28
RSCL
RSDA
I2CEN
OE_N
PRE
OVS
VCC_0 VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6
GND_0 GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 PAD
TXC_P
TXC_N
TX0_P
TX0_N
TX1_P
TX1_N
TX2_P
TX2_N
TSCL
TSDA
VSADJ
TMDS141RHAR
RH5 2K
RH6 2K
RH7 10K
RH8 NC
RH9 10K
RH10 4.64K 1%
RH12 NC
RH13 10K
RH14 10K
5V
RH1 1.5K
RH2 1.5K
RH3 PTS120630V012
D1 BAS16XV2T1
RH4 27K
JH1
SHIELD1
SHIELD2
SHIELD3
SHIELD4
TX2+
GND1
TX2-
TX1+
GND2
TX1-
TX0+
GND3
TX0-
TXC+
GND4
TXC-
CEC
NC
SCL
SDA
GND5
+5V
HTPLUG
HDMI TYPEA
RH11 10K
HDMI_TX_HPD
QH1
FDV301N
RH15 100K
12V
U4
IN BST
GND SW
EN FB
MP2359DT/J
ECP1 10uF/25V
C1 0.01uF
D2
B230A-13-F
L1
IHLP2020CZE10RM11
R1 49.9K
R2 100K
R3 9.53K
ECP2 10uF/25V
ECP3 10uF/25V
TP3
201-M-1P
V3BEST
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eagleGT
Size A4
Document Number
07 CAMERA&HDMI
Rev V2.0
Date: Sunday, May 05, 2019
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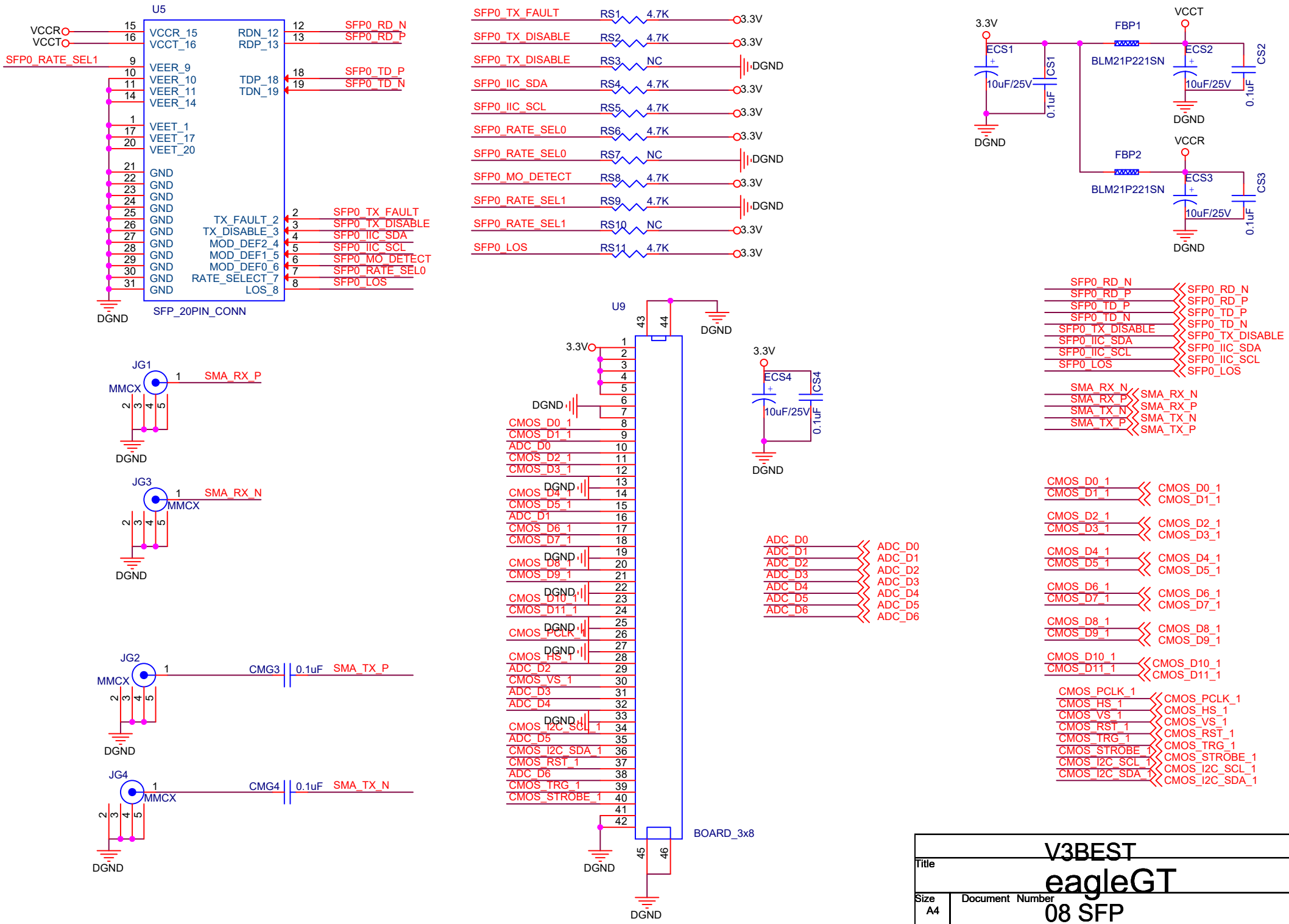
U5
VCCR
VCCT
SFP0_RATE_SEL1
VCCR_15
VCCT_16
VEER_9
VEER_10
VEER_11
VEER_14
VEET_1
VEET_17
VEET_20
GND
RDN_12
RDP_13
TDP_18
TDN_19
TX_FAULT_2
TX_DISABLE_3
MOD_DEF2_4
MOD_DEF1_5
MOD_DEF0_6
RATE_SELECT_7
LOS_8
SFP0_RD_N
SFP0_RD_P
SFP0_TD_P
SFP0_TD_N
SFP0_TX_FAULT
SFP0_TX_DISABLE
SFP0_IIC_SDA
SFP0_IIC_SCL
SFP0_MO_DETECT
SFP0_RATE_SEL0
SFP0_LOS
SFP_20PIN_CONN
DGND
SFP0_TX_FAULT RS1 4.7K 3.3V
SFP0_TX_DISABLE RS2 4.7K 3.3V
SFP0_TX_DISABLE RS3 NC DGND
SFP0_IIC_SDA RS4 4.7K 3.3V
SFP0_IIC_SCL RS5 4.7K 3.3V
SFP0_RATE_SEL0 RS6 4.7K 3.3V
SFP0_RATE_SEL0 RS7 NC DGND
SFP0_MO_DETECT RS8 4.7K 3.3V
SFP0_RATE_SEL1 RS9 4.7K DGND
SFP0_RATE_SEL1 RS10 NC 3.3V
SFP0_LOS RS11 4.7K 3.3V
3.3V
ECS1
10uF/25V
CS1
0.1uF
DGND
VCCT
FBP1
BLM21P221SN
ECS2
10uF/25V
CS2
0.1uF
DGND
VCCR
FBP2
BLM21P221SN
ECS3
10uF/25V
CS3
0.1uF
DGND
JG1
MMCX
SMA_RX_P
DGND
JG3
MMCX
SMA_RX_N
DGND
JG2
MMCX
CMG3
0.1uF
SMA_TX_P
DGND
JG4
MMCX
CMG4
0.1uF
SMA_TX_N
DGND
U9
3.3V
DGND
CMOS_D0_1
CMOS_D1_1
ADC_D0
CMOS_D2_1
CMOS_D3_1
CMOS_D4_1
CMOS_D5_1
ADC_D1
CMOS_D6_1
CMOS_D7_1
CMOS_D8_1
CMOS_D9_1
CMOS_D10_1
CMOS_D11_1
CMOS_PCLK_1
CMOS_HS_1
ADC_D2
CMOS_VS_1
ADC_D3
ADC_D4
CMOS_I2C_SCL_1
ADC_D5
CMOS_I2C_SDA_1
CMOS_RST_1
ADC_D6
CMOS_TRG_1
CMOS_STROBE_1
BOARD_3x8
3.3V
ECS4
10uF/25V
CS4
0.1uF
DGND
ADC_D0
ADC_D1
ADC_D2
ADC_D3
ADC_D4
ADC_D5
ADC_D6
SFP0_RD_N
SFP0_RD_P
SFP0_TD_P
SFP0_TD_N
SFP0_TX_DISABLE
SFP0_IIC_SDA
SFP0_IIC_SCL
SFP0_LOS
SMA_RX_N
SMA_RX_P
SMA_TX_N
SMA_TX_P
CMOS_D0_1
CMOS_D1_1
CMOS_D2_1
CMOS_D3_1
CMOS_D4_1
CMOS_D5_1
CMOS_D6_1
CMOS_D7_1
CMOS_D8_1
CMOS_D9_1
CMOS_D10_1
CMOS_D11_1
CMOS_PCLK_1
CMOS_HS_1
CMOS_VS_1
CMOS_RST_1
CMOS_TRG_1
CMOS_STROBE_1
CMOS_I2C_SCL_1
CMOS_I2C_SDA_1
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V3BEST
eagleGT
Size
A4
Document Number
08 SFP
Rev
V2.0
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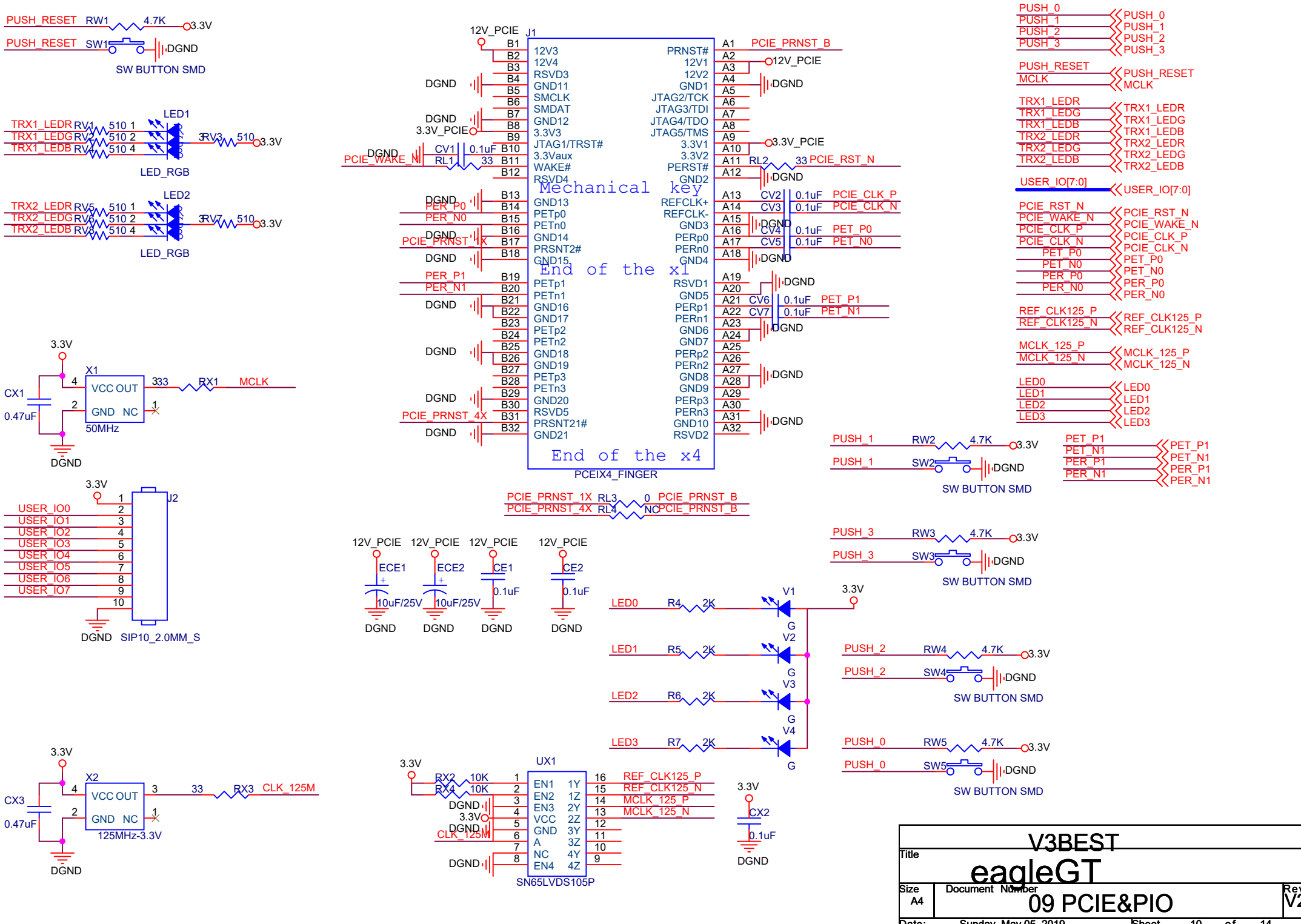
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PUSH_RESET SW1 DGND
SW BUTTON SMD
LED1
TRX1_LEDR RV1 510 1
TRX1_LEDG RV2 510 2
TRX1_LEDB RV4 510 4
RV3 510 3.3V
LED_RGB
LED2
TRX2_LEDR RV5 510 1
TRX2_LEDG RV6 510 2
TRX2_LEDB RV8 510 4
RV7 510 3.3V
LED_RGB
3.3V
X1
CX1
0.47uF
VCC OUT
GND NC
50MHz
333 RX1 MCLK
DGND
3.3V
J2
USER_IO0
USER_IO1
USER_IO2
USER_IO3
USER_IO4
USER_IO5
USER_IO6
USER_IO7
DGND SIP10_2.0MM_S
3.3V
X2
CX3
0.47uF
VCC OUT
GND NC
125MHz-3.3V
33 RX3 CLK_125M
DGND
12V_PCIE J1
DGND
3.3V_PCIE
PCIE_WAKE_N CV1 0.1uF RL1 33
PCIE_PRNST_1X
PCIE_PRNST_4X
PER_P0
PER_N0
PER_P1
PER_N1
12V3
12V4
RSVD3
GND11
SMCLK
SMDAT
GND12
3.3V3
JTAG1/TRST#
3.3Vaux
WAKE#
RSVD4
Mechanical key
GND13
PETp0
PETn0
GND14
PRSNT2#
GND15
End of the x1
PETp1
PETn1
GND16
GND17
PETp2
PETn2
GND18
GND19
PETp3
PETn3
GND20
RSVD5
PRSNT21#
GND21
End of the x4
PCEIX4_FINGER
PRNST#
12V1
12V2
GND1
JTAG2/TCK
JTAG3/TDI
JTAG4/TDO
JTAG5/TMS
3.3V1
3.3V2
PERST#
GND2
REFCLK+
REFCLK-
GND3
PERp0
PERn0
GND4
RSVD1
GND5
PERp1
PERn1
GND6
GND7
PERp2
PERn2
GND8
GND9
PERp3
PERn3
GND10
RSVD2
PCIE_PRSNT_B
12V_PCIE
3.3V_PCIE
PCIE_PRST_N RL2 33
CV2 0.1uF PCIE_CLK_P
CV3 0.1uF PCIE_CLK_N
CV4 0.1uF PET_P0
CV5 0.1uF PET_N0
CV6 0.1uF PET_P1
CV7 0.1uF PET_N1
PCIE_PRNST_1X RL3 0 PCIE_PRNST_B
PCIE_PRNST_4X RL4 NC PCIE_PRNST_B
12V_PCIE ECE1 10uF/25V
12V_PCIE ECE2 10uF/25V
12V_PCIE CE1 0.1uF
12V_PCIE CE2 0.1uF
DGND
LED0 R4 2K
LED1 R5 2K
LED2 R6 2K
LED3 R7 2K
V1
V2
V3
V4
G
3.3V
UX1
RX2 10K
RX4 10K
3.3V
CLK_125M
EN1 1Y
EN2 1Z
EN3 2Y
VCC 2Z
GND 3Y
A 3Z
NC 4Y
EN4 4Z
SN65LVDS105P
REF_CLK125_P
REF_CLK125_N
MCLK_125_P
MCLK_125_N
CX2
0.1uF
PUSH_1 RW2 4.7K 3.3V
PUSH_1 SW2 DGND
SW BUTTON SMD
PUSH_3 RW3 4.7K 3.3V
PUSH_3 SW3 DGND
SW BUTTON SMD
PUSH_2 RW4 4.7K 3.3V
PUSH_2 SW4 DGND
SW BUTTON SMD
PUSH_0 RW5 4.7K 3.3V
PUSH_0 SW5 DGND
SW BUTTON SMD
PUSH_0
PUSH_1
PUSH_2
PUSH_3
PUSH_RESET
MCLK
TRX1_LEDR
TRX1_LEDG
TRX1_LEDB
TRX2_LEDR
TRX2_LEDG
TRX2_LEDB
USER_IO[7:0]
PCIE_RST_N
PCIE_WAKE_N
PCIE_CLK_P
PCIE_CLK_N
PET_P0
PET_N0
PER_P0
PER_N0
REF_CLK125_P
REF_CLK125_N
MCLK_125_P
MCLK_125_N
LED0
LED1
LED2
LED3
PET_P1
PET_N1
PER_P1
PER_N1
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eagleGT
Size A4
Document Number
09 PCIE&PIO
Rev V2.0
Date: Sunday, May 05, 2019
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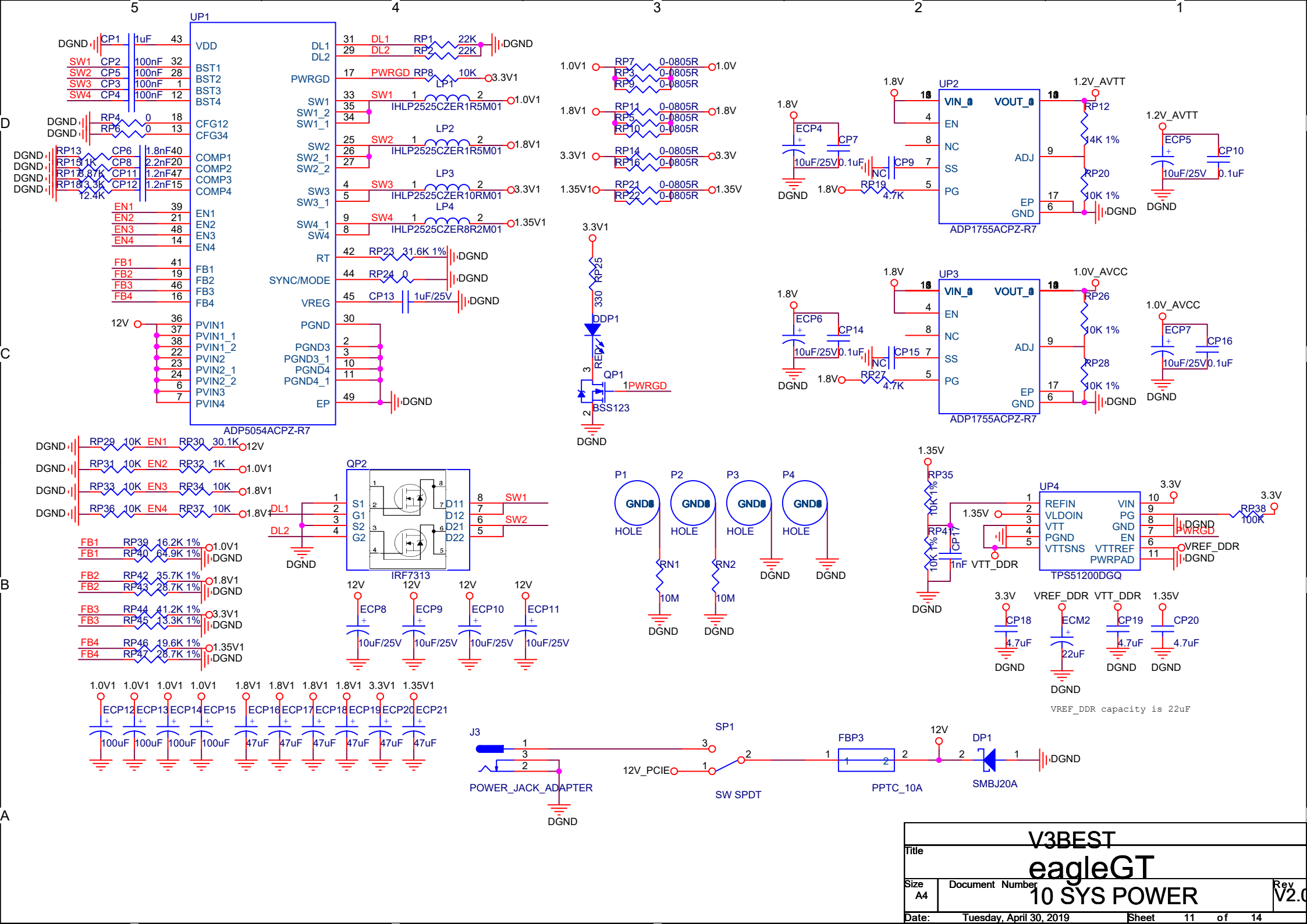
5
4
3
2
1
D
C
B
A
UP1
ADP5054ACPZ-R7
VDD
BST1
BST2
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BST4
CFG12
CFG34
COMP1
COMP2
COMP3
COMP4
EN1
EN2
EN3
EN4
FB1
FB2
FB3
FB4
PVIN1
PVIN1_1
PVIN1_2
PVIN2
PVIN2_1
PVIN2_2
PVIN3
PVIN4
DL1
DL2
PWRGD
SW1
SW1_2
SW1_1
SW2
SW2_1
SW2_2
SW3
SW3_1
SW4_1
SW4
RT
SYNC/MODE
VREG
PGND
PGND3
PGND3_1
PGND4
PGND4_1
EP
12V
DGND
1.0V1
1.8V1
3.3V1
1.35V1
1.8V
3.3V
1.2V_AVTT
1.0V_AVCC
UP2
UP3
ADP1755ACPZ-R7
VIN_1
VIN_2
VOUT_1
VOUT_2
EN
NC
SS
PG
ADJ
EP
GND
DDP1
QP1
BSS123
1PWRGD
QP2
IRF7313
S1
G1
S2
G2
D11
D12
D21
D22
P1
P2
P3
P4
HOLE
GND
RN1
RN2
10M
UP4
TPS51200DGQ
REFIN
VLDOIN
VTT
PGND
VTTSNS
VIN
PG
GND
EN
VTTREF
PWRPAD
VTT_DDR
VREF_DDR
PWRGD
VREF_DDR capacity is 22uF
J3
POWER_JACK_ADAPTER
SP1
SW SPDT
12V_PCIE
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ECP21
ECM2
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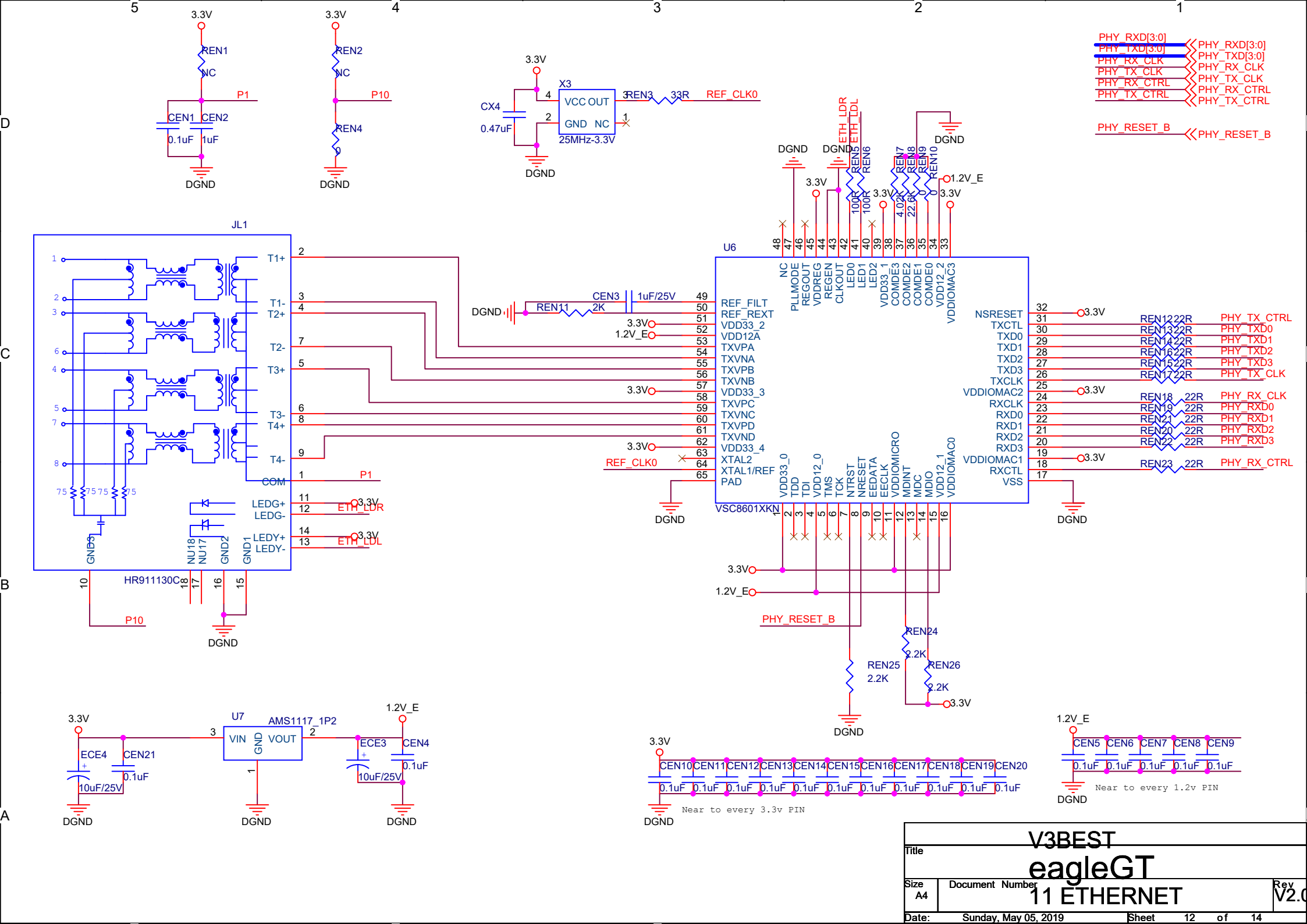

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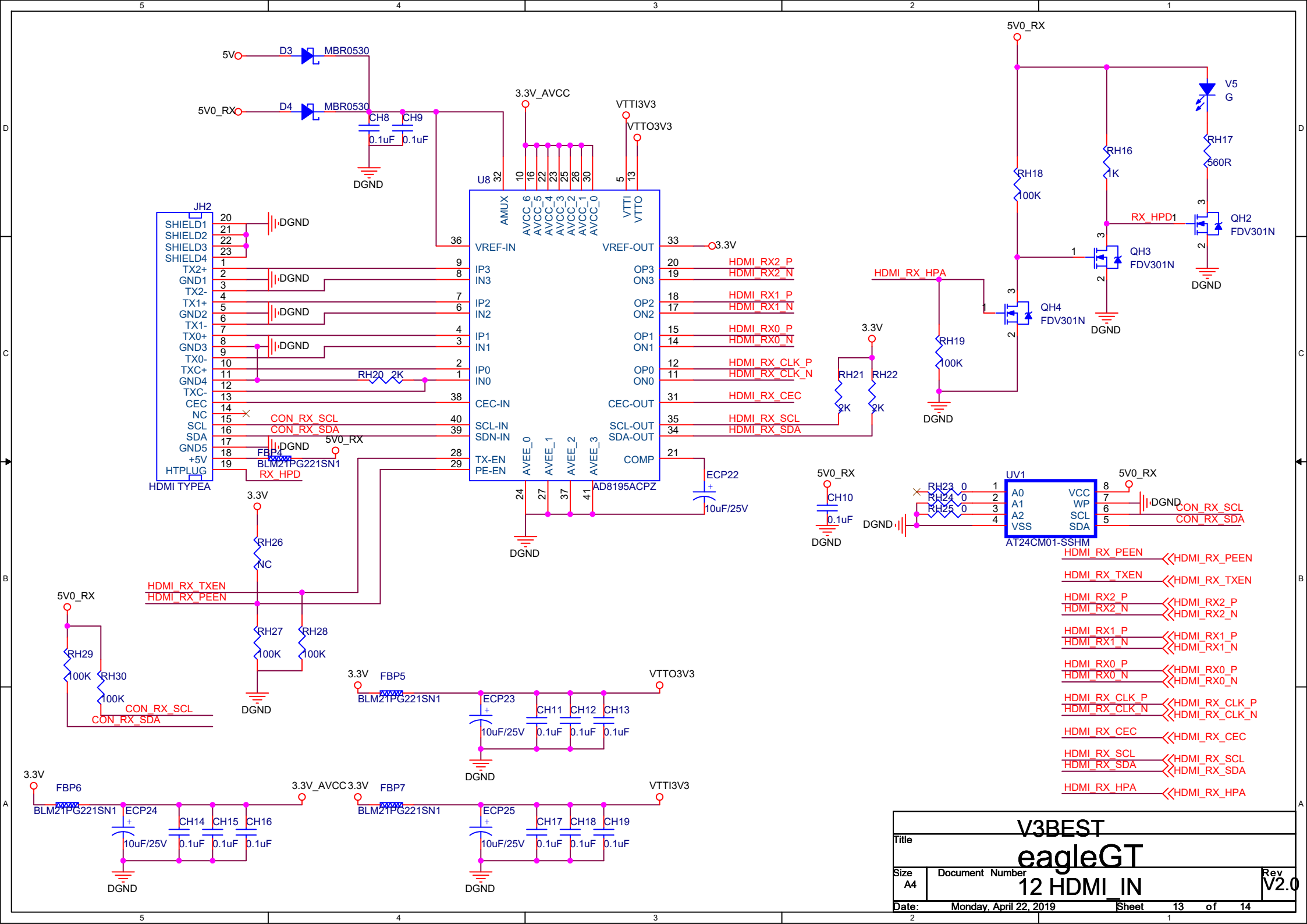

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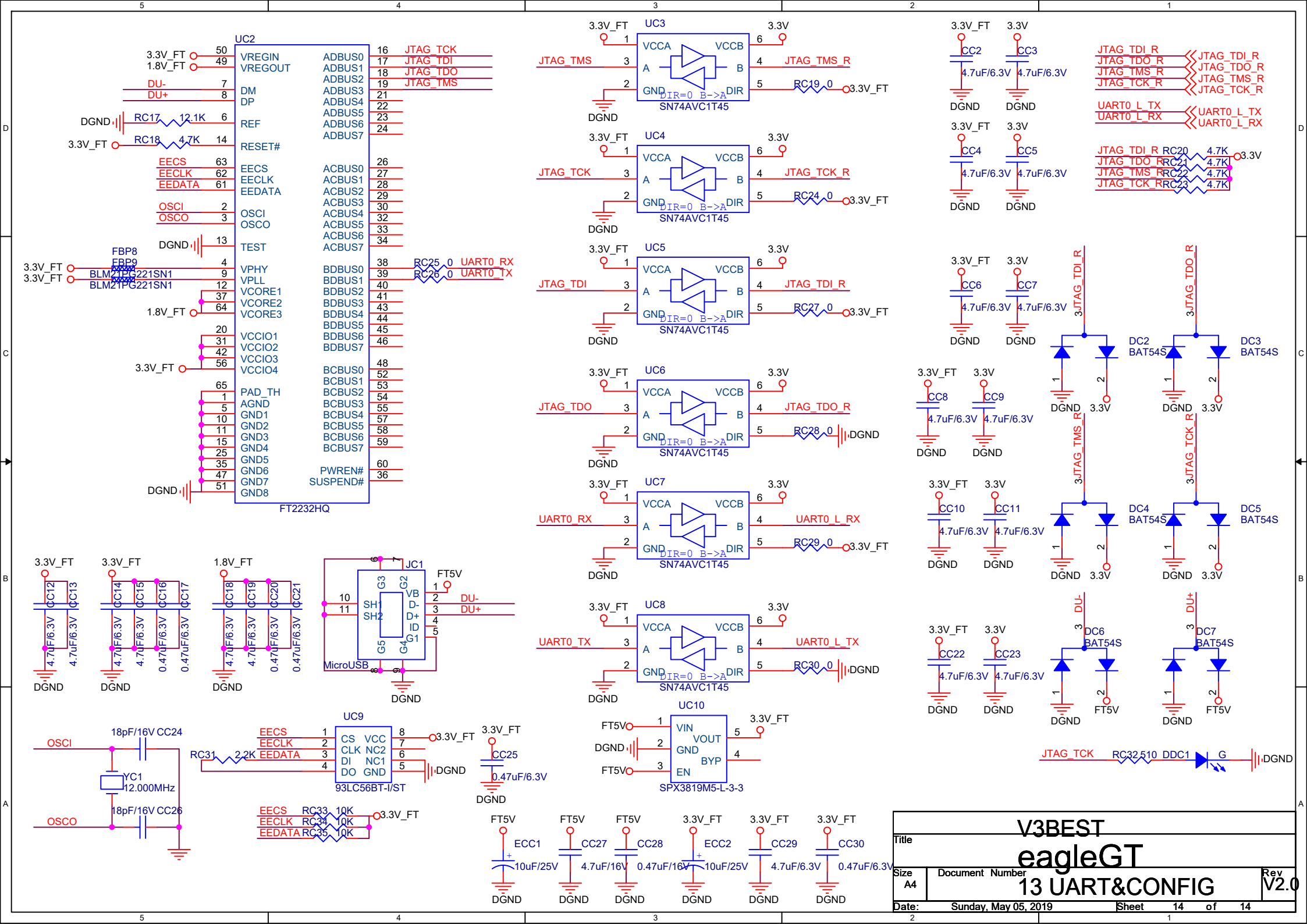

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