



Barefoot Technology Intro

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The Barefoot Solution

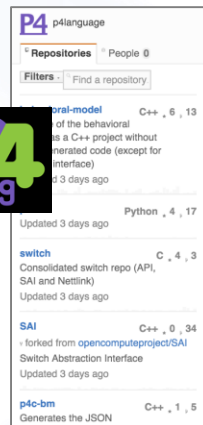
New Open Source Ecosystem



Barefoot Software



Barefoot Hardware

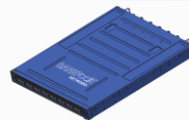
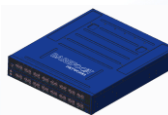


New Network Functions

Differentiation

Network Analytics

Rapid Innovation

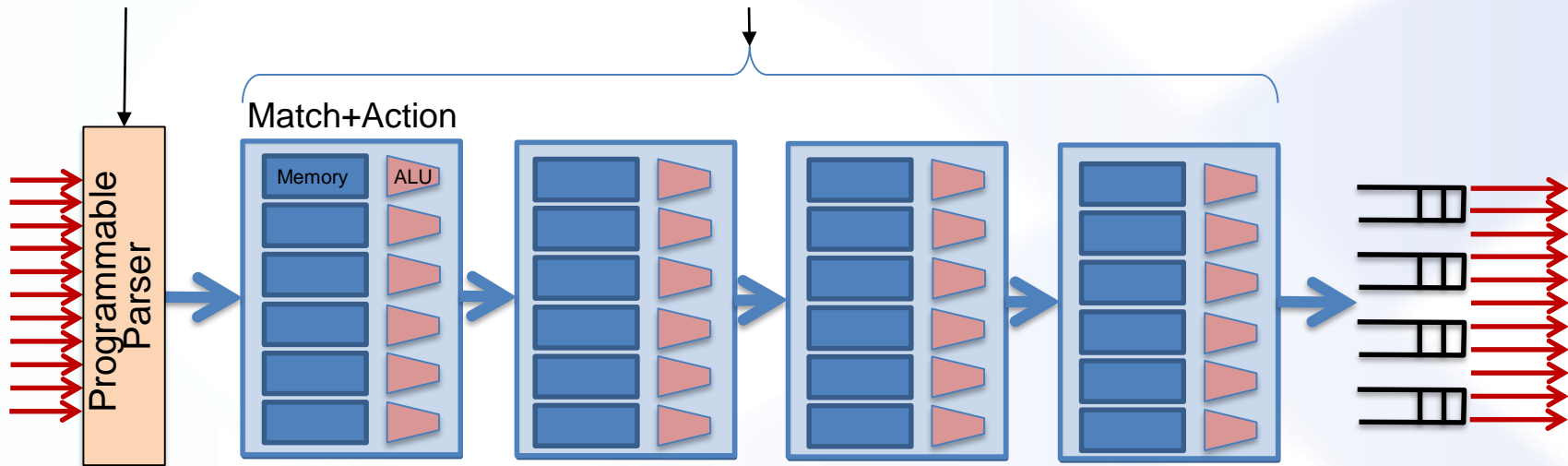


“Programmability without Compromise”

PISA: Protocol Independent Switch Architecture

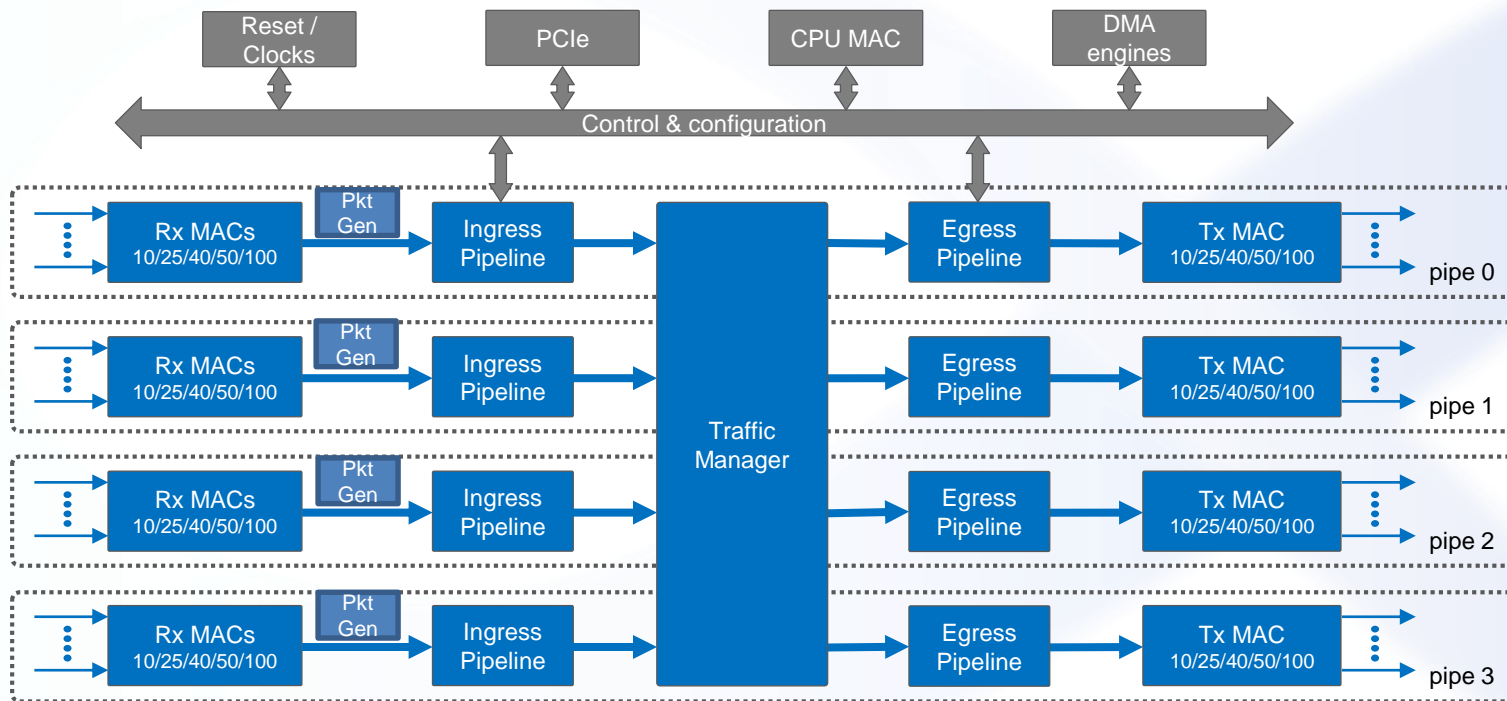
Programmer declares which headers are recognized

Programmer declares what tables are needed and how packets are processed



All stages are identical – makes PISA a good “compiler target”

Barefoot Tofino™ - 6.5T Tofino Block Diagram



**Each pipe has 16x100G MACs
Packet Generator, CPU**

Barefoot Tofino™ family

6.5Tb/s



260 x 25G SerDes

example port configurations:

- 65 x 100GE/40GE
- 130 x 50GE/(40GE via gearbox)
- 260 x 25GE/10GE

3.3Tb/s



132 x 25G SerDes

example port configurations:

- 33 x 100GE/40GE
- 66 x 50GE (40GE via gearbox)
- 132 x 25GE/10GE

2.5Tb/s



100 x 25G SerDes

example port configuration:

- 48 x 25GE / 10GE + 13 x 100GE / 40GE

1.9Tb/s



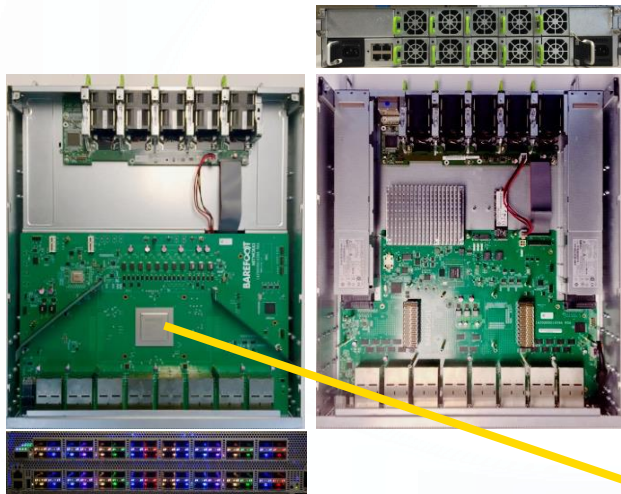
96 x 10G SerDes + 36 x 25G SerDes or 76 x 25G SerDes

example port configurations:

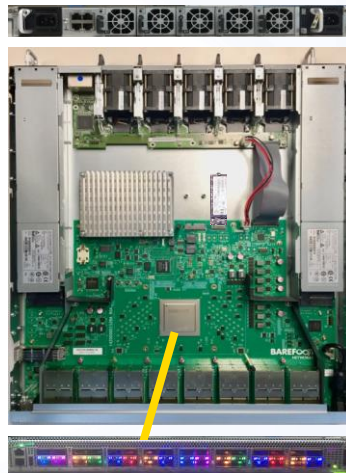
- 96 x 10GE/24 x 40GE + 9 x 100GE / 40GE
- 48 x 25GE / 10GE + 7 x 100GE / 40GE

Programmability without compromises

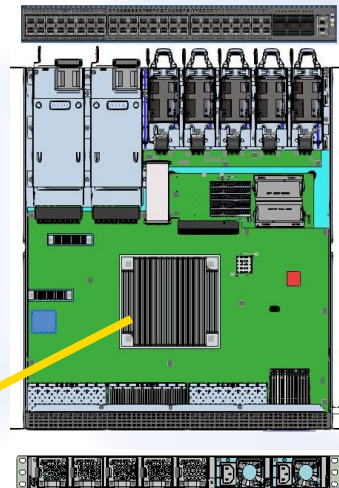
Wedge100BF-65X (AS7616-65X)



Wedge100BF-32X (AS7616-32X)



OSW 1800

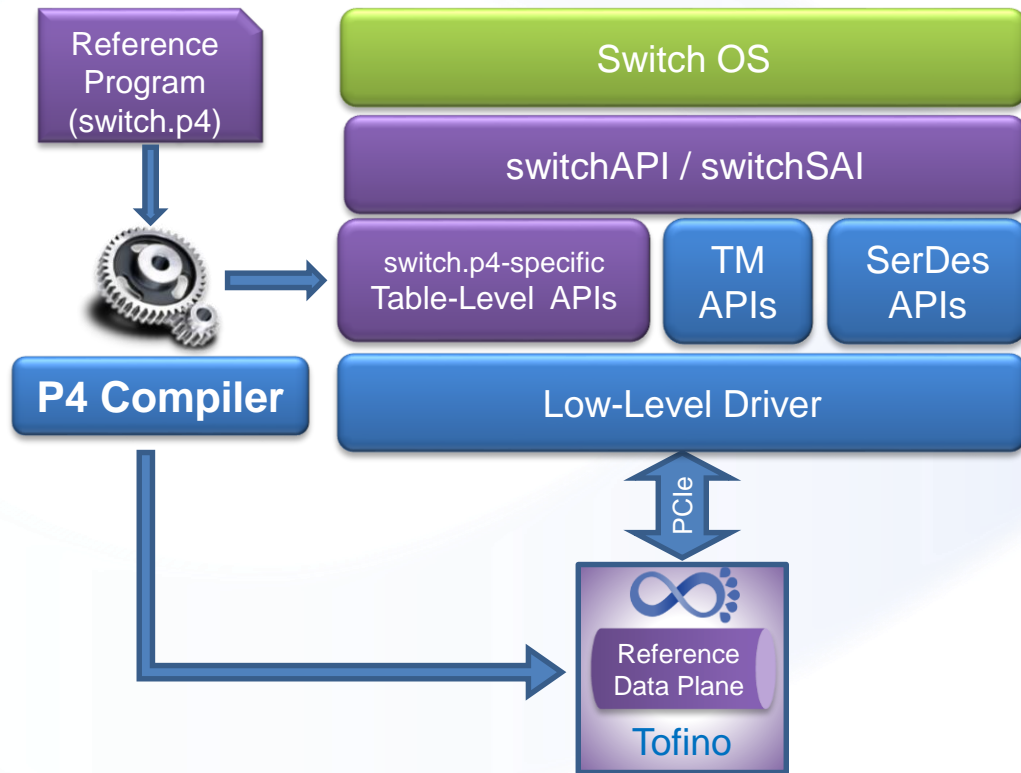


Tofino™ ASIC

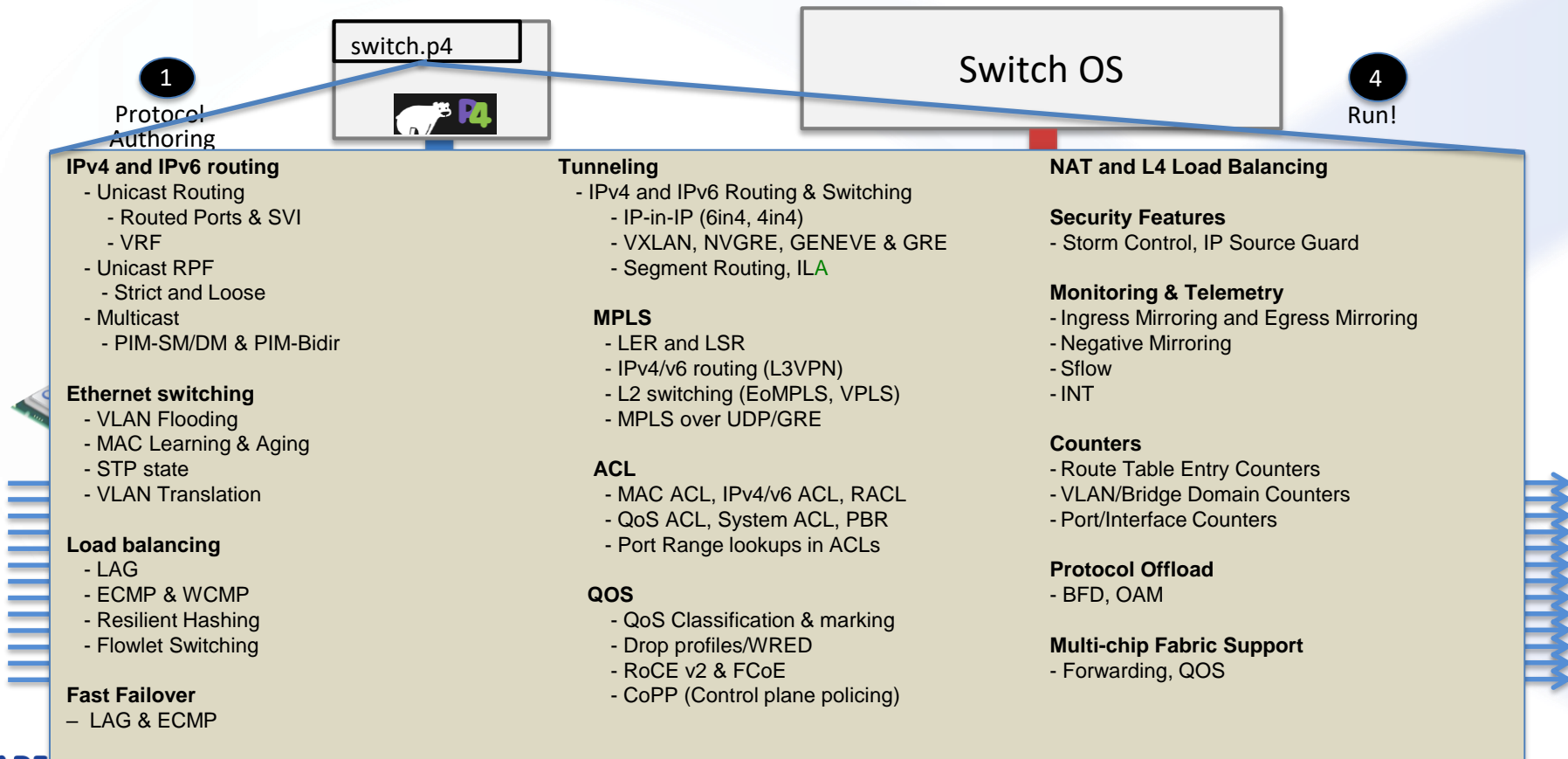
**same power, same cost, same or better performance
of a fixed-function switch chip**

more P4 Tofino
platforms
to come in 2017

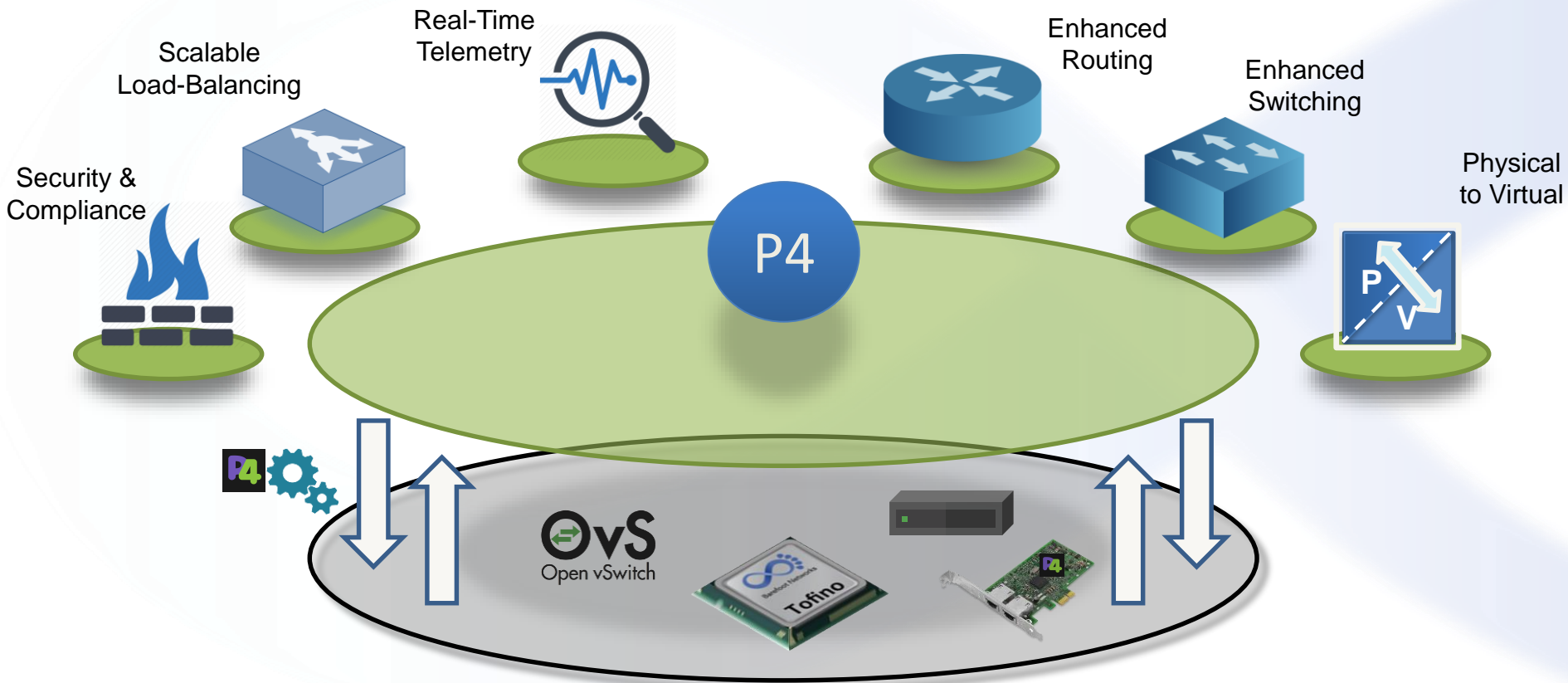
Barefoot and Switch OS Integration Model



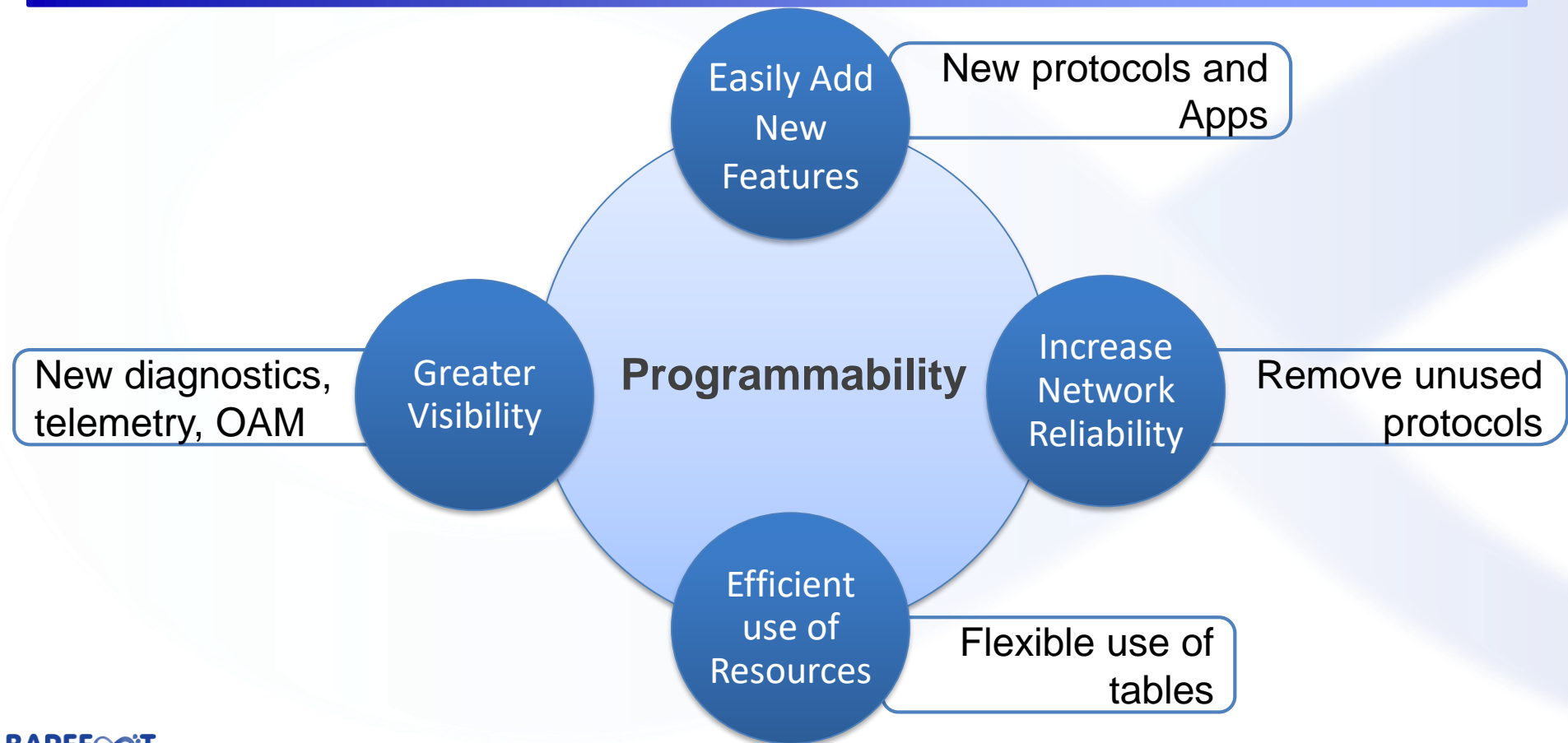
switch.p4 & switchAPI Features



Programmability with P4 Advanced Apps



Benefits of a Programmable Forwarding Plane



Thank you

