Parallel Heuristic Placement and Routing Algorithm for Optimizing Logical Clarity of Schematics (Supplementary Materials)

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I. Time Complexity of the Algorithm

Let the number of components on the netlist be D, the number of single wires be S, and the number of merged bus lines be C. The parameter a represents the average proportion of components connected to other components $(0 < a \leq 1)$.

In the preliminary layout of topological sorting phase, the algorithm performs an initial layout using topological sorting, with a time complexity of $O(D + S)$ [1].

Parallel bidirectional value propagation placement optimization within column employs a parallel bidirectional value propagation algorithm to optimize the intra-column layout. When the components are evenly distributed across all columns, each column contains approximately $\sqrt{D}$ components. The time complexity for calculating the bubble values of different components is $O(\frac{D \times a \times D}{Pr}) = O(\frac{aD^2}{Pr})$, while the time complexity for sorting the bubble values is $O(D \log \sqrt{D})$. The reallocation of bubble values takes $O(D)$ time. When the component connectivity is relatively simple (i.e., a is large), the computation of different component bubble values becomes the primary time-consuming step. Therefore, the time complexity of the parallel bidirectional value propagation algorithm is $O(max\{\frac{aD^2}{Pr}, D \log \sqrt{D}\})$.

In the parallel dynamic programming of column stretching and leaving blank phase, a parallel dynamic programming algorithm is used for intra-column whitespace expansion. Assuming the components are evenly distributed across all columns, each column contains approximately $\sqrt{D}$ components, and there are approximately $\sqrt{D}$ columns. The time complexity of this step is approximately $O(\sqrt{D} \times (\frac{\sqrt{D}}{Pr} \times \sqrt{D}) \times \frac{a \times D}{vecLen}) = O(\frac{aD^{\frac{5}{2}}}{Pr \times vecLen})$.

The fourth step involves determining the geometric positions of the components, with a time complexity of approximately $O(D + S)$ [1].

In the parallel routing phase. Apart from the wire routing phase, the most time-consuming part is the heuristic column gap compression, which has a time complexity of $O(\sqrt{D} \times C \log C)$ [1]. The wire routing phase is also time-consuming due to the consideration of overlap avoidance when routing horizontal lines from each port connected to the wire [1], with a time complexity of $O(\frac{C}{Pr} \times \sqrt{D} \times \sqrt{D}) = O(\frac{D \times C}{Pr})$. Thus, the time complexity of the parallel routing algorithm is $O(\sqrt{D} \times C \times max\{\frac{\sqrt{D}}{Pr}, \log C\})$.

In summary, the total time complexity of the algorithm can be represented as $O(max\{\frac{aD^2}{Pr}, D \log \sqrt{D}, \frac{aD^{\frac{5}{2}}}{Pr \times vecLen}, \sqrt{D} \times C \log C, \frac{D \times C}{Pr}, D + S\})$, and simplified as $O(max\{D \log \sqrt{D}, \frac{aD^{\frac{5}{2}}}{Pr \times vecLen}, \sqrt{D} \times C \log C, \frac{D \times C}{Pr}\})$.

References

[1] Xingyu Cui, Zhaopeng Feng, Yanfeng Ding, Hui Sun, Zhiliang Li, Zhenrong Li, Xiaoguang Liu, Gang Wang, Heuristic Placement and Routing Algorithm for Optimizing Logical Clarity of Schematics, National Conference of Theoretical Computer Science 2023, unpublished.