Work Log

Date	Task	Who
02/22/2022	Working out design	Syed, Brendan, Sam
02/23/2022	Working out design	Yiwei, Wonjin, Syed, Brendan, Sam
02/24/2022	Draft of the diagram	Brendan, Syed
02/26/2022	Final draft of the system design document	Yiwei, Wonjin, Syed, Brendan, Sam
02/28/2022	Start working on Verilog	Yiwei
03/01/2022	Working on Addition/Subtraction	Yiwei, Wonjin, Syed, Brendan, Sam
03/02/2022	Working on Multiplication/Division	Yiwei, Wonjin, Syed, Brendan, Sam
03/04/2022	Draft for the whole program	Yiwei, Wonjin, Syed, Brendan, Sam
03/06/2022	Code matched with System Design	Yiwei, Wonjin, Syed, Brendan, Sam