

## Work Log

Date	Task	Who
04/11/2022	Update System Design Description	Syed, Brendan, Sam
04/13/2022	Starting working on Verilog code	Yiwei, Wonjin, Syed, Brendan, Sam
04/18/2022	Debug	Yiwei, Wonjin, Syed, Brendan, Sam
04/20/2022	Finish the code	Yiwei, Wonjin, Syed, Brendan, Sam
04/22/2022	Double check and submit	Yiwei, Wonjin, Syed, Brendan, Sam