

System Design

2.2.2 System Design Description

2.2.2.1 List of Inputs

- “inputA” - 16-bit integer number to be operated on
- “opcode” - 4-bit operational code
- “clk” - 1-bit clock signal

2.2.2.2 List of Outputs

- “outputC” - 32-bit integer result from the performed mathematical operation
- “error” - 2-bit error code

2.2.2.3 List of Interfaces

- “outputADD” - Adder-subtractor module-to-multiplexor for addition
 - 32-bit wire bus that connects the adder-subtractor modules’ output to 1 out of 16 of the multiplexor’s 32-bit channels.
- “outputSUB” - Adder-subtractor module-to-multiplexor for subtraction
 - 32-bit wire bus that connects the adder-subtractor modules’ output to 1 out of 16 of the multiplexor’s 32-bit channels.
- “outputMUL” - Multiplication module-to-multiplexor
 - 32-bit wire bus that connects the multiplication modules’ output to 1 out of 16 of the multiplexor’s 32-bit channels.
- “outputDIV” - Division module-to-multiplexor
 - 32-bit wire bus that connects the division modules’ output to 1 out of 16 of the multiplexor’s 32-bit channels.
- “outputMOD” - Modulo module-to-multiplexor
 - 32-bit wire bus that connects the modulo modules’ output to 1 out of 16 of the multiplexor’s 32-bit channels.
- “select” - Decoder-to-multiplexor channel select
 - 16-bit wire bus that connects the decoder’s output to the multiplexor’s one-hot channel select.
- “outputMUX” - Multiplexor-to-memory register
 - 32-bit wire bus that connects the multiplexor’s output to the memory register’s input.
- “feedback” - The lower 16 bits from the output feeding back into the second input of the circuit
- “outputAND” - 32-bit padded AND result connected to the multiplexor

- “outputNAND” - 32-bit padded NAND result connected to the multiplexor
- “outputNOR” - 32-bit padded NOR result connected to the multiplexor
- “outputNOT” - 32-bit padded NOT result connected to the multiplexor
- “outputOR” - 32-bit padded OR result connected to the multiplexor
- “outputXNOR” - 32-bit padded XNOR result connected to the multiplexor
- “outputXOR” - 32-bit padded XOR result connected to the multiplexor

2.2.2.4 List of Parts

- “addsub” - Adder-subtractor module
 - Adds or subtracts two 16-bit integers and returns a 32-bit integer and a 2-bit error code. Overflow will set the least significant bit of the error code to 1. Uses structured code.
- “mul” - Multiplier module
 - Multiplies two 16-bit integers and returns a 32-bit integer and a 2-bit error code. Uses structured code.
- “div” - Division module
 - Divides two 16-bit integers and returns a 32-bit integer and a 2-bit error code. Divide-by-zero will set the most significant bit of the error code to 1. Uses behavioral code.
- “mod” - Modulo module
 - Performs modulo on two 16-bit integers and returns a 32-bit integer and a 2-bit error code. Uses behavioral code.
- “mux” - Multiplexor module
 - Takes 16 32-bit values as input and returns 1 of them based on a 16-bit decoded one-hot value.
- “decoder” - Decoder module
 - Takes the 4-bit operational code as input and returns a 16-bit one-hot value to the multiplexor’s channel select.
- “AND” - AND module
 - Performs 16-bit by 16-bit AND and pads the result to 32 bits
- “NAND” - NAND module
 - Performs 16-bit by 16-bit NAND and pads the result to 32 bits
- “NOR” - NOR module
 - Performs 16-bit by 16-bit NOR and pads the result to 32 bits
- “NOT” - NOT module
 - Performs 16-bit NOT and pads the result to 32 bits
- “OR” - OR module
 - Performs 16-bit by 16-bit OR and pads the result to 32 bits
- “XNOR” - XNOR module
 - Performs 16-bit by 16-bit XNOR and pads the result to 32 bits

- “XOR” - XOR module
 - Performs 16-bit by 16-bit XOR and pads the result to 32 bits
- “dff” - D Flip-flop module given by the professor
 - 32-bit register storing the result of the circuit in which its lower 16 bits are used as the second input for the circuit’s next operation

2.2.2.5 Top-Level Circuit Diagram

