Work Log

Date	Task	Who
03/08/2022	Update System Design Description	Syed, Brendan, Sam
03/10/2022	Update logic from part 1	Yiwei, Sam
03/13/2022	Update Top-level Circuit Diagram/State Machine	Brendan, Syed, Wonjin
03/22/2022	Continue the state machine	Yiwei, Wonjin, Syed, Brendan, Sam
03/23/2022	Finish the state machine	Yiwei, Sam, Wonjin, Syed, Brendan
03/23/2022	Starting working on Verilog code	Yiwei, Wonjin, Syed, Brendan, Sam
03/28/2022	Debug	Yiwei, Wonjin, Syed, Brendan, Sam
03/31/2022	Finish the code	Yiwei, Wonjin, Syed, Brendan, Sam
04/01/2022	Double check the matchup of all the diagram with the code	Yiwei, Wonjin, Syed, Brendan, Sam