Protocol Laboratory Digital Engineering #2

Hochschule Rhein-Waal

Rhine-Waal University of Applied Sciences

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Course name:	Laboratory Digital Engineering	
Group:	A	
Faculty:	Communication and Environment	
Deadline:	24.02.2019	
Semester:	WS 2018/19	
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Study Questions

Question #1 – What is linear regulator (7805)?

An electrical component used to maintain a steady voltage.

Question #2 – Is it possible to connect an LED directly to 5V?

No, an LED in this lab can only handle 3V maximum.

Question #3 – What kind of resistor is used to connect an LED to 5V? How can it be calculated?

At least 100 Ohm resistor.

LED can handle 3V, input is 5V. So, we need a resistor to drop 2V.

R = V / I = 2V / 20mA = 100 Ohm.

Question #4 – What is the electrical representation (voltage) of a logical LOW and a logical HIGH?

LOW means voltage connects to ground. HIGH means voltage connects to Vcc (Voltage common collector / Voltage input).

Question #5 – What kind of plastic packages are available for ICs?

PDIP/DIP Plastic Dual-Inline Package. SOIC Small Outline Integrated Circuit.

Question #6 – What is the indication of pin #1 of an IC?

There are multiple indications and depends on the IC, most common ones are:

If there is a small circle in a corner on top of the IC:

Pin #1 is the pin on the most far lower left and closest to the circle.

If there is a half-circle on top of the IC:

Orient the IC so that the half-circle is on your left-hand-side.

Pin #1 is the pin on the most far lower left of a half circle.

If the previous two indicators are not available:

Pin #1 is the pin on the most far lower left according to the orientation of the text printed on top of the IC.

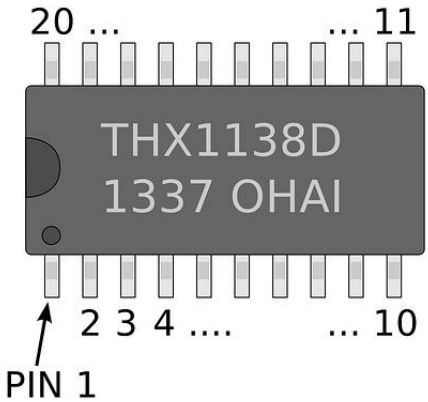


Figure 1: Examples on how to find pin #1.

Source: https://www.evilmadscientist.com/2010/basics-finding-pin-1/

Question #7 – What is the function of pin #7 and pin #14 of the majority of the 74xxxseries?

Pin #7 is connected to Ground, Pin #14 is connected to Vcc (Voltage common collector / Voltage input).

Question #8 – Where do you find detailed information about pin-out, supply and

logical voltages? Search the internet for the ICs used in this lab.

We found information about the ICs through the online shop of Texas Instruments where they include a detailed datasheet for each product and can be seen for free.

Question #9 – What are the standard logic levels for the ICs used in this lab.

AND, OR, NAND, NOR, XOR, XNOR.

Question #10 – What is “bouncing of a switch”?

When a switch is pressed it is making contact, but then it will bounce up (due to physical collision) which breaks contact, then the switch comes down and make contact again, and the cycle repeats until it stops completely. All of this happened roughly in a millisecond. This results in registering many inputs with 1 press.

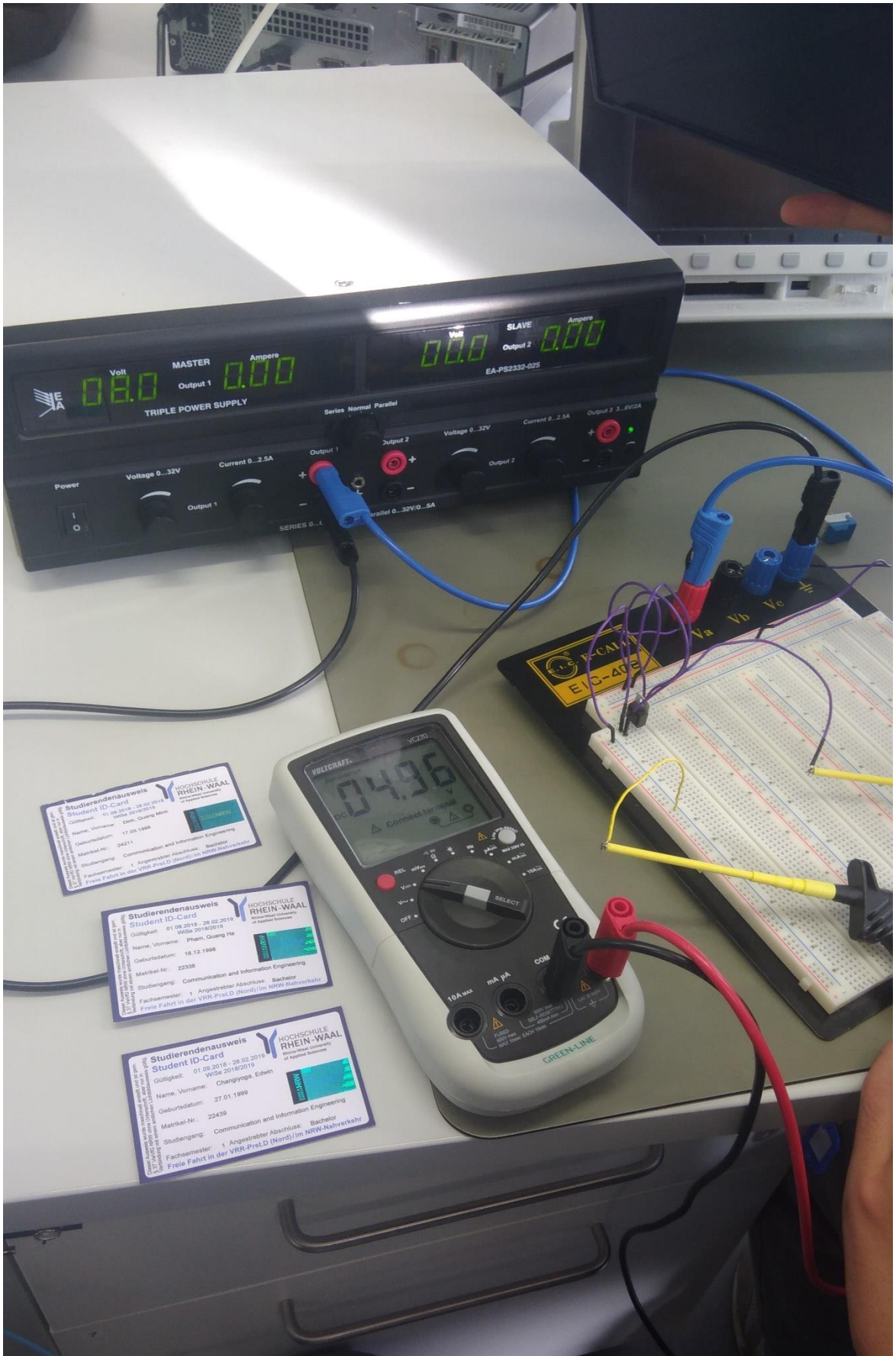
We like to imagine “bouncing of a switch” similar to a basketball bouncing in real life. Through this real-life example, we are able to understand the concept of a bouncing switch much better.

Challenge #1

Abstract:

Our group managed to follow the steps given in the Description and completed the challenge without anything special to report.

Pictures:



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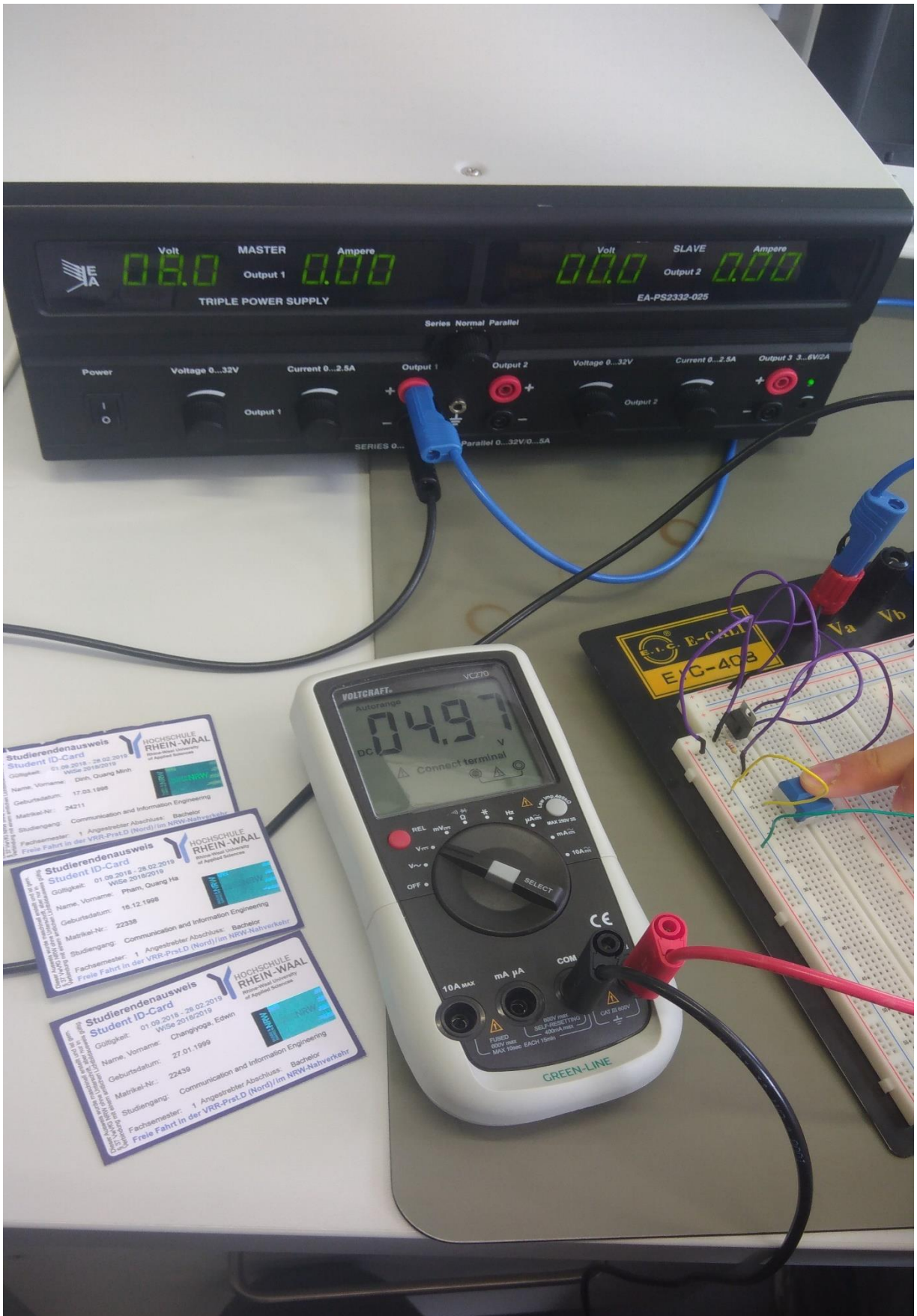

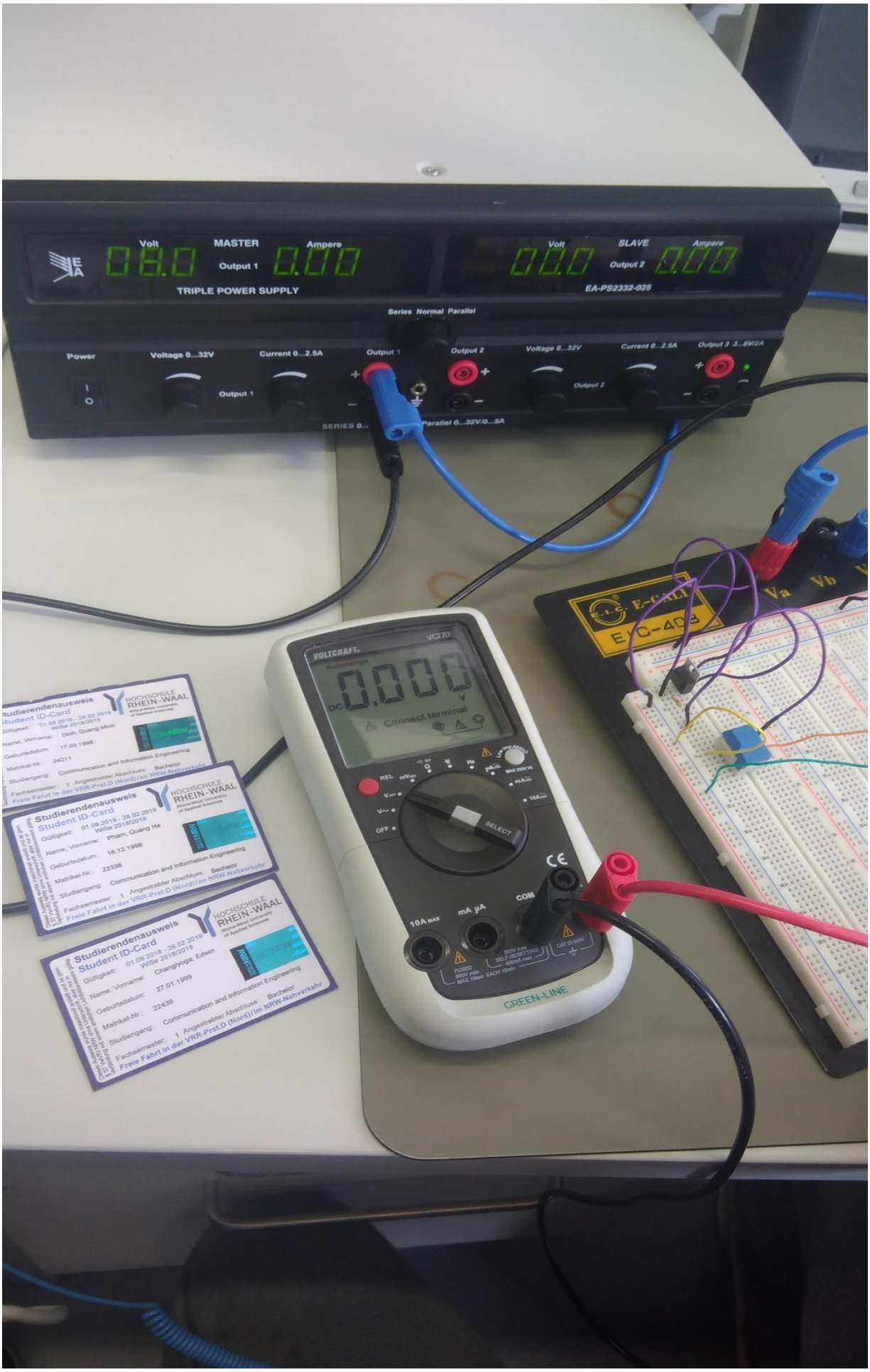
Volt
MASTER
Ampere
Output 1
TRIPLE POWER SUPPLY
SLAVE
Output 2
EA-PS2332-025
Series Normal Parallel
Power
Voltage 0...32V
Current 0...2.5A
Output 1
Output 2
Output 3 3...6V/2A
VOLTCRAFT
VC270
Autorange
Connect terminal
SELECT
COM
10A MAX
mA µA
GREEN-LINE
E-CALI
EYC-403
Va
Vb
Studierendenausweis
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HOCHSCHULE RHEIN-WAAL
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Result:

State of Switch	Voltage of DIGITALOUTPUT [V]
Not pressed	0
Pressed	4.97

Challenge #3

Abstract:

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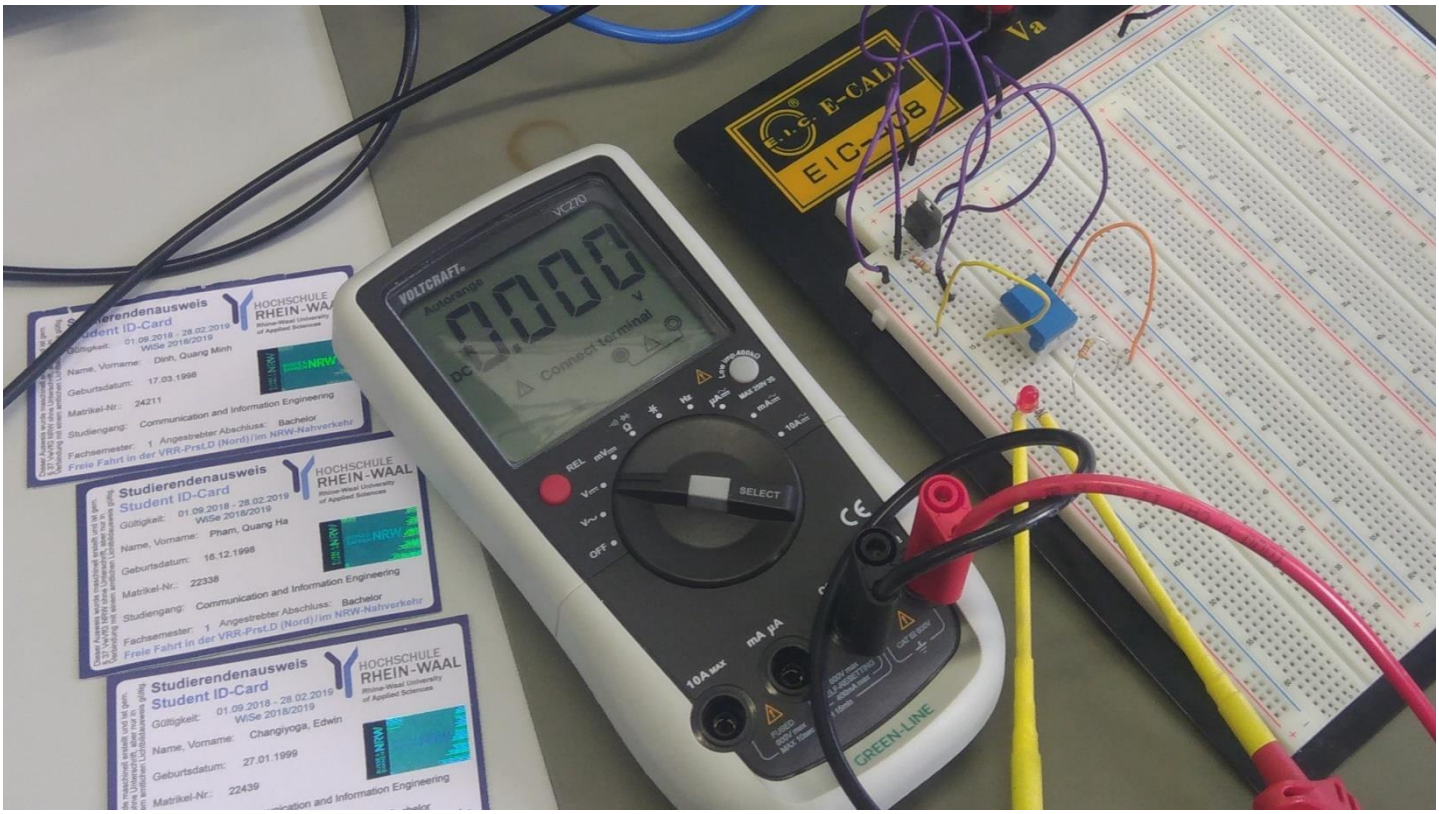

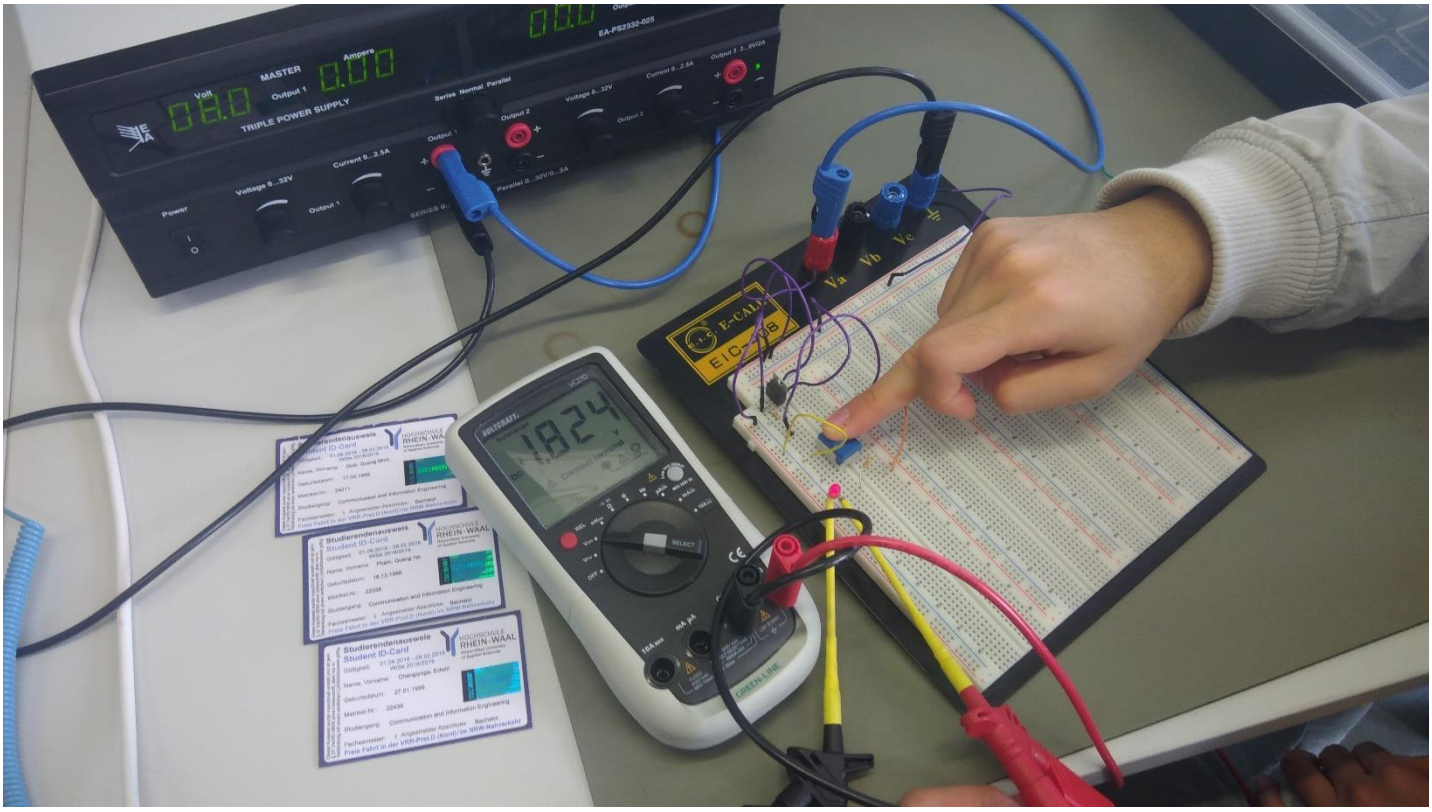

Result:

DIGITALINPUT connected to	LED [on/off]
GND	Off
5V	On

Challenge #4

Abstract:

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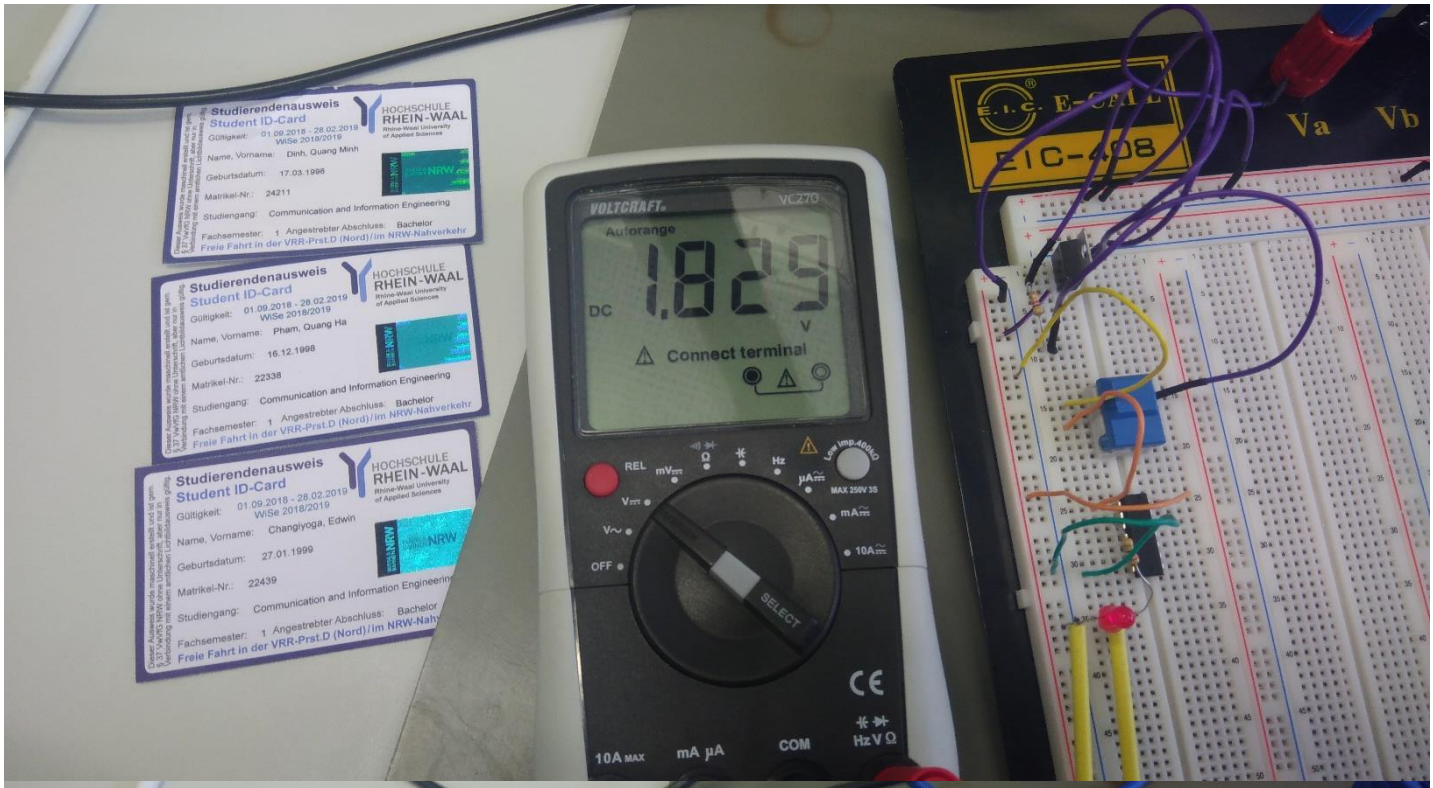

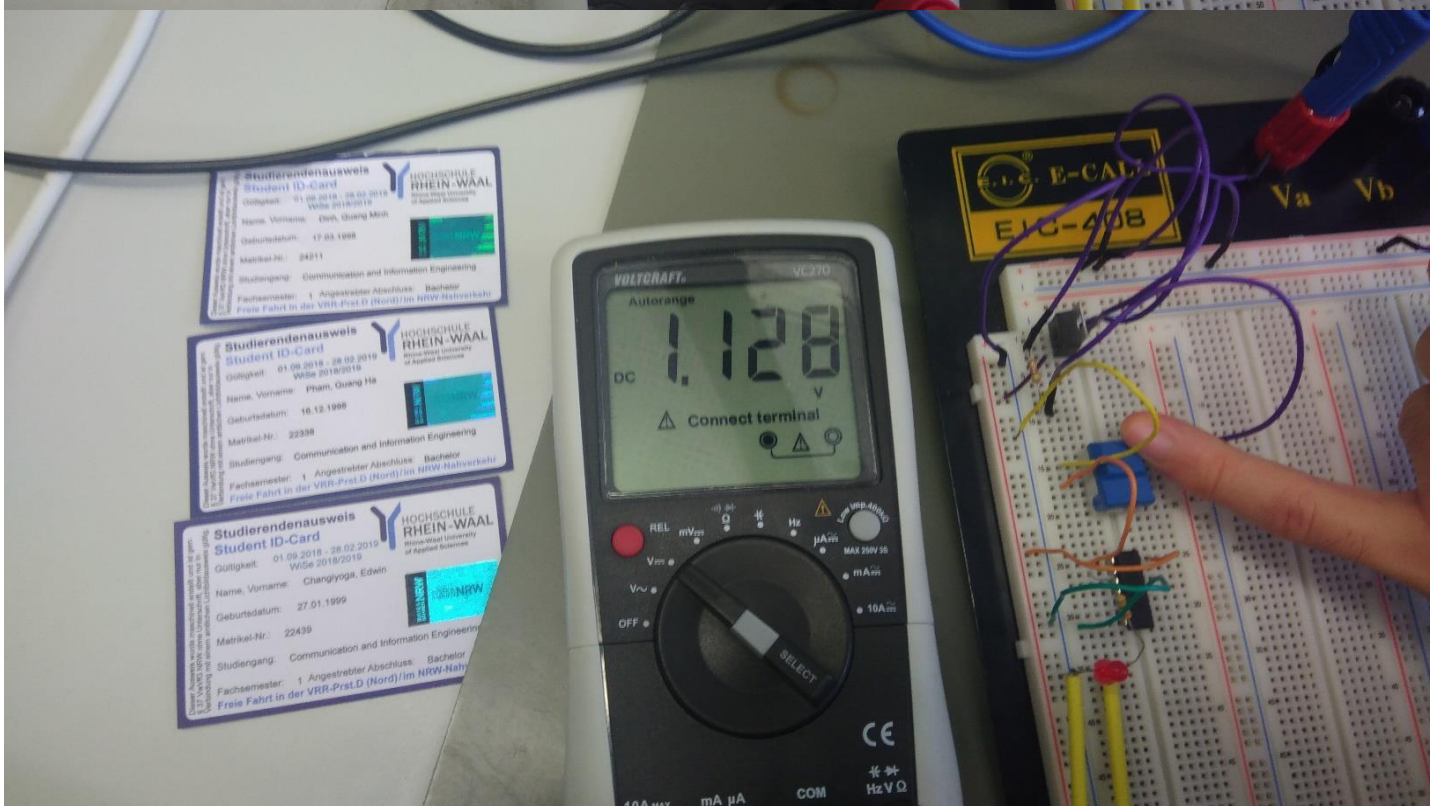

Result:

State of switch	LED on/off
Not pressed	On
Pressed	Off

INPUT	OUTPUT
0	1
1	0

Challenge #5

Abstract:

Our group managed to follow the steps given in the Description and completed the challenge without anything special to report.

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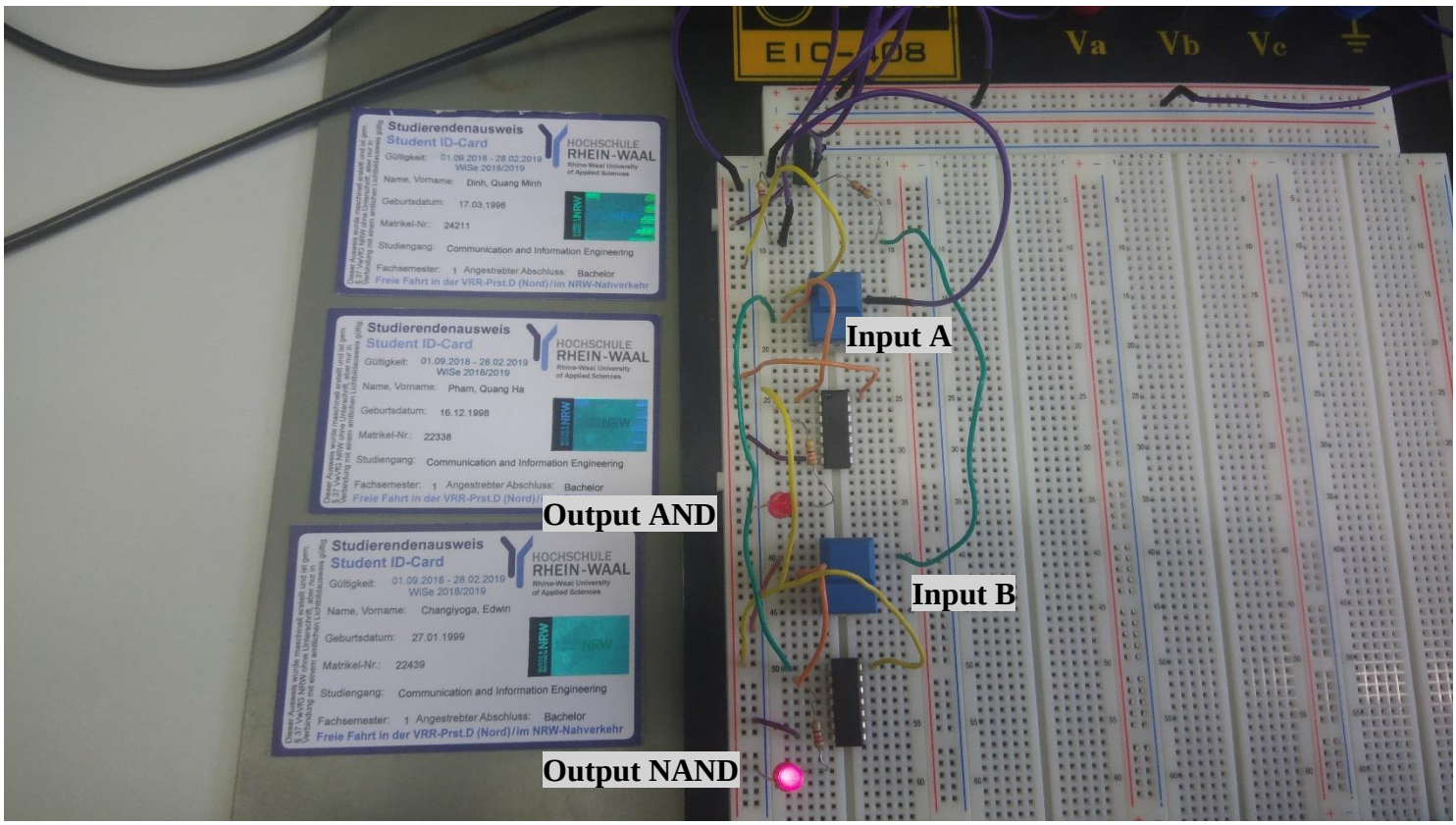

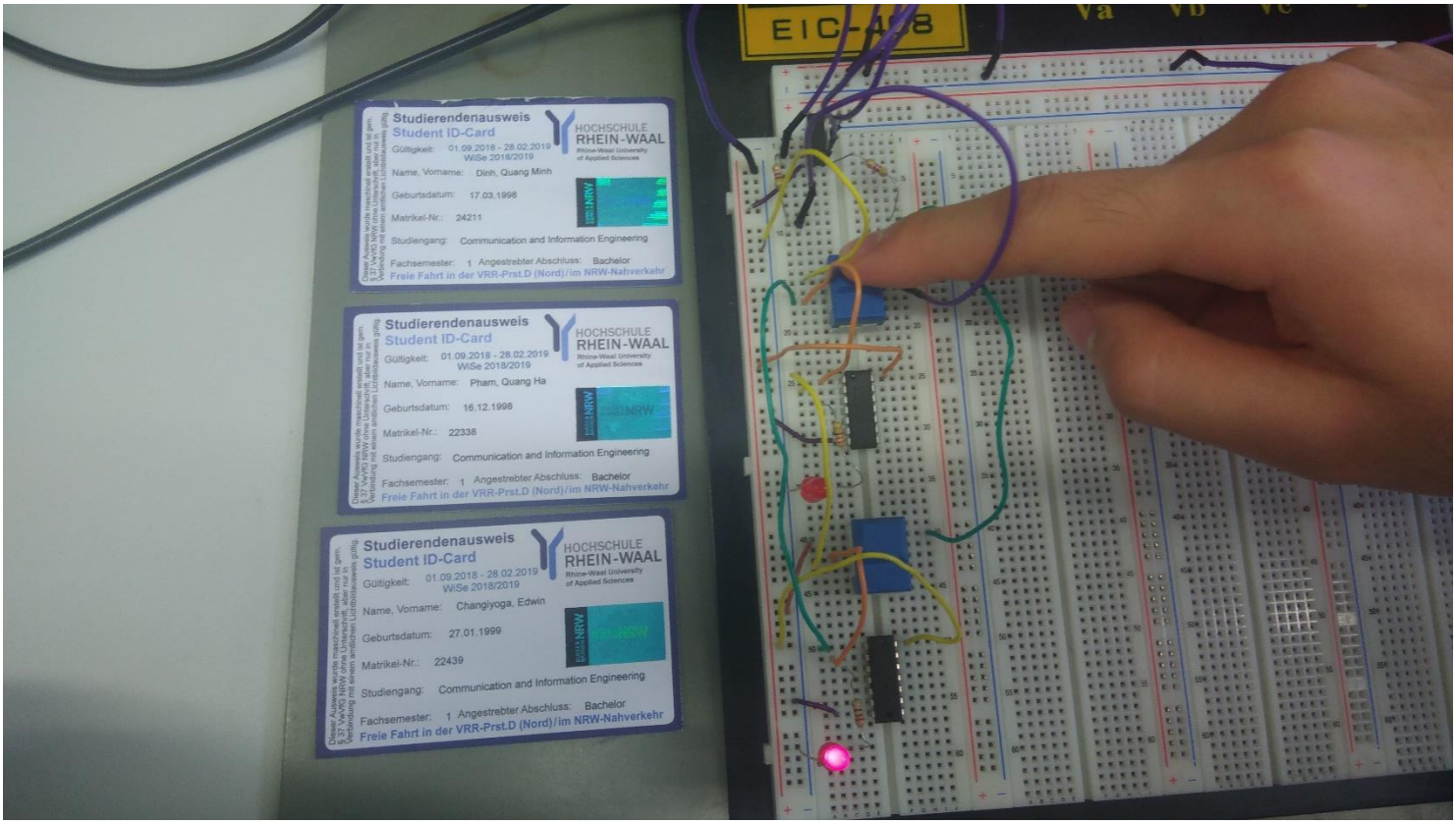
EIC-408
Va
Vb
Vc
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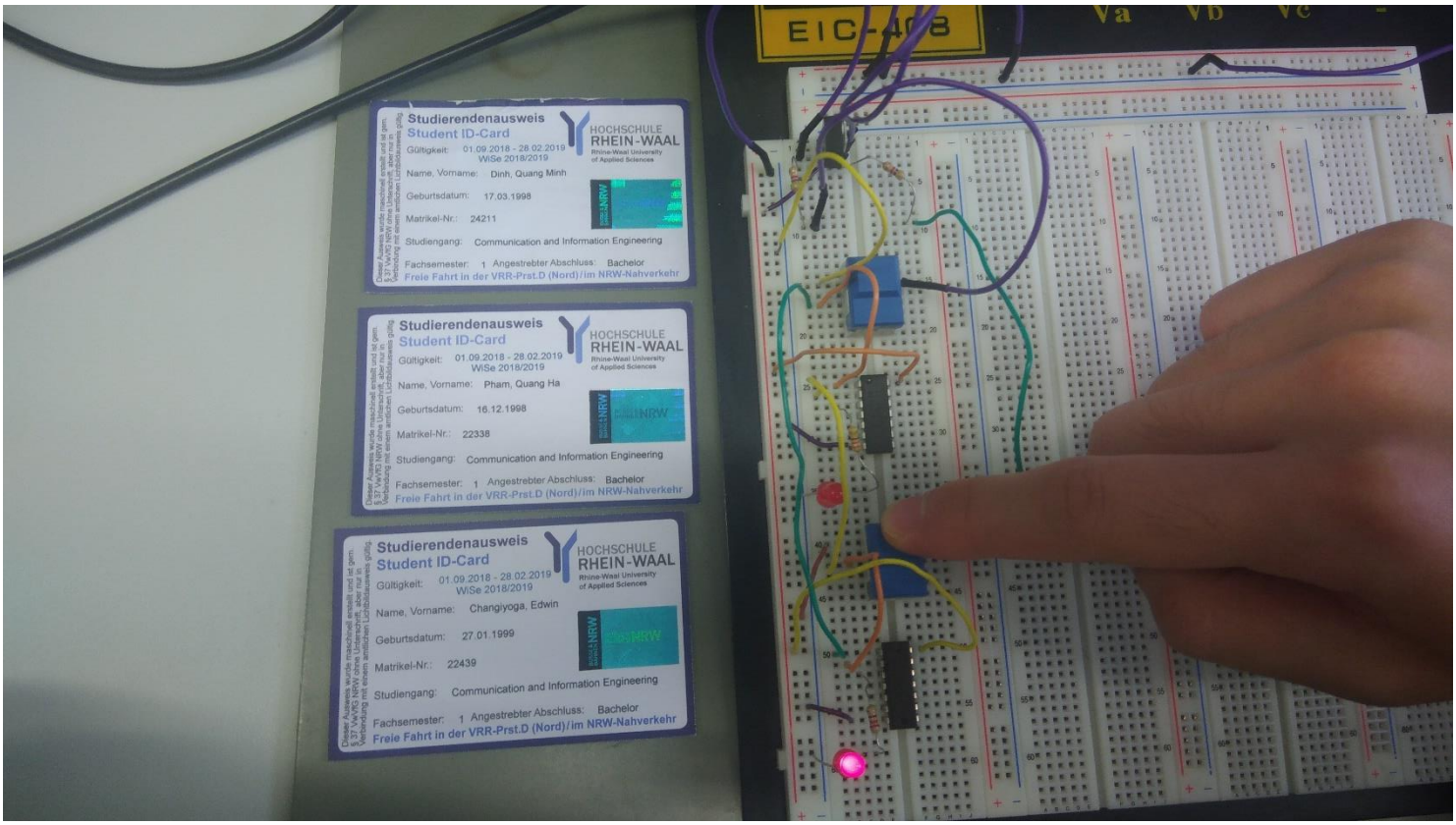
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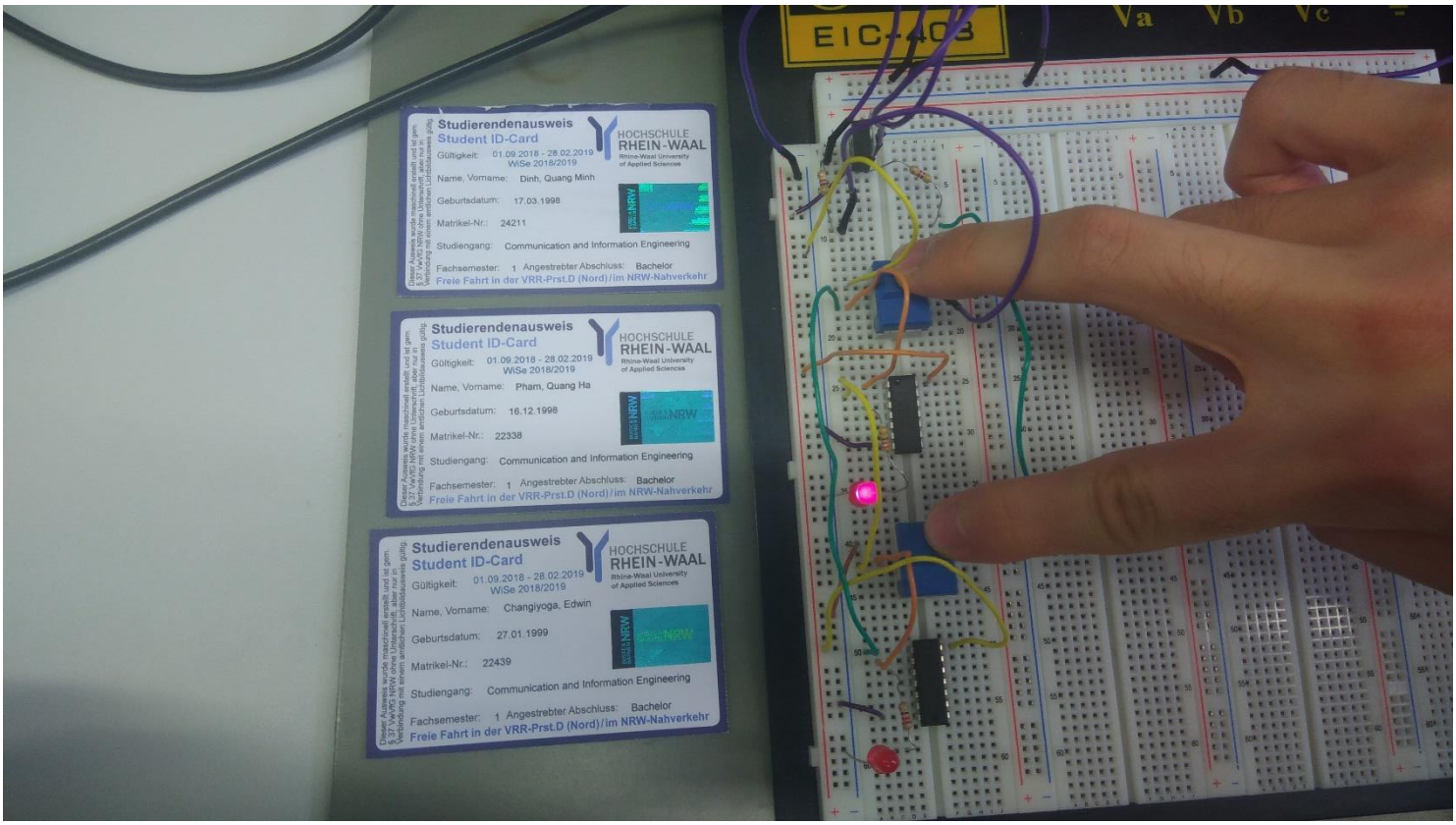

Result:

Input A	Input B	Output AND Gate	Output NAND Gate
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

The output of NAND gate is the complete opposite of AND gate, it is similar to an AND gate with the output connected to an Inverter.

Challenge #6

Abstract:

Our group managed to follow the steps given in the Description and completed the challenge without anything special to report.

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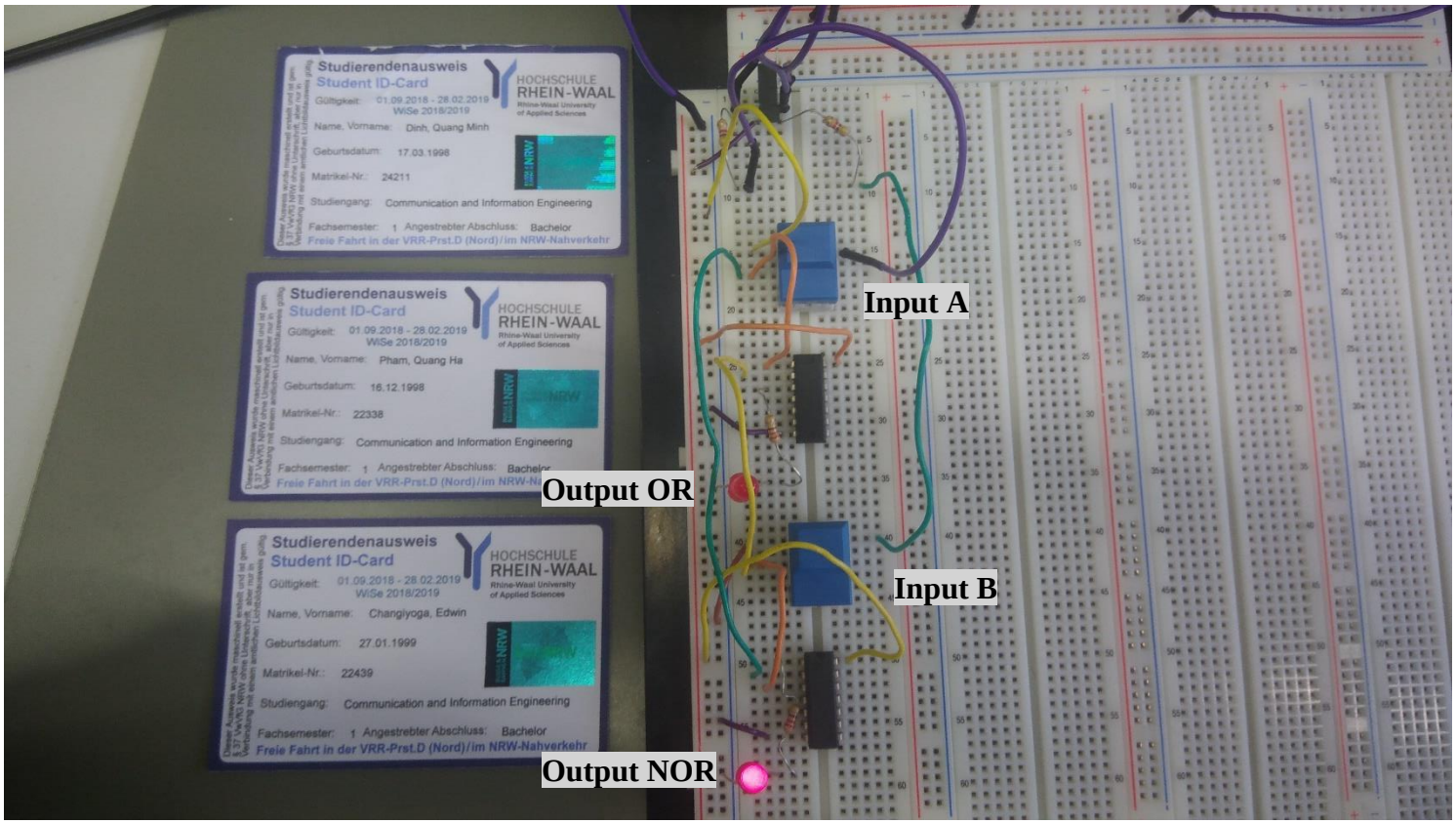

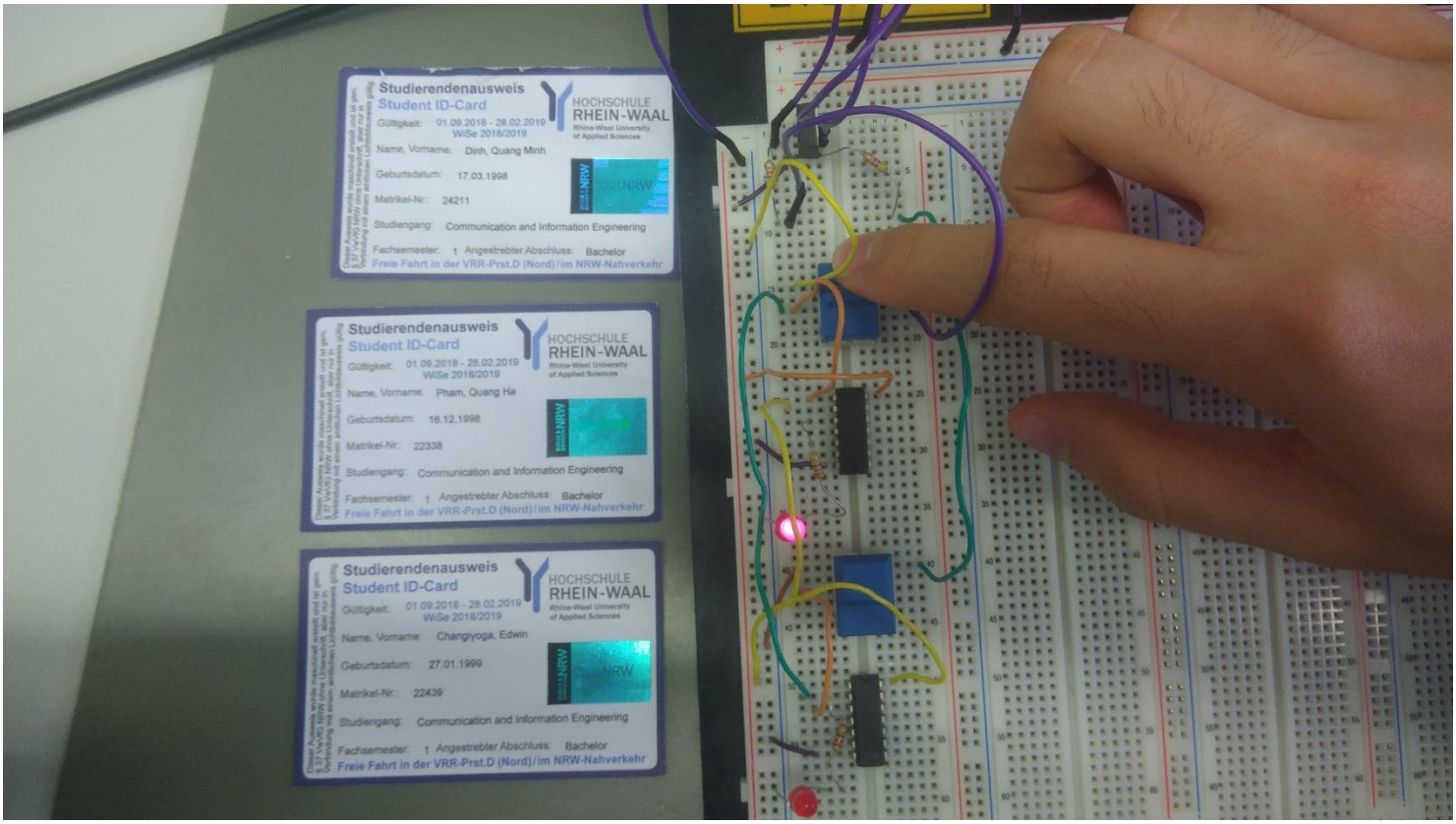
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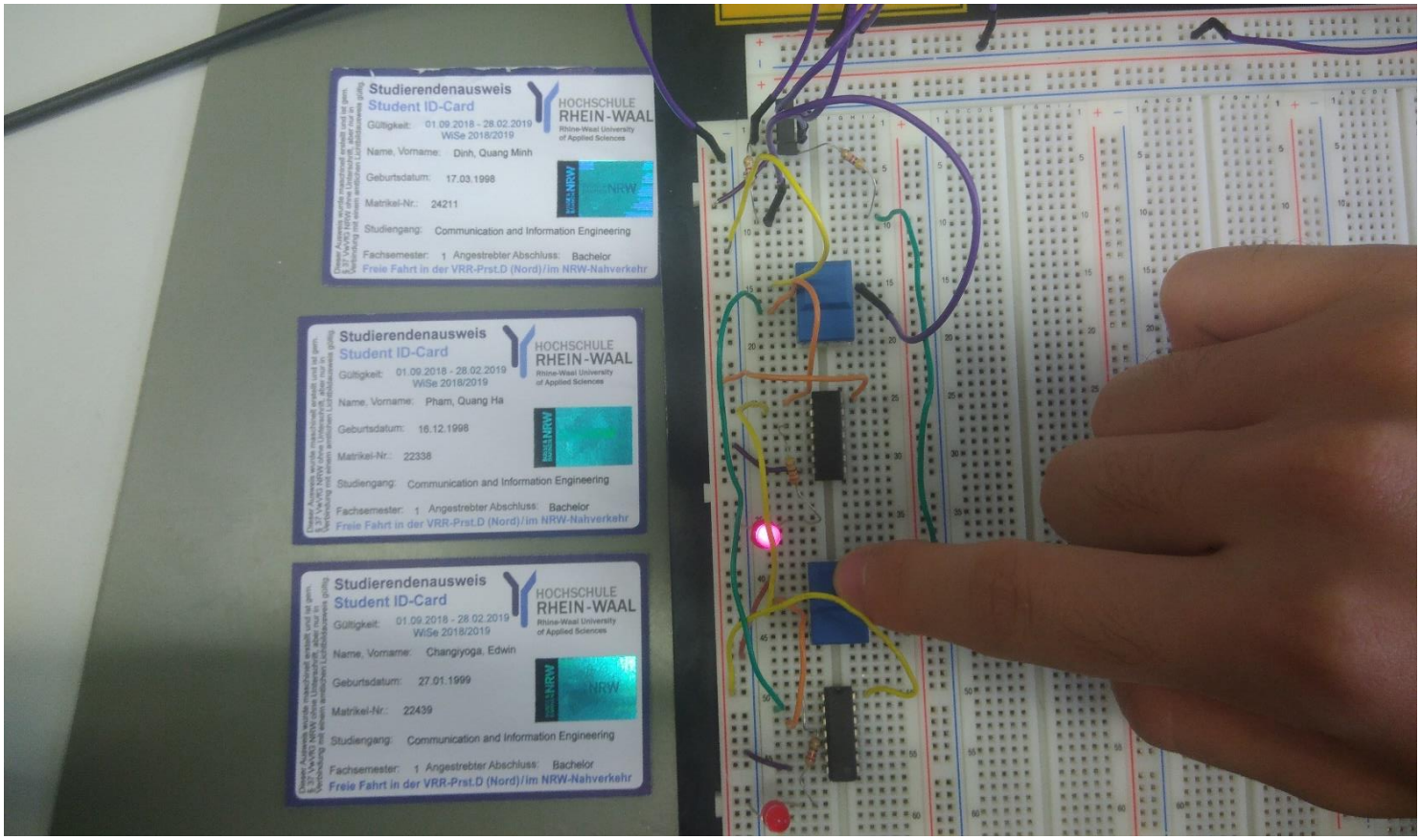
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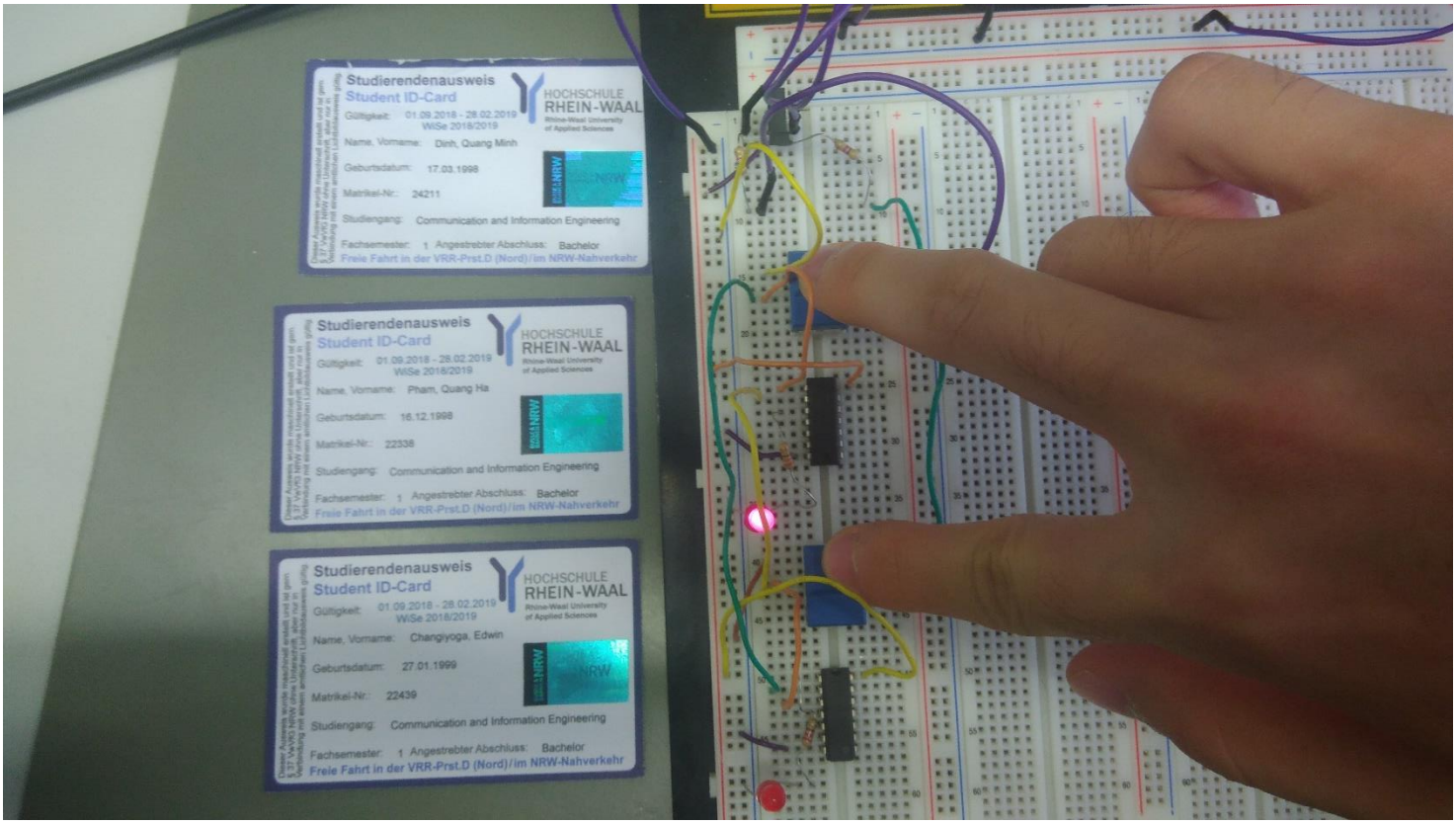


Result:

Input A	Input B	Output OR Gate	Output NOR Gate
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

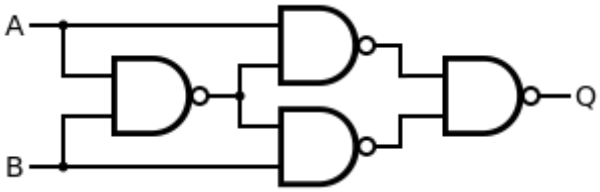
Similar to challenge 5, OR and NOR is the opposite to each other output wise.

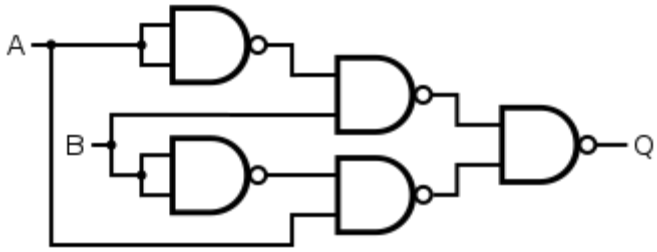
Challenge #7

Abstract:

Our group managed to follow the steps given in the Description and completed the challenge. But there are some things to note.

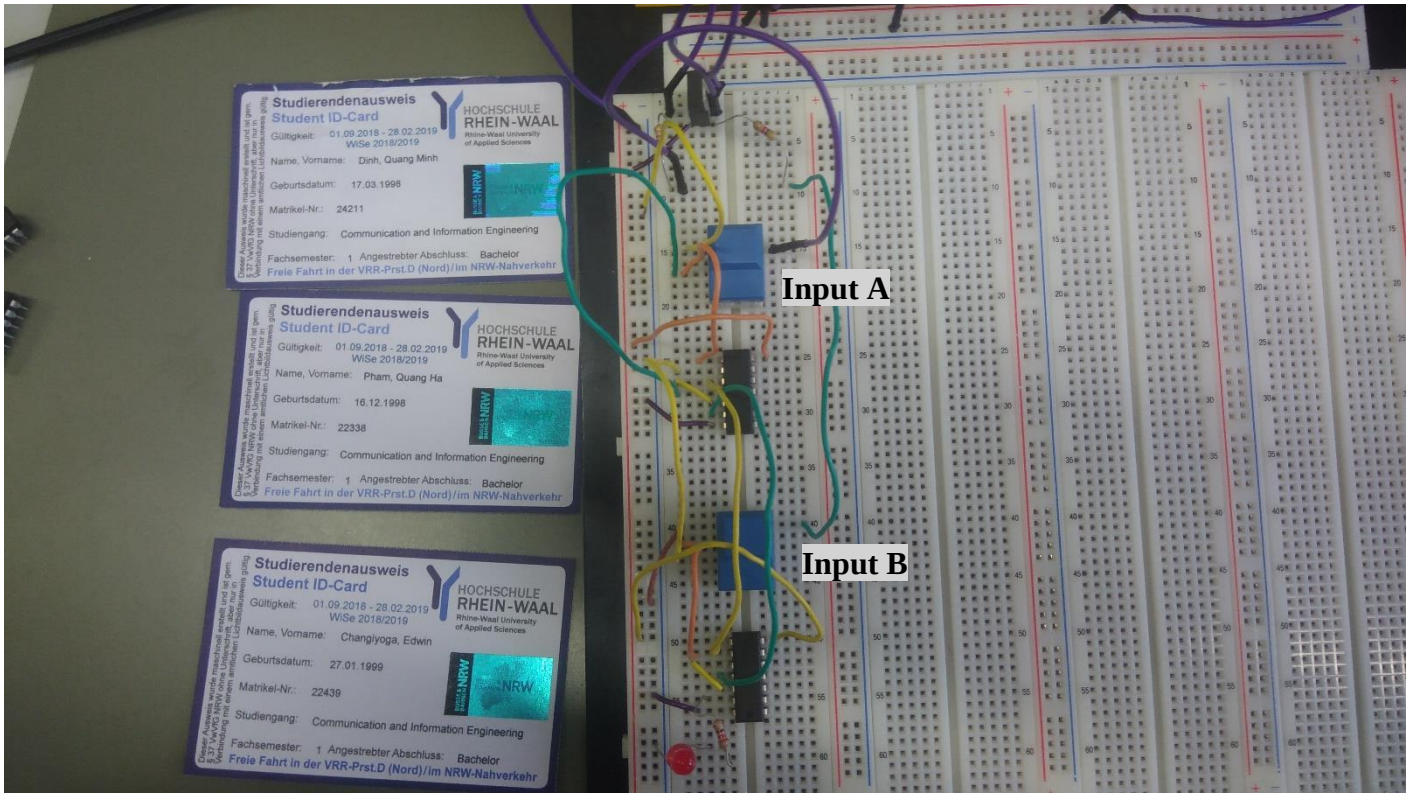
We found these two pictures describing how XOR gate can be constructed using NAND gates on Wikipedia (https://en.wikipedia.org/wiki/XOR_gate).

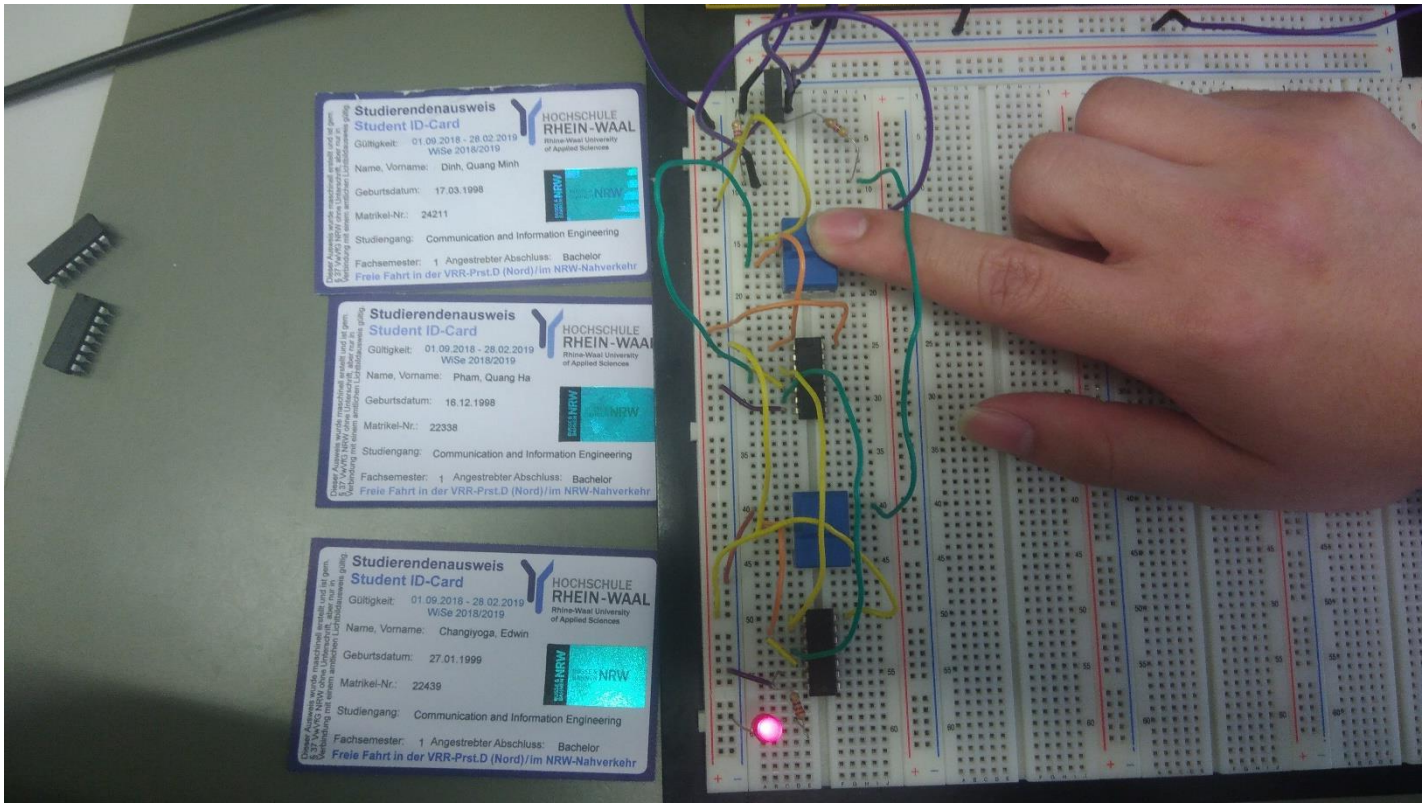




We decided to construct the circuit on our breadboard using the schematic on the left.

Pictures:

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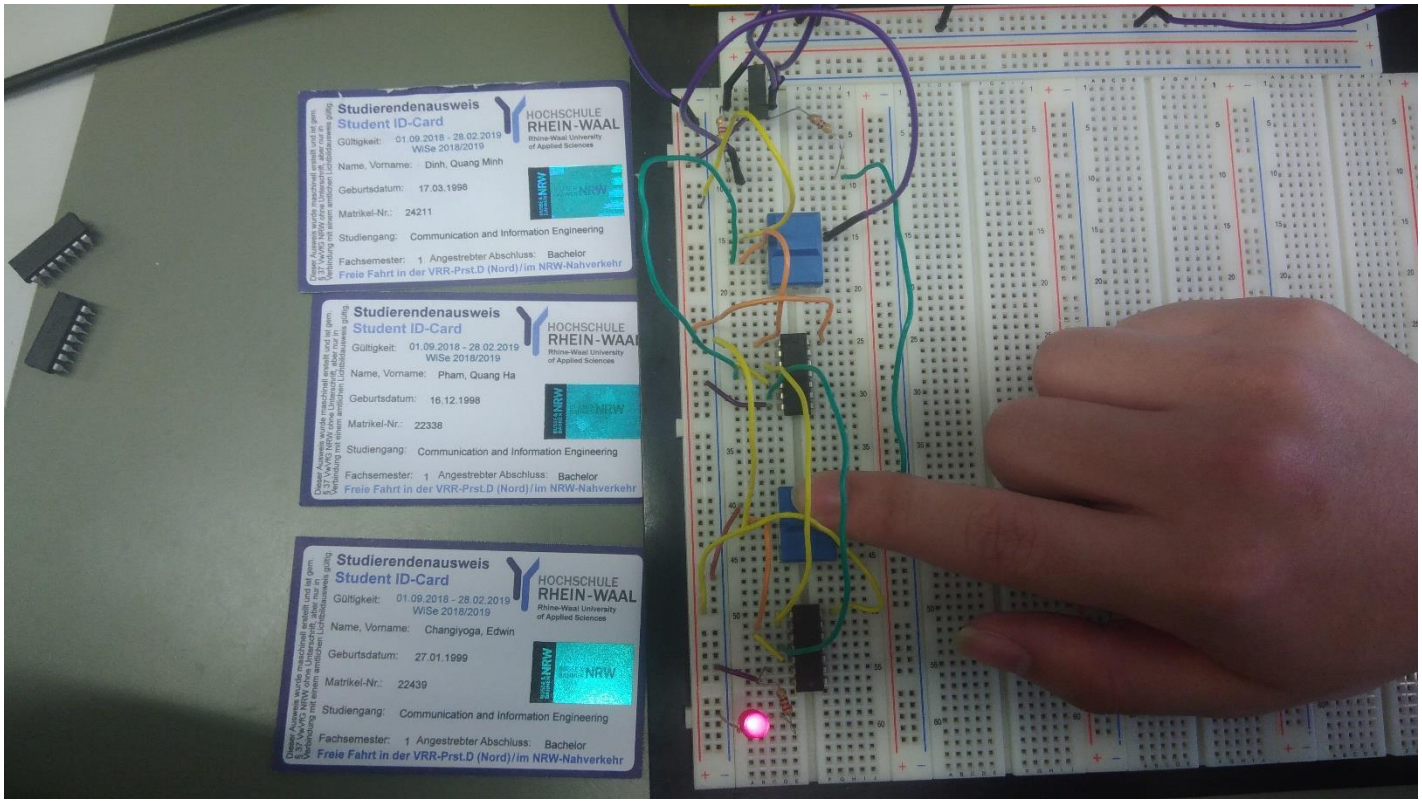
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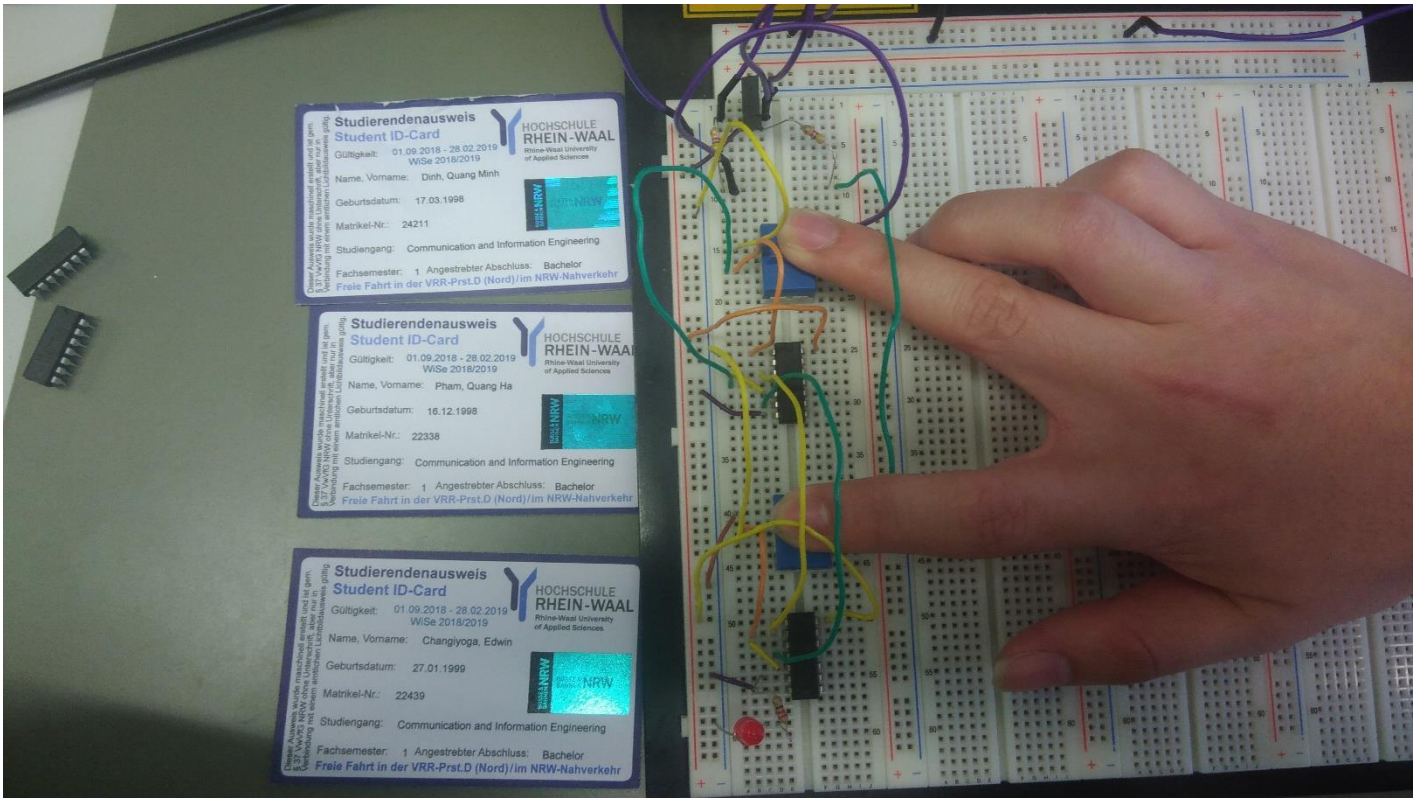


Result:

Input A	Input B	Output Tested XOR Gate	Output Specification
0	0	0	0
1	0	1	1
0	1	1	1
1	1	0	0

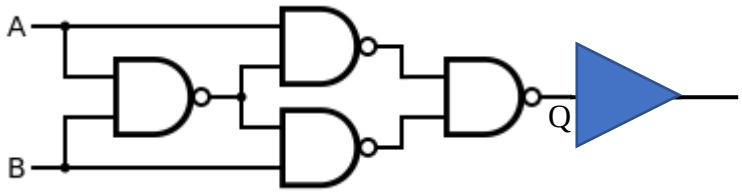
Challenge #8

Abstract:

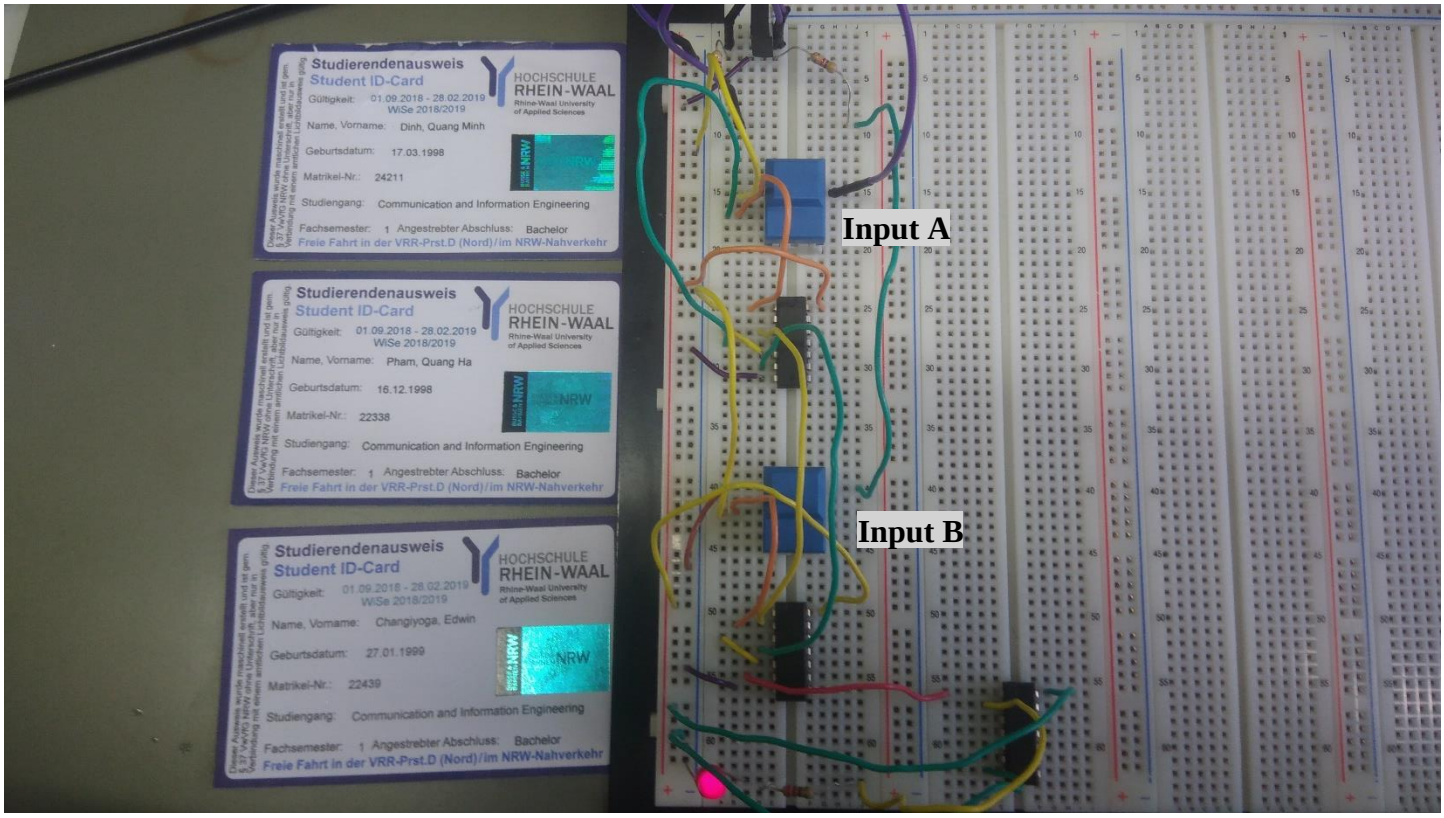
Our group managed to follow the steps given in the Description and completed the challenge. But there are some things to note.

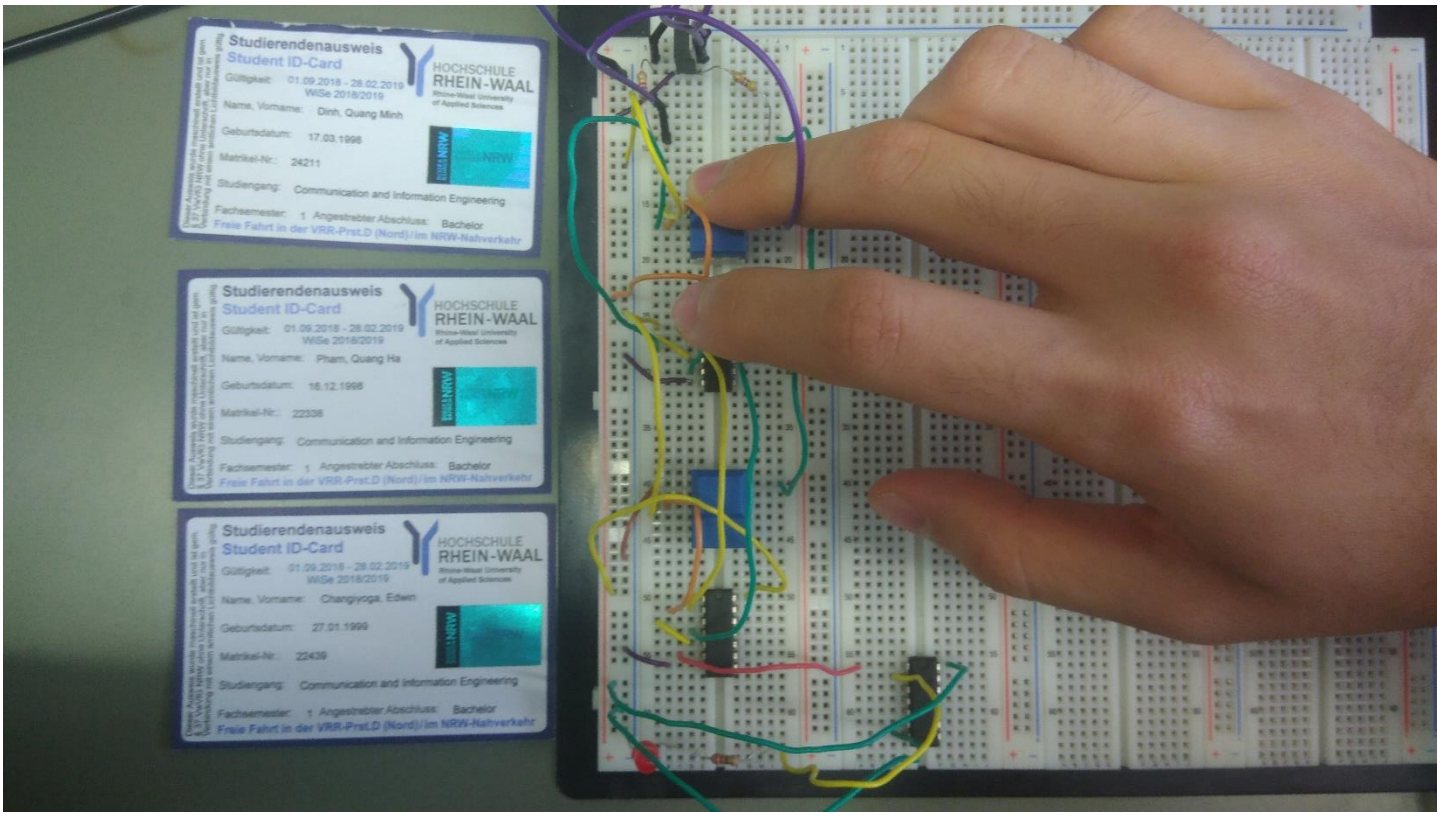
The booklet asks us “How can an XNOR-Gate be built by using the result of challenge #7” so the way we understand it is to expand the circuitry from Challenge #7.

Using our understanding, we figured that the XNOR gate is the same as an XOR gate with an Inverter. So, the only thing we needed to do is connect the output Q from Challenge #7 to an Inverter (represented by a blue triangle).



Pictures:




Studierendenausweis
Student ID-Card
HOCHSCHULE
RHEIN-WAAL
Gültigkeit: 01.09.2018 - 28.02.2019
WiSe 2018/2019
Name, Vorname: Dinh, Quang Minh
Geburtsdatum: 17.03.1998
Matrikel-Nr.: 24211
Studiengang: Communication and Information Engineering
Fachsemester: 1 Angestrebter Abschluss: Bachelor
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Gültigkeit: 01.09.2018 - 28.02.2019
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Name, Vorname: Changiyoga, Edwin
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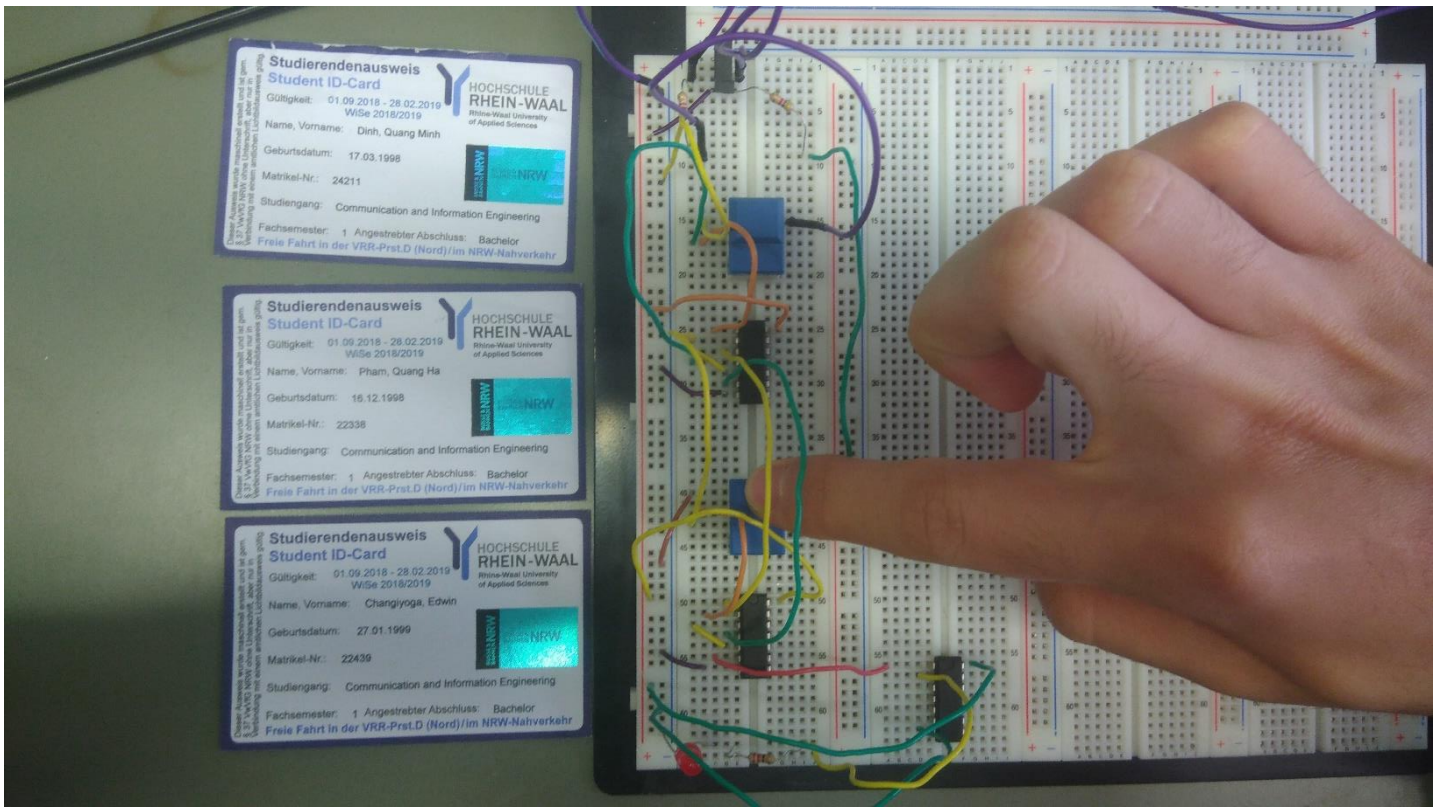
Matrikel-Nr.: 22439
Studiengang: Communication and Information Engineering
Fachsemester: 1 Angestrebter Abschluss: Bachelor
Freie Fahrt in der VRR-Prst.D (Nord)/im NRW-Nahverkehr


Studierendenausweis
Student ID-Card
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Gültigkeit: 01.09.2018 - 28.02.2019
WiSe 2018/2019
Name, Vorname: Dinh, Quang Minh
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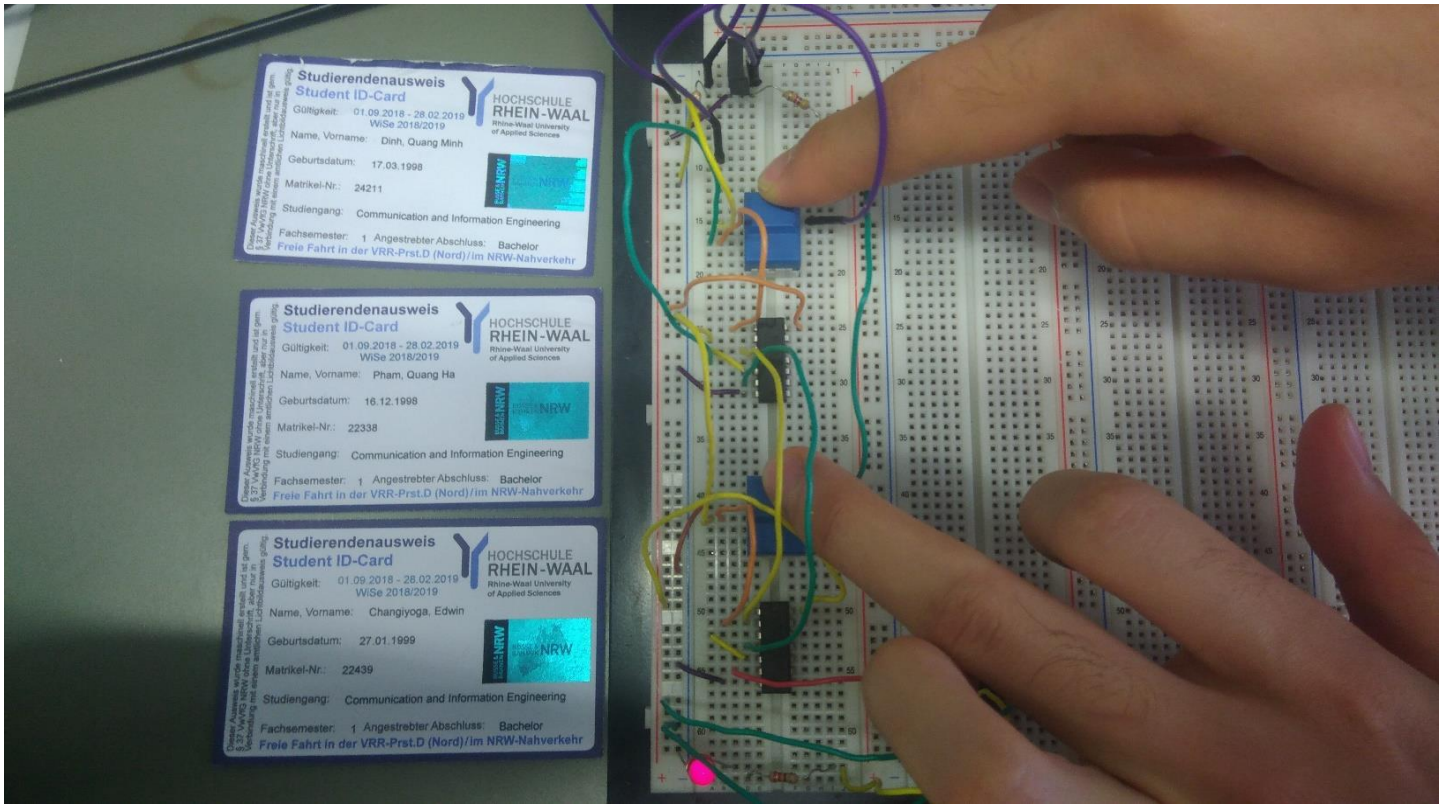


Result:

Input A	Input B	Output Tested XNOR Gate	Output Specification
0	0	1	1
1	0	0	0
0	1	0	0
1	1	1	1

Challenge #9

Abstract:

Our group managed to follow the steps given in the Description and completed the challenge without anything special to report.

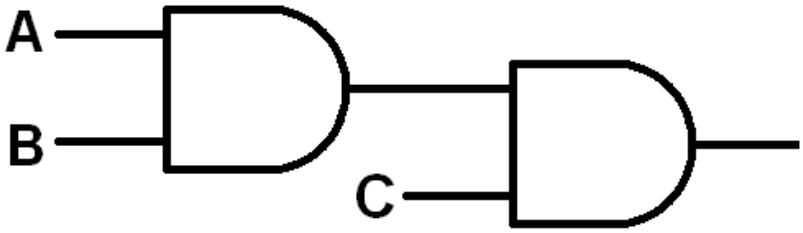
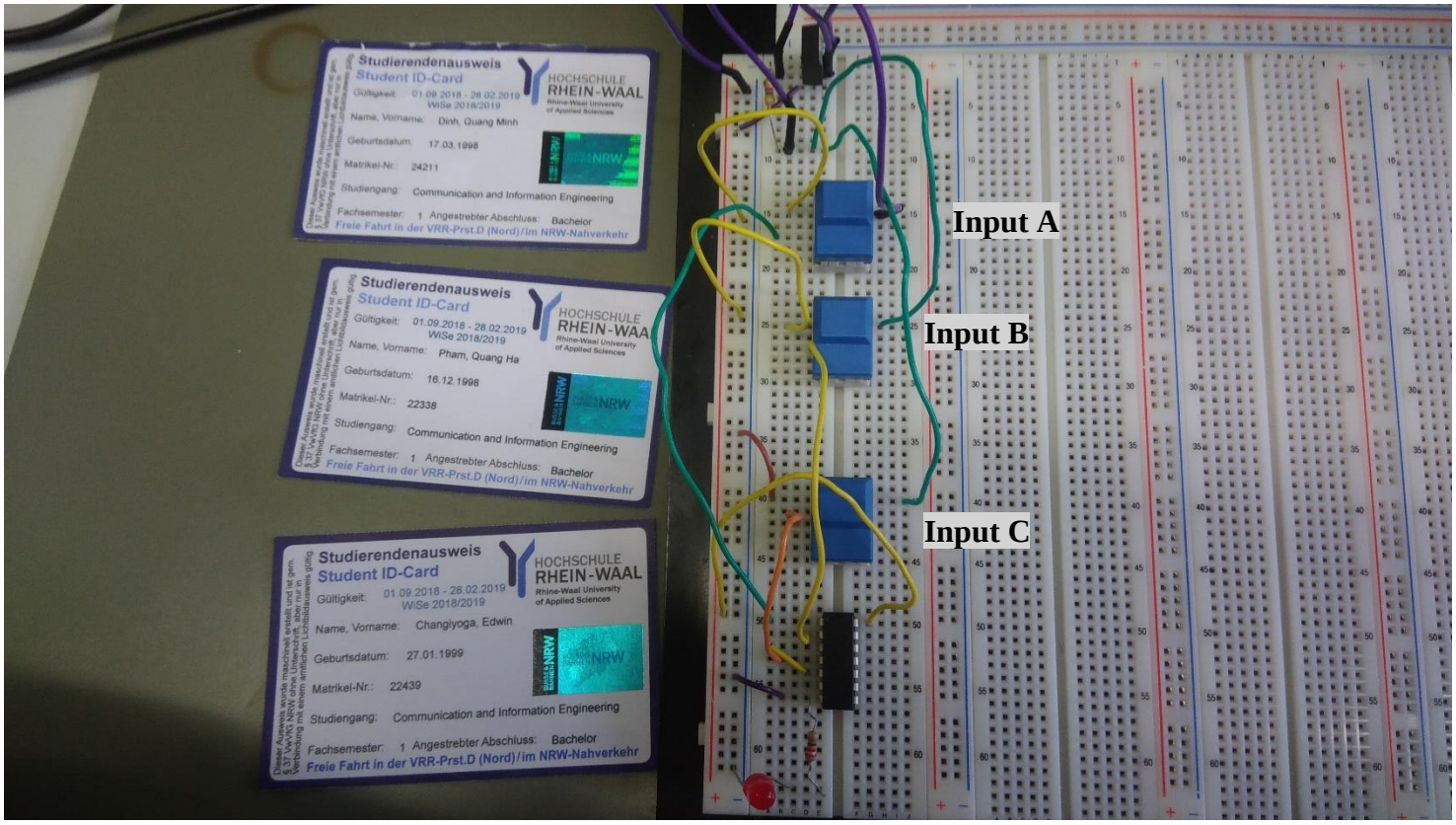
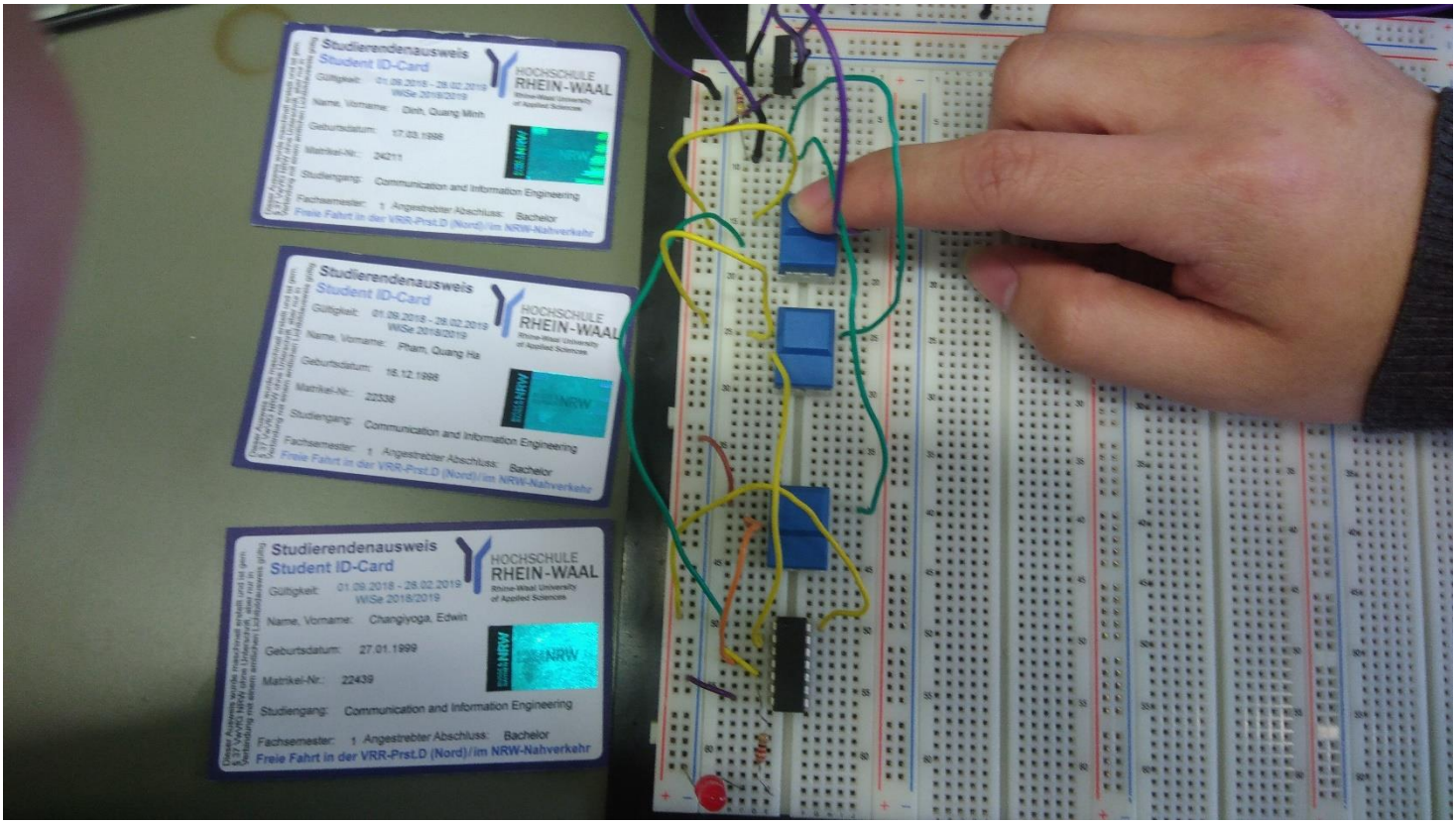


Figure 2: 3 Input AND using two 2 Input AND

Pictures:

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Gültigkeit: 01.09.2018 - 28.02.2019
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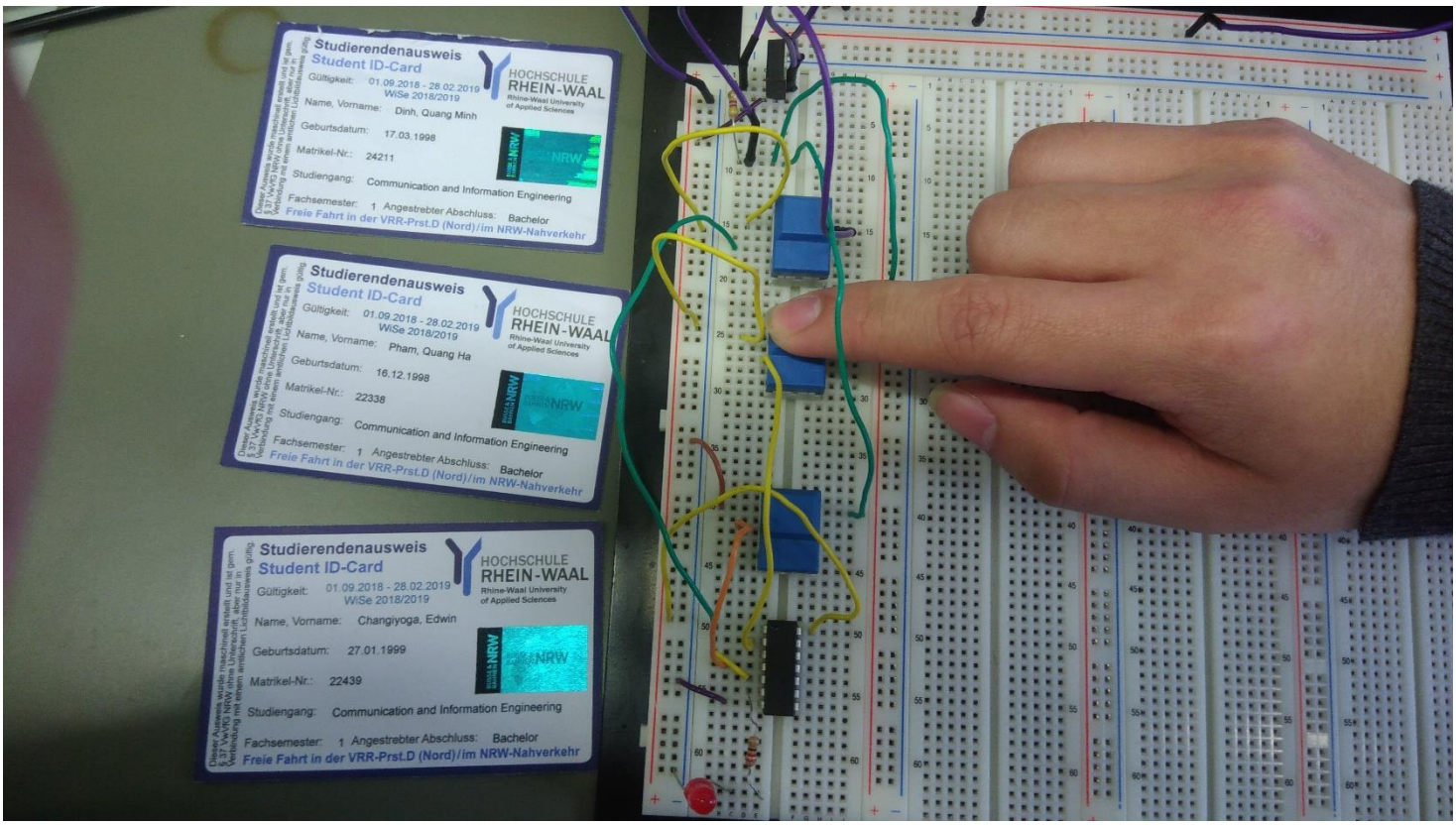
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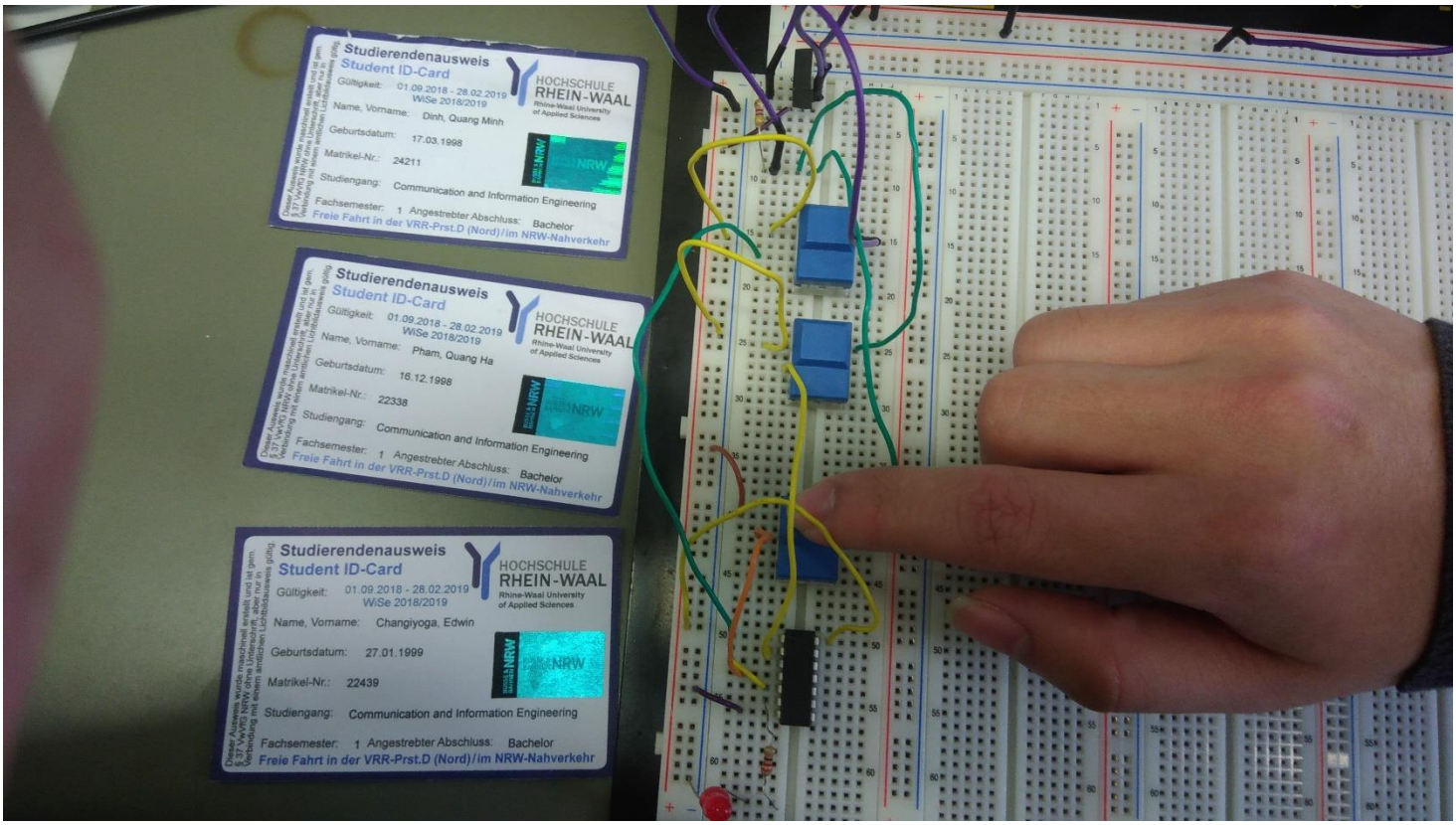
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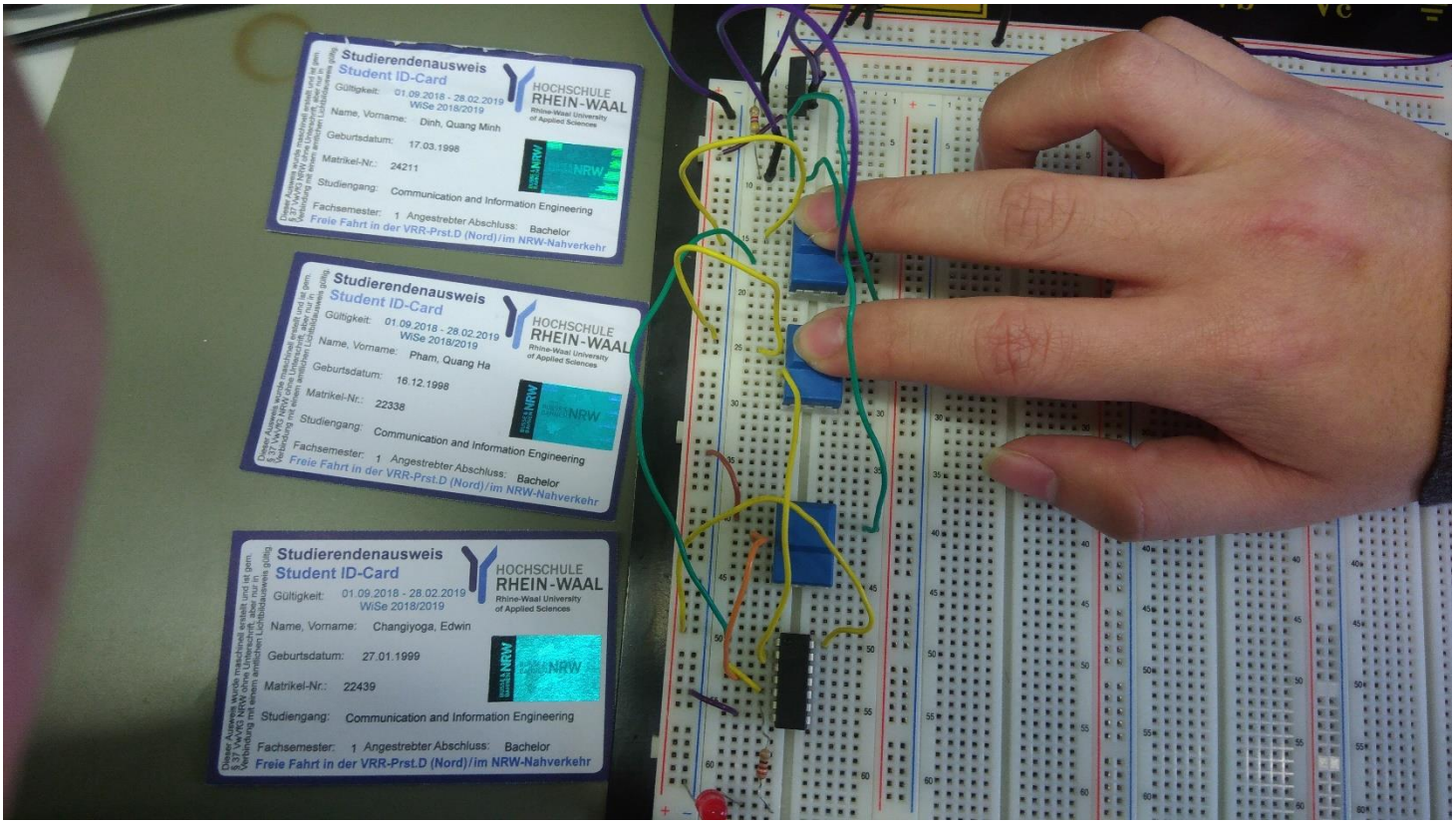
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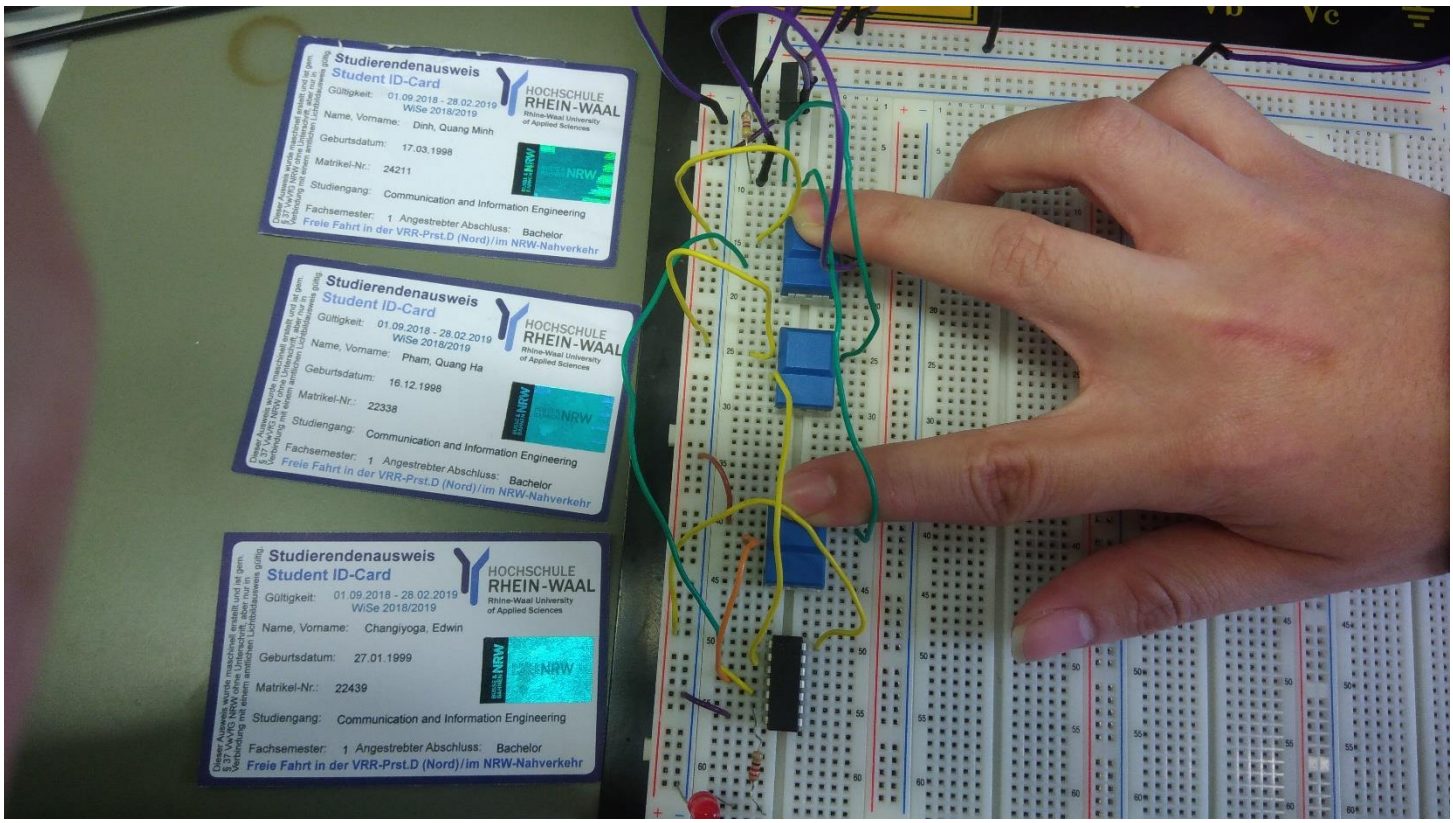
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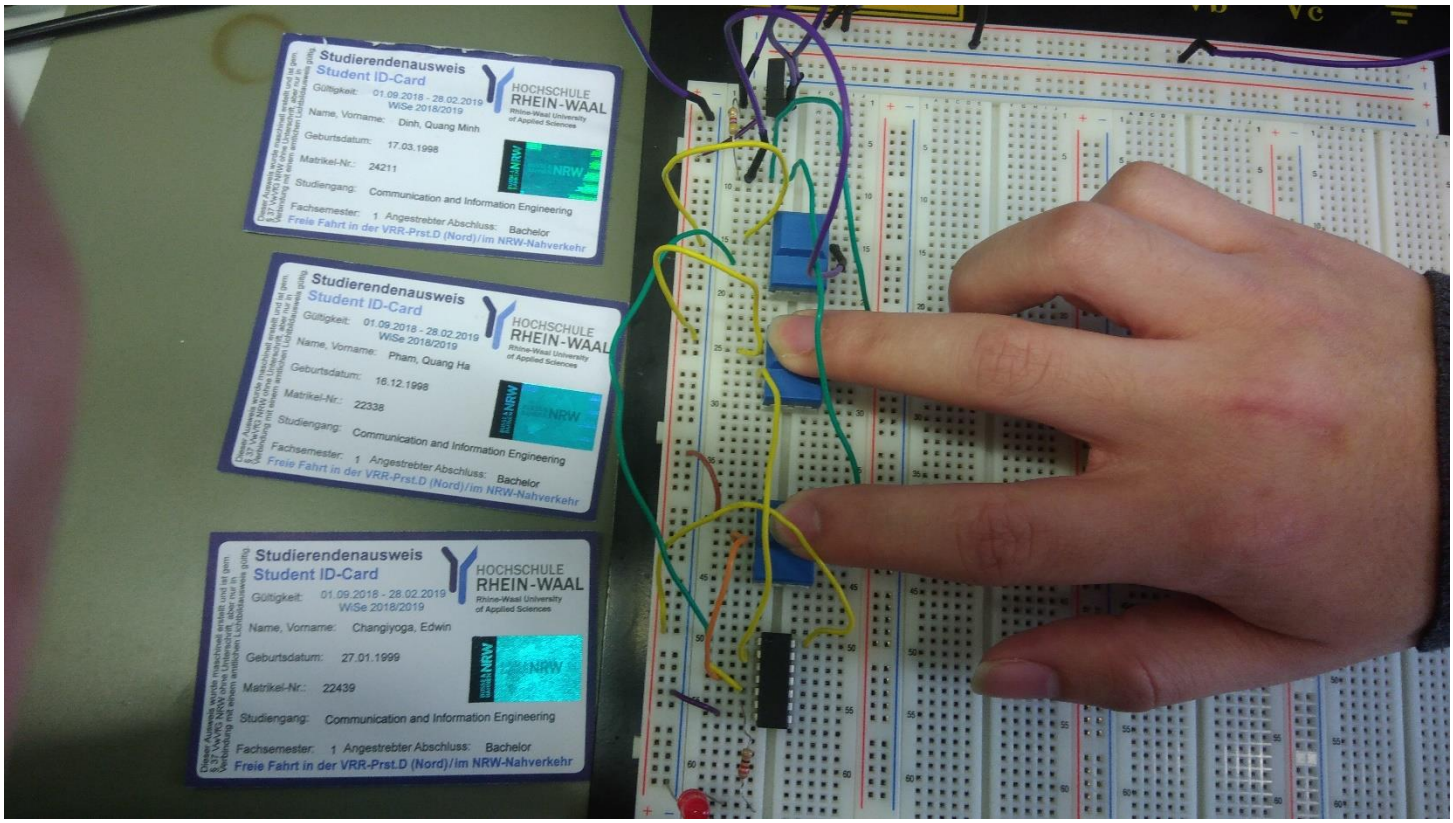
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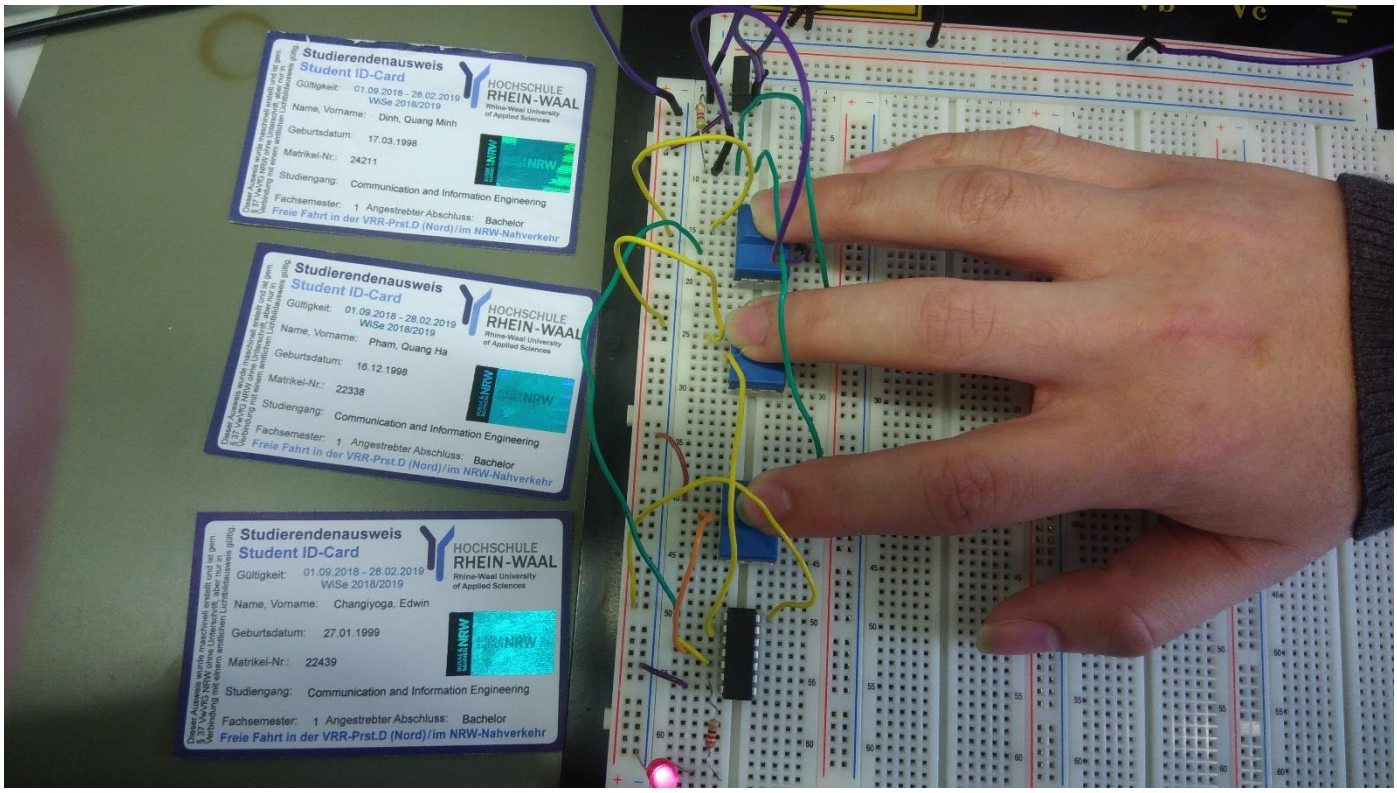


Result:

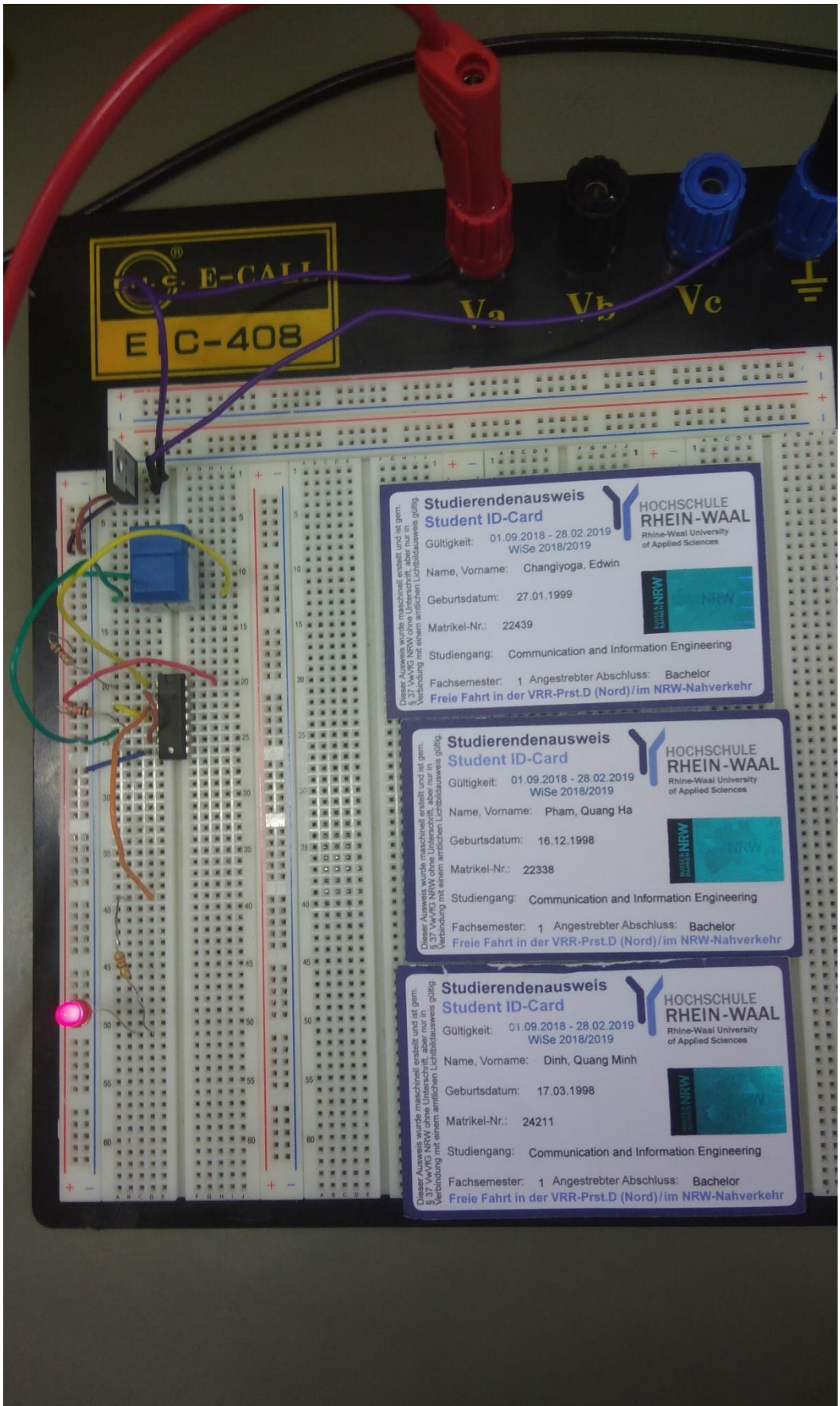
Input A	Input B	Input C	Output AND-Gate	Output Specification
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	0
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	1	1

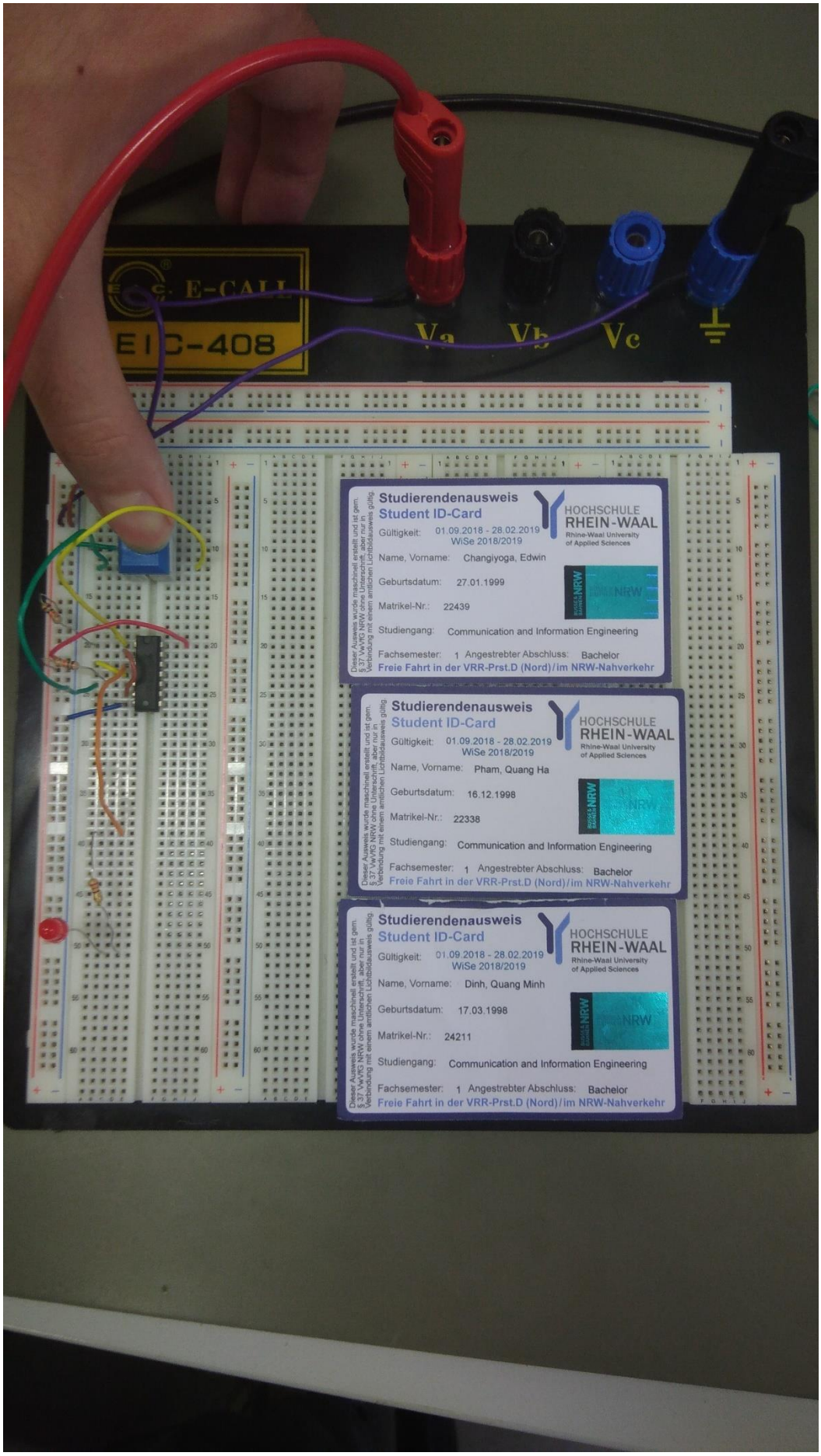
Challenge #10

Abstract:

Our group managed to follow the steps given in the Description and completed the challenge without anything special to report.

Pictures:




E-CALL
EIC-408
Va
Vb
Vc
Studierendenausweis
Student ID-Card
Gültigkeit: 01.09.2018 - 28.02.2019
WiSe 2018/2019
HOCHSCHULE RHEIN-WAAL
Rhine-Waal University of Applied Sciences
Name, Vorname: Changiyoga, Edwin
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Freie Fahrt in der VRR-Prst.D (Nord)/im NRW-Nahverkehr

Result:

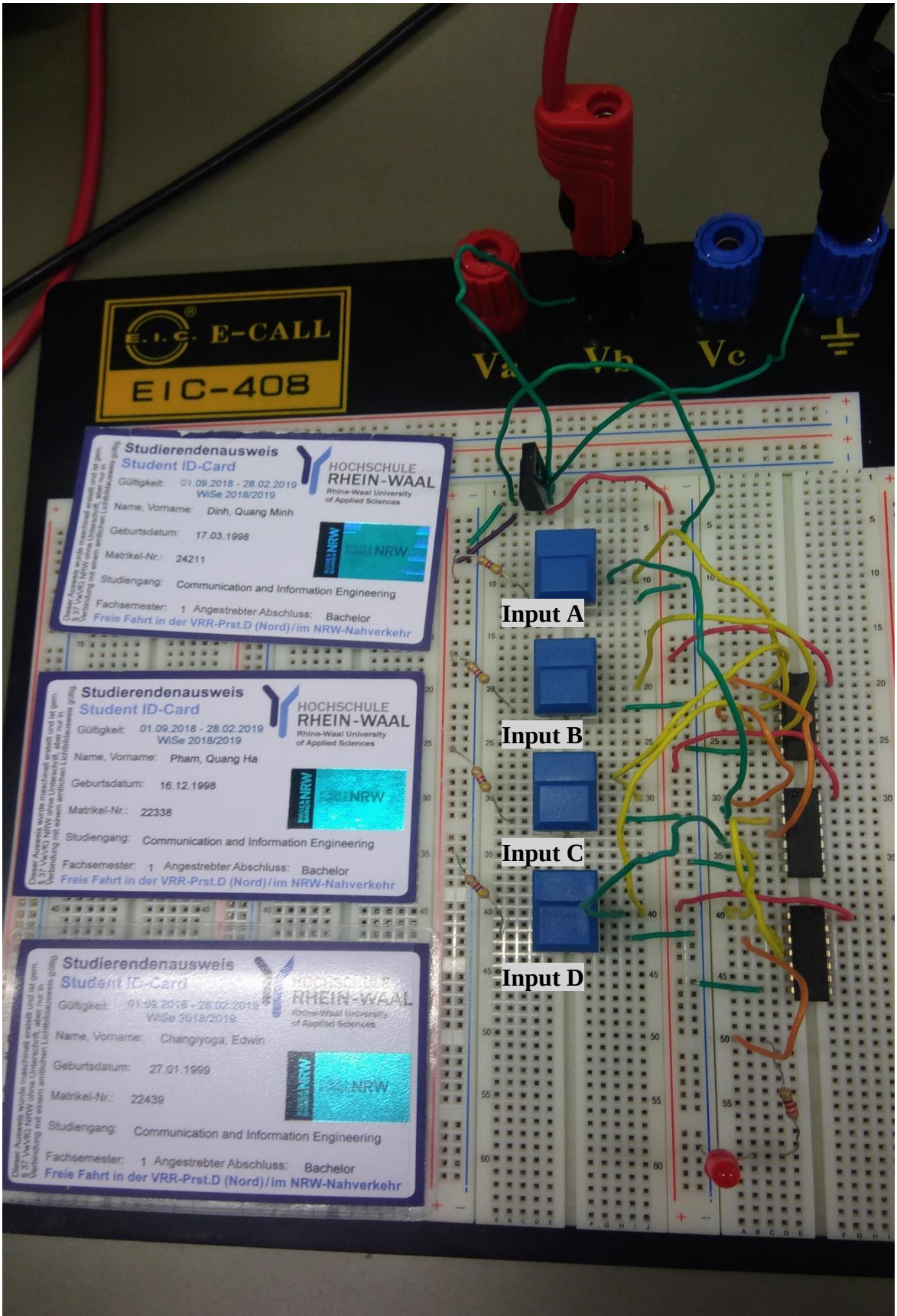
State of switch	Logical output
Not pressed	1
Pressed	0

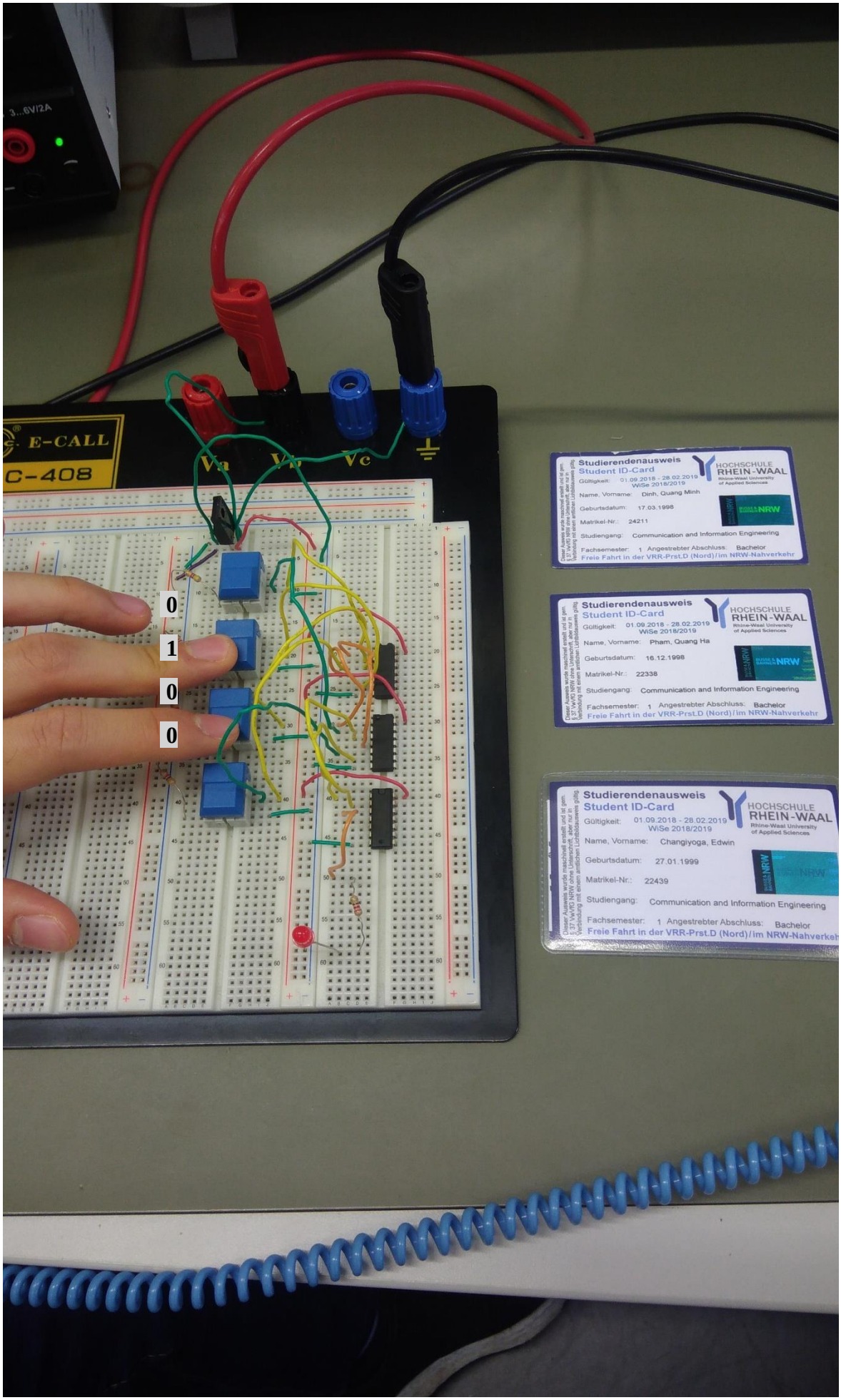
Challenge #11

Abstract:

Our group managed to follow the steps given in the Description and completed the challenge without anything special to report.

Pictures:




E-CALL
C-408
Va
Vb
Vc
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1
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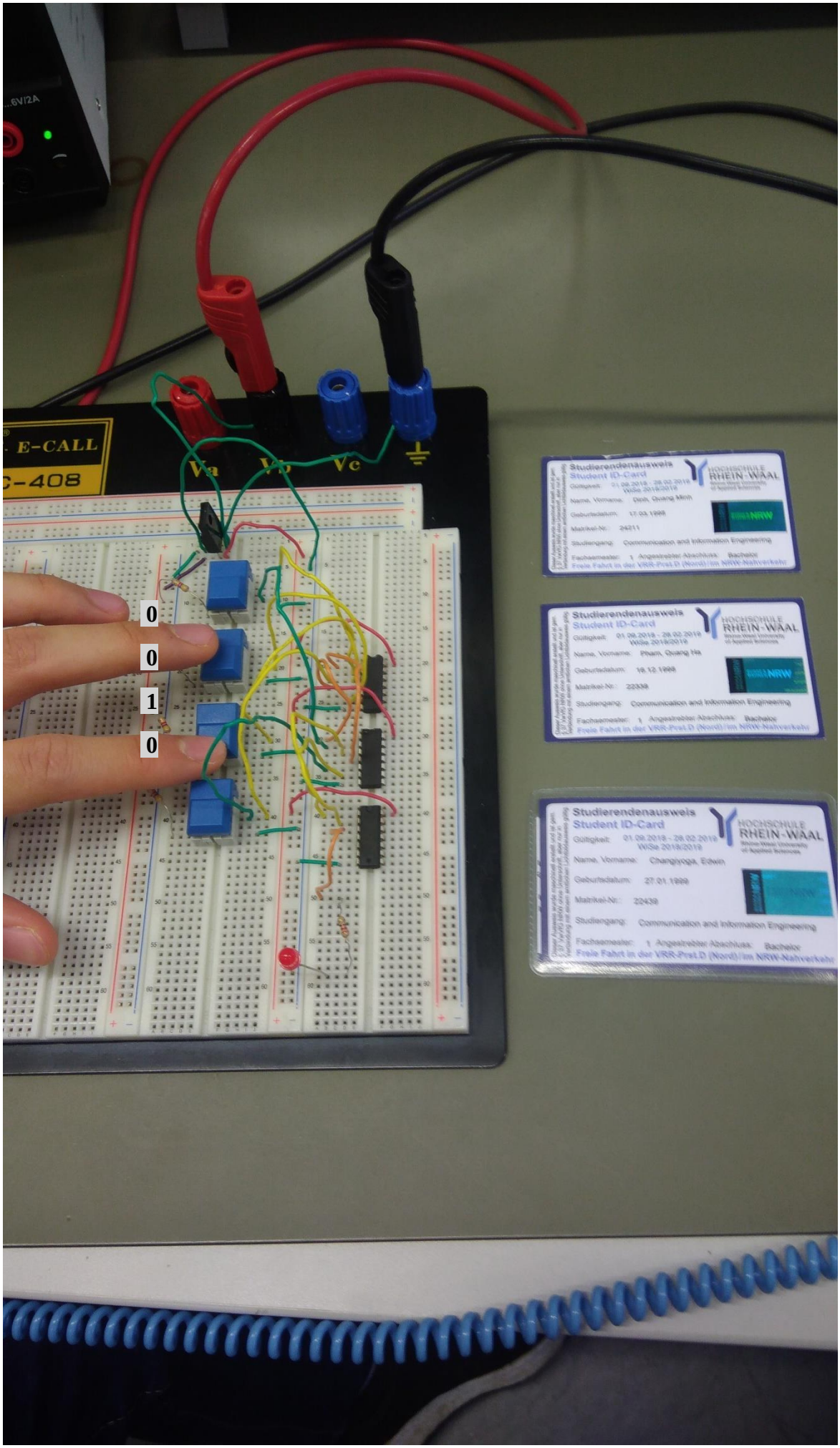
E-CALL
C-408
Va
Vb
Vc
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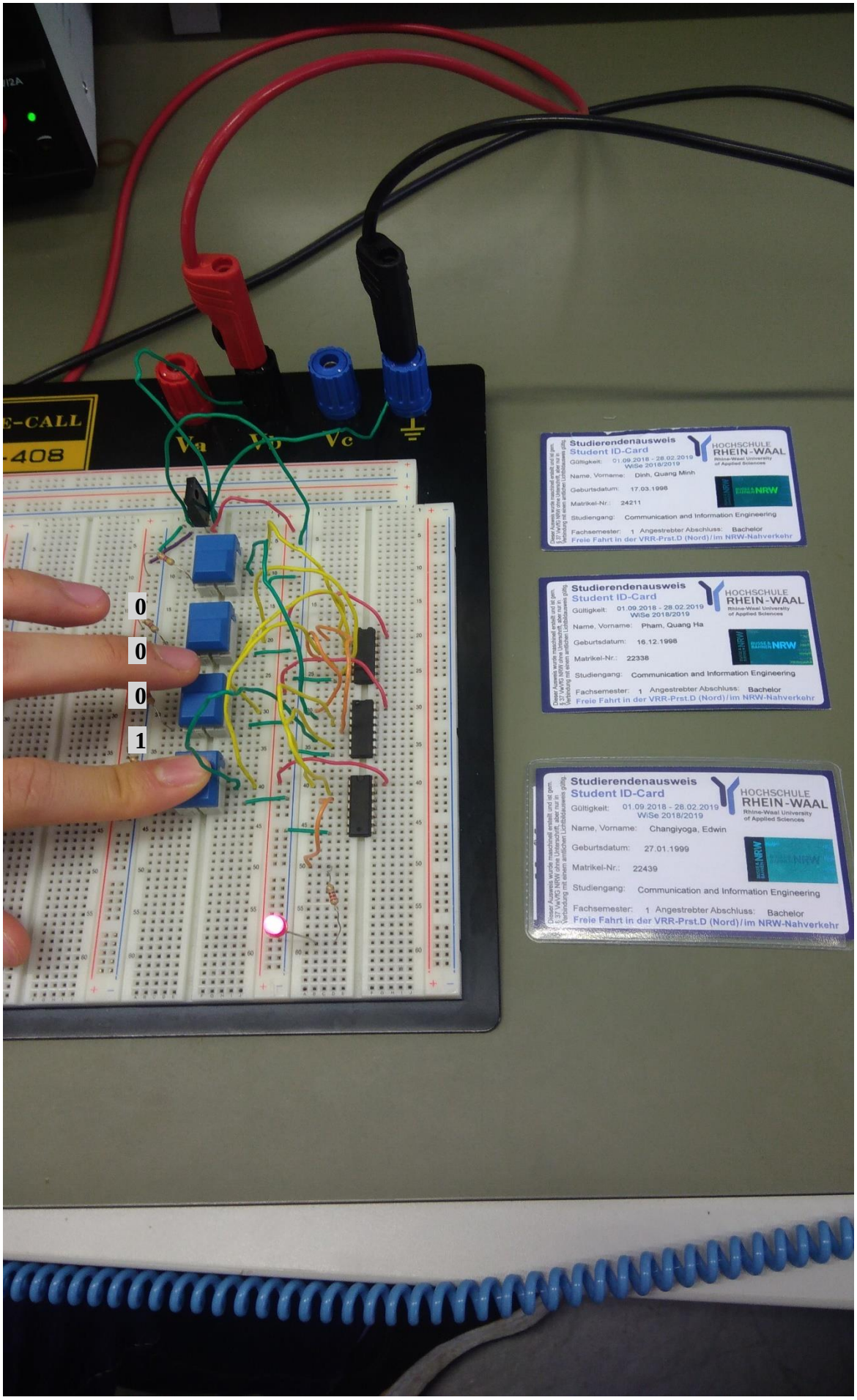
1
0
Studierendenausweis
Student ID-Card
HOCHSCHULE RHEIN-WAAL
Studierendenausweis
Student ID-Card
HOCHSCHULE RHEIN-WAAL
Studierendenausweis
Student ID-Card
HOCHSCHULE RHEIN-WAAL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Vb
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Studierendenausweis
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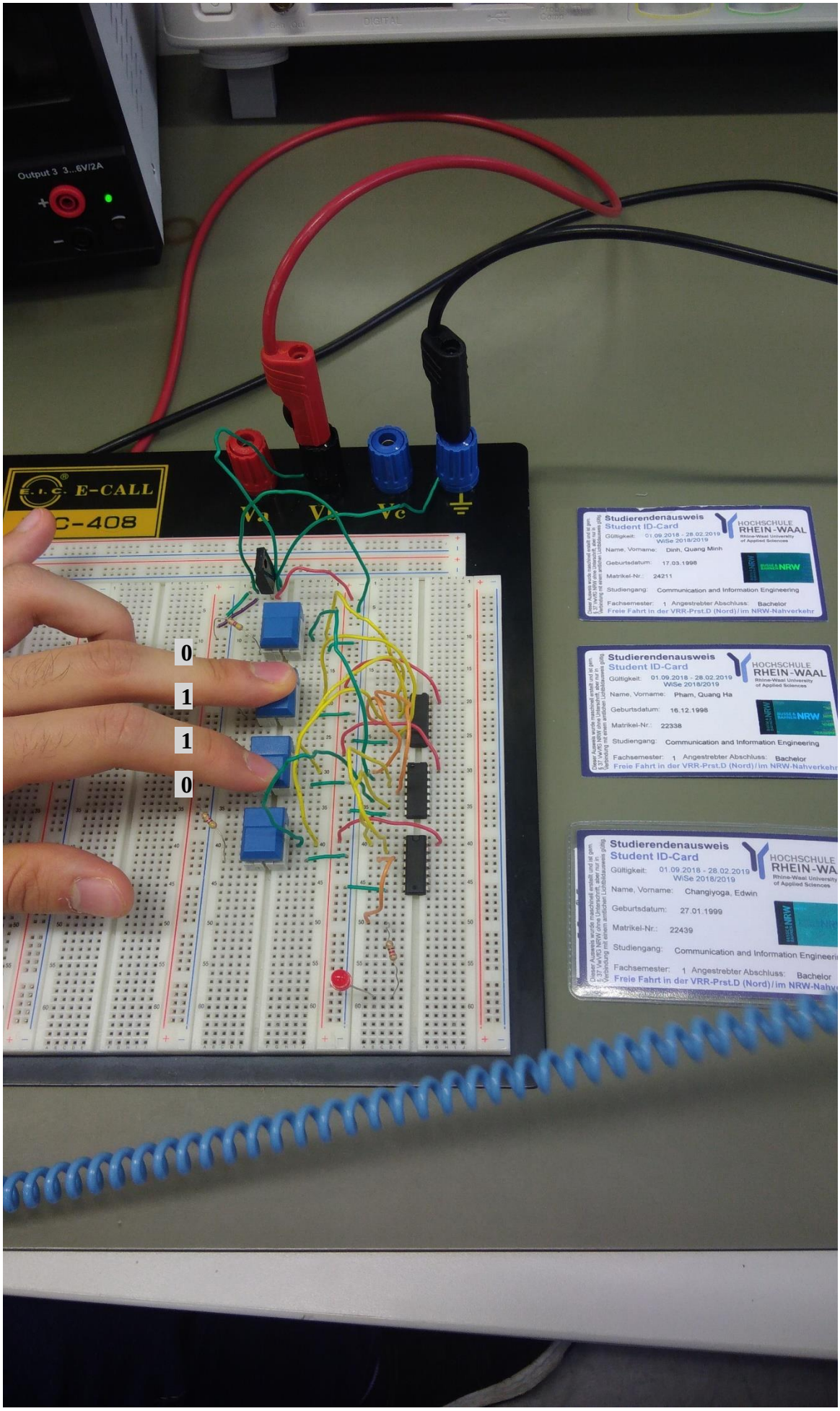
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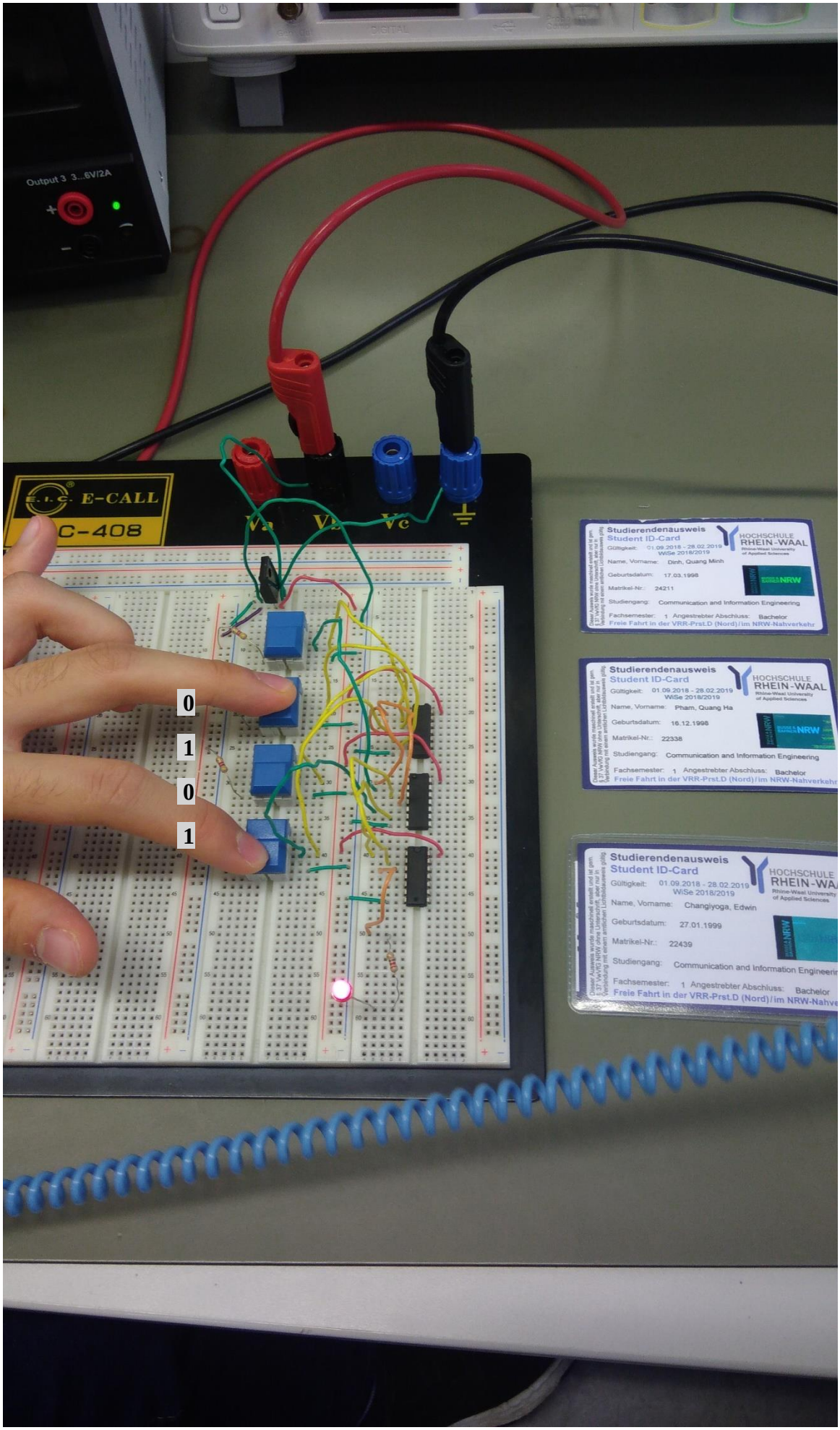
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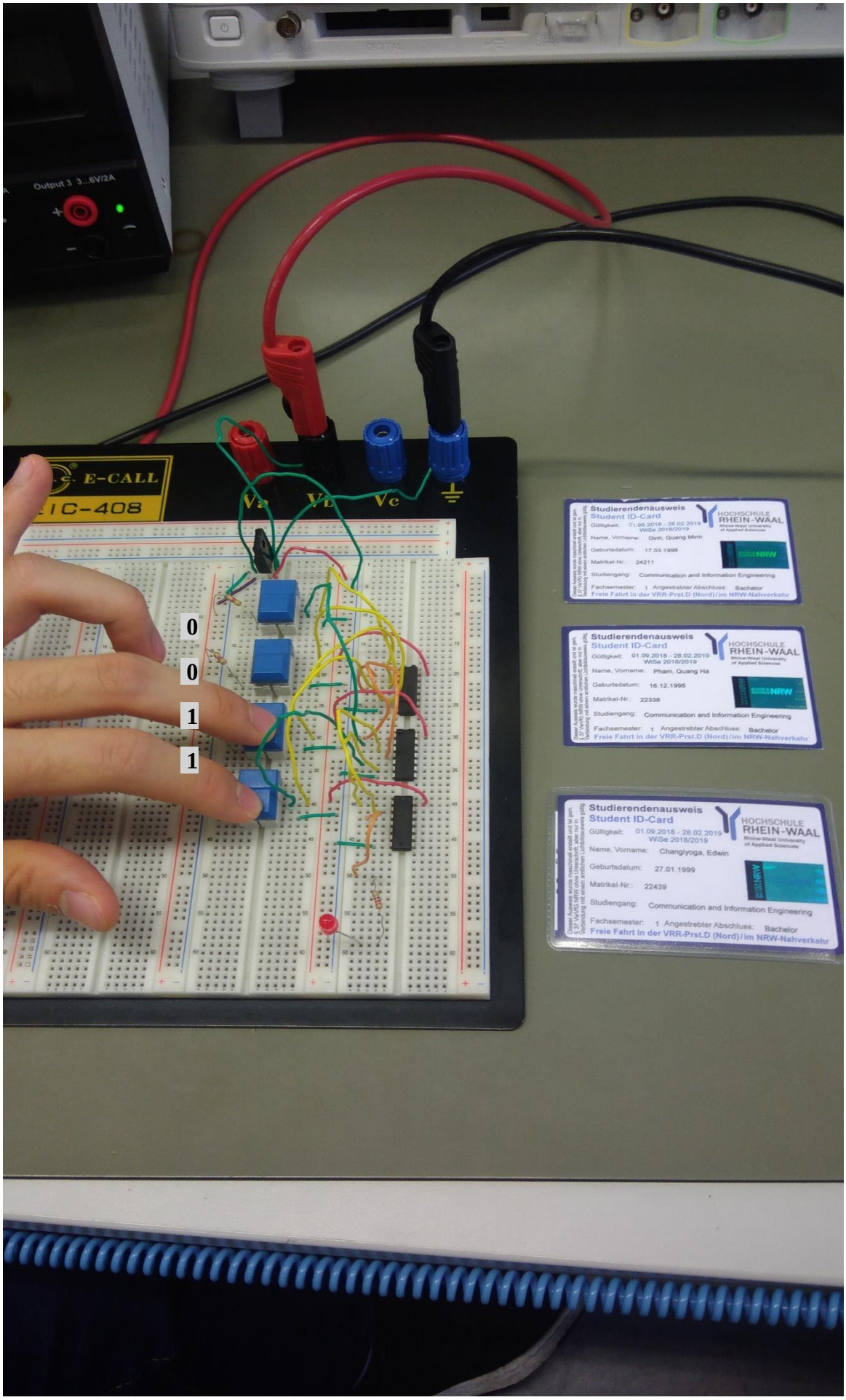
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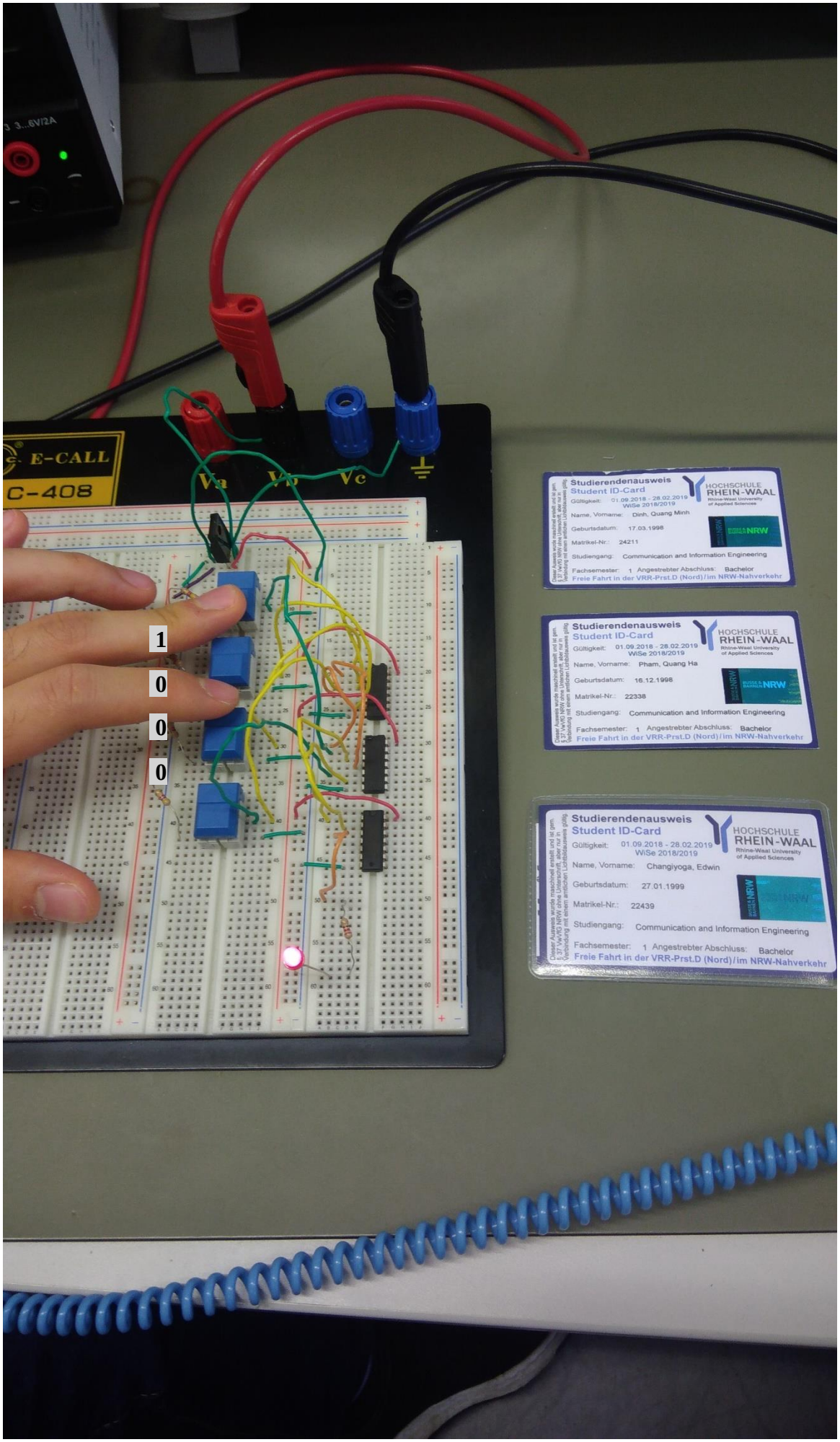
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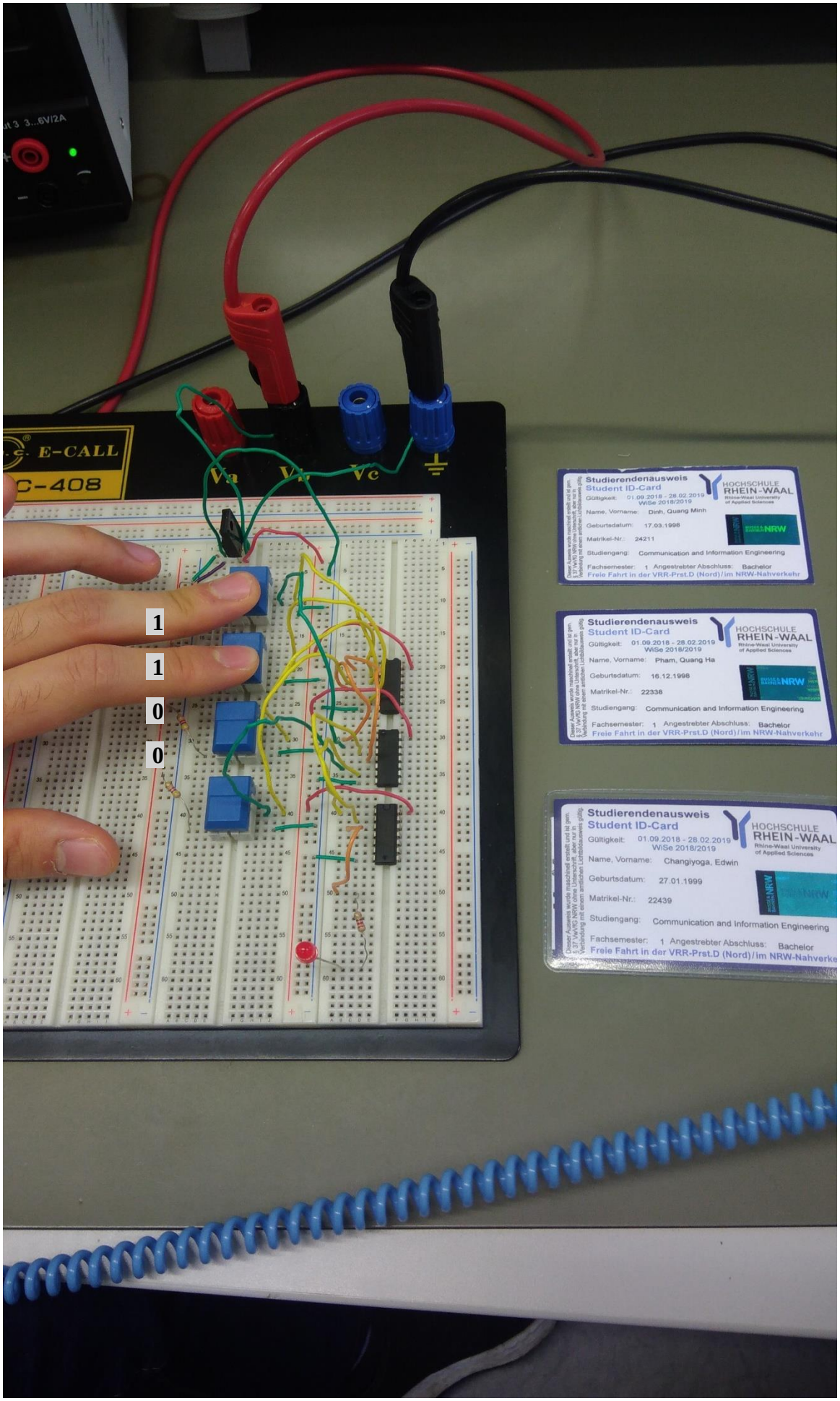
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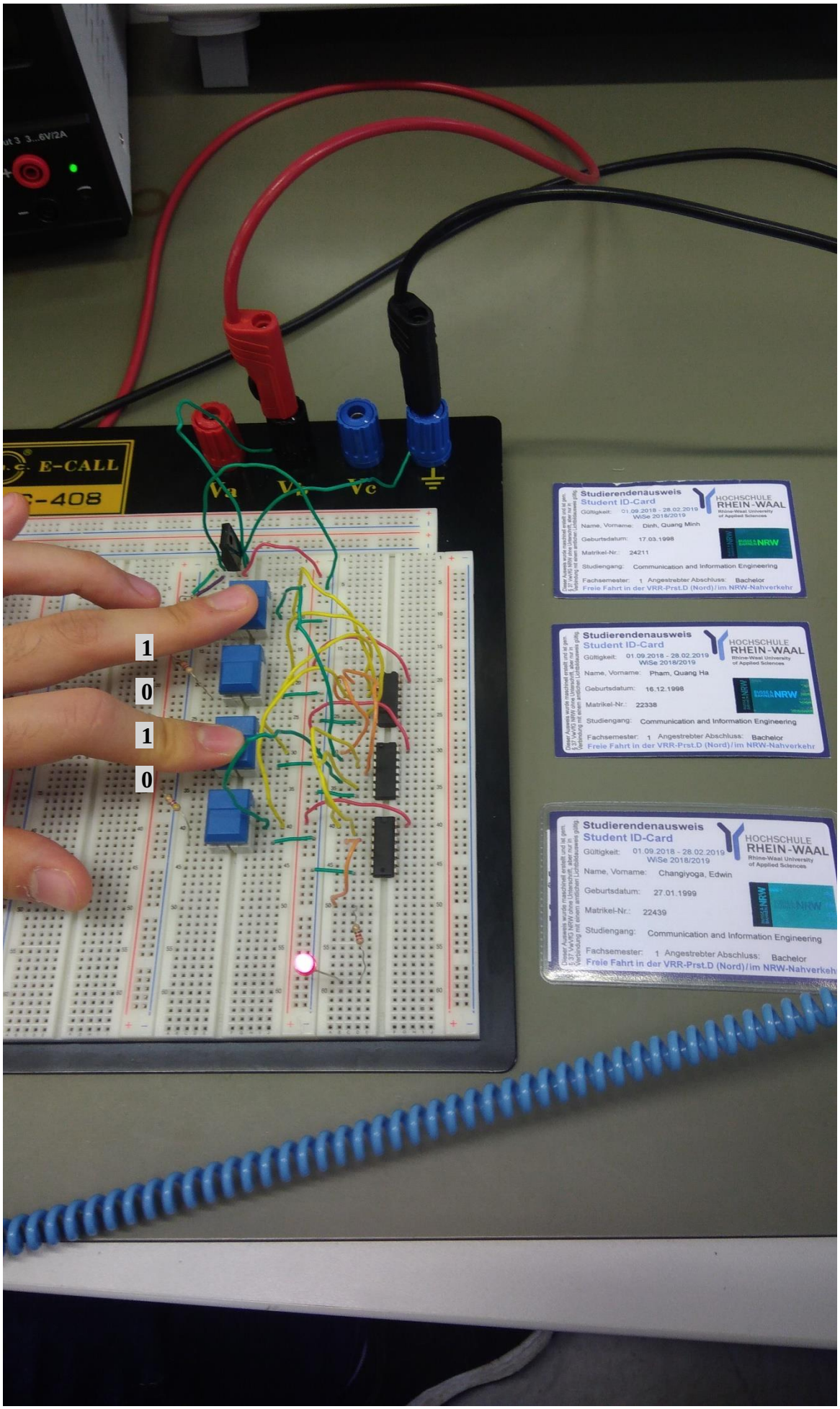
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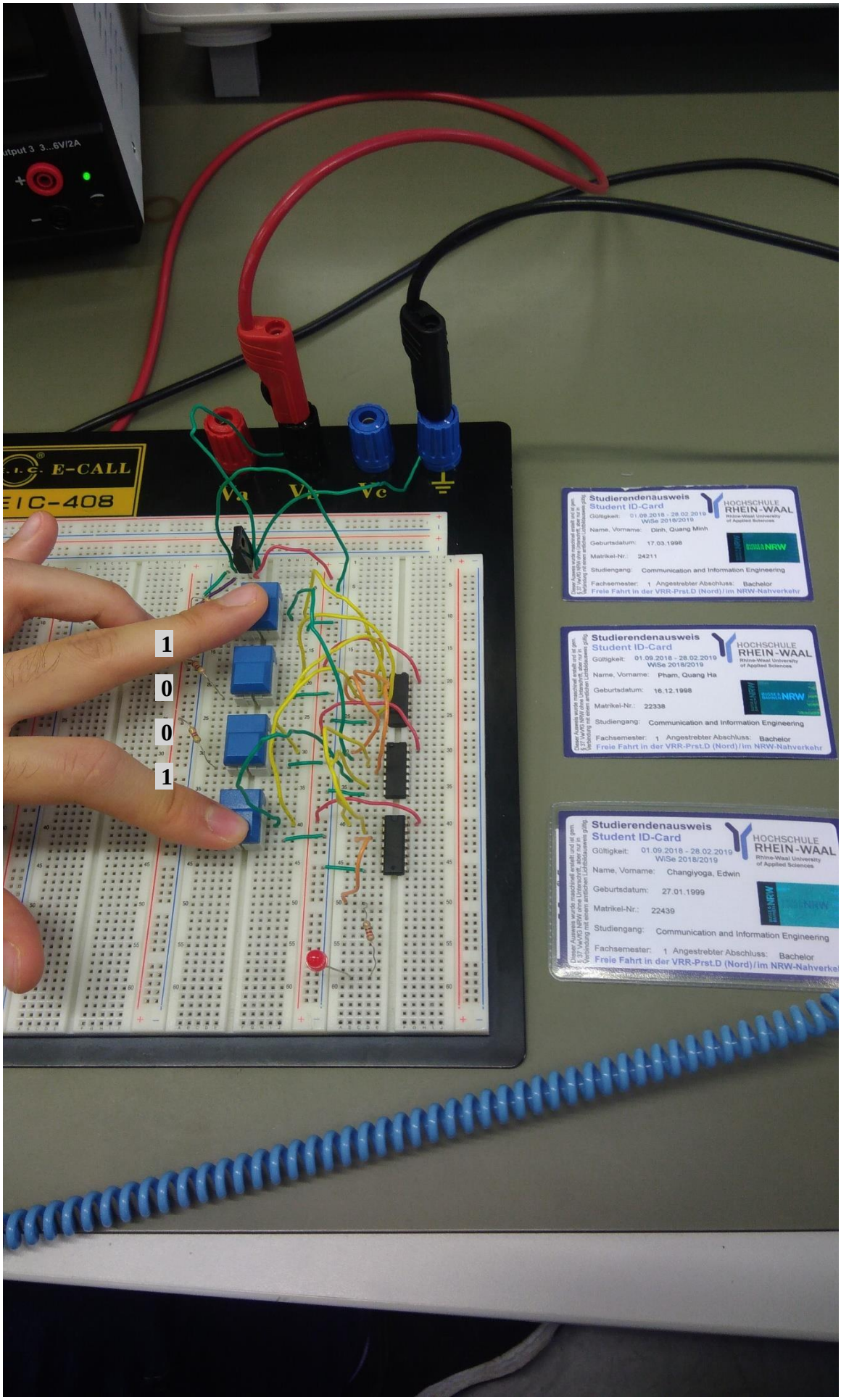
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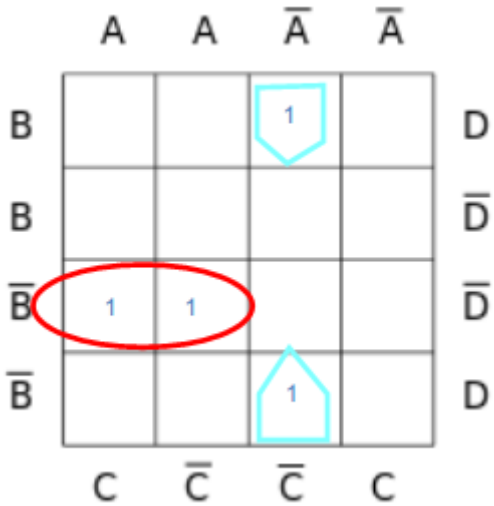
Result:

After testing our circuit by checking the output signal for all input combinations, the results we got were the same to our initial truth table. We only took 11 pictures out of 16 possible cases because the last 5 output cases have a logic output of 0.

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Table 1: Initial truth table for the control circuit



$(\neg A \wedge \neg C \wedge D) \vee (A \wedge \neg B \wedge \neg D)$

Figure 3: KV-Diagram used to simplify the circuit