Jinghao Ding

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EDUCATION

Southwest University of Science and Technology *Expected Jun. 2024*
Master of Electronic Information *GPA: 3.71/5.0*

Heilongjiang University of Science and Technology *Sep. 2016 - Jun. 2020*
Bachelor of Software Engineering *GPA: 3.79/5.0*

RESEARCH EXPERIENCE

Southwest University of Science and Technology *2021 - 2023*

- **Global Placement: Simultaneous Analytic Placement and Clock Tree Synthesis for Power Demand Balancing Between Clock and Signal Nets.**
  - Extend the original placement objective of wirelength towards power consumption.
  - Propose a gradient approximation heuristic through summation of clock wirelength gradient along each root-to-leaf path with weighting adjustment.
  - Validate the effectiveness of the proposed algorithm with 45.1% reduction on clock wirelength and 12.7% reduction on switching power compared to our baseline placer RePlAce.
- **Clock Tree Synthesis: Reducing Time Complexity for Nearest Neighbor Selection in Clock Tree Construction.**
  - Develop a *multi-grid search* strategy for clock tree merging candidates, the time complexity for constructing a complete tree has been optimized from $O(n^2logn)$ to $O(nlogn + k^2n)$.
- **Detailed Placement: Algorithm for Resolving Both Inter- and Intra-Row MIA Violations.**
  - Assist senior colleagues in developing a minimum-implant-area (MIA) aware detailed placement algorithm for multi-row-height standard cells.
  - Contributed to develop an enhancement to the legalization framework OpenDP with significant wirelength improvement achieved.
- **Global Routing: Optimizing Maze Routing Algorithm.**
  - Assist senior colleagues in developing a parallel maze router featuring bidirectional path search and dynamic routing scheduling.
  - Contributed to implement a competitive dynamic scheduling strategy, synchronize the usage of global routing resources, and resolve conflicts between the winning routing thread and other routing threads.

PUBLICATION

- **Jinghao Ding**, Linhao Lu, Zhaoqi Fu, Jie Ma, Yuanrui Qi, Mengshi Gong, and Wenxin Yu, "**Clock Aware Low Power Placement**", The 42th IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), San Francisco, CA, USA, Oct. 29 - Nov. 2, 2023 (In Press).

TECHNICAL SKILLS

- **Programming** C/C++, Python, Java, Tcl
- **Toolkits** PyTorch, Git, LaTeX
- **Languages** English (Fluent), Mandarin (Native)

AWARD

- **National Scholarship**×2 years Heilongjiang University of Science and Technology, 2017-2018
- **National Encouragement Scholarship** Heilongjiang University of Science and Technology, 2019
- **First-grade Academic Scholarship**×3 years Heilongjiang University of Science and Technology, 2017-2019