ADC register map

The following table summarizes the ADC registers.

Table 49. ADC global register map

Offset	Register
0x000 - 0x058	ADC
0x05C - 0x2FC	Reserved
0x300 - 0x304	Common registers

Table 50. ADC register map and reset values

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_SR	Reserved																						JCNR	RCNR	Reserved	ADONS	OVR	STRT	JSTRT	JEOC	EOC	AWD
Reset value																							0	0		0	0	0	0	0	0	0
ADC_CR1	Reserved					OVRIE	RES[1:0]		AWDEN	JAWDEN	Reserved				PDI	PDD	DISC NUM [2:0]			JDISCEN	DISCEN	JAUTO	AWD SGL	SCAN	JEOCIE	AWDIE	EOCIE	AWDCH[4:0]				
Reset value						0	0	0	0	0					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_CR2	Reserved	SWSTART	EXTEN[1:0]		EXTSEL [3:0]				Reserved	JSWSTART	JEXTEN[1:0]		JEXTSEL [3:0]				Reserved				ALIGN	EOCS	DDS	DMA	Reserved	DELS[2:0]			Reserved	ADC_CFG	CONT	ADON
Reset value		0	0	0	0	0	0	0		0	0	0	0	0	0	0					0	0		0		0	0	0		0	0	0
ADC_SMPR1	Sample time bits SMPx_x																															
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_SMPR2	Sample time bits SMPx_x																															
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_SMPR3	Sample time bits SMPx_x																															
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_JOFR1	Reserved																				JOFFSET1[11:0]											
Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
ADC_JOFR2	Reserved																				JOFFSET2[11:0]											
Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
ADC_JOFR3	Reserved																				JOFFSET3[11:0]											
Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
ADC_JOFR4	Reserved																				JOFFSET4[11:0]											
Reset value																					0	0	0	0	0	0	0	0	0	0	0	0
ADC_HTR	Reserved																				HT[11:0]											
Reset value																					1	1	1	1	1	1	1	1	1	1	1	1
ADC_LTR	Reserved																				LT[11:0]											
Reset value																					0	0	0	0	0	0	0	0	0	0	0	0

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_SQR1	Reserved							L[4:0]					Regular channel sequence SQx_x bits																			
Reset value								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_SQR2	Reserved		Regular channel sequence SQx_x bits																													
Reset value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_SQR3	Reserved		Regular channel sequence SQx_x bits																													
Reset value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_SQR4	Reserved		Regular channel sequence SQx_x bits																													
Reset value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_SQR5	Reserved		Regular channel sequence SQx_x bits																													
Reset value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_JSQR	Reserved										JL[1:0]		Injected channel sequence JSQx_x bits																			
Reset value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_JDR1	Reserved																JDATA[15:0]															
Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_JDR2	Reserved																JDATA[15:0]															
Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_JDR3	Reserved																JDATA[15:0]															
Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_JDR4	Reserved																JDATA[15:0]															
Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_DR	Reserved																Regular DATA[15:0]															
Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADC_SMPR0	Sample time bits SMPx_x																															
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 51. ADC register map and reset values (common registers)

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_CSR	Reserved																									ADONS	OVR	STRT	JSTRT	JEOC	EOC	AWD
Reset value																										0	0	0	0	0	0	0
	ADC1																															
ADC_CCR	Reserved								TSVREFE	Reserved							ADCPRE		Reserved													
Reset value									0								0	0														

ADC status register (ADC_SR)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							JCNR	RCNR	Reserved	ADONS	OVR	STRT	JSTRT	JEOC	EOC	AWD
							r	r		r	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Bits 31:10 Reserved, must be kept at reset value

Bit 9 **JCNR:** Injected channel not ready

This bit is set and cleared by hardware after the JSQR register is written. It indicates if a new injected conversion can be launched (by setting the JSWSTART bit).

0: Injected channel ready

1: Injected channel not ready, JSWSTART must not be set

Bit 8 **RCNR:** Regular channel not ready

This bit is set and cleared by hardware after one of the SQRx register is written or after the OVR bit is cleared. It indicates if a new regular conversion can be launched (by setting the SWSTART bit).

0: Regular channel ready

1: Regular channel not ready, SWSTART must not be set

Bit 7 Reserved, must be kept at reset value

Bit 6 **ADONS:** ADC ON status

This bit is set and cleared by hardware to indicate if the ADC is ready to convert.

0: The ADC is not ready

1: The ADC is ready to convert. External triggers can be enabled, the SWSTART and JSWSTART bits can be set

Bit 5 **OVR:** Overrun

This bit is set by hardware when regular conversion data are lost. It is cleared by software. Overrun detection is enabled only when DMA = 1 or EOCS = 1.

0: No overrun occurredF

1: Overrun has occurred

Bit 4 **STRT:** Regular channel start flag

This bit is set by hardware when regular channel conversion starts. It is cleared by software.

0: No regular channel conversion started

1: Regular channel conversion has started

Bit 3 **JSTRT:** Injected channel start flag

This bit is set by hardware when injected group conversion starts. It is cleared by software.

0: No injected group conversion started

1: Injected group conversion has started

Bit 2 **JEOC:** Injected channel end of conversion

This bit is set by hardware at the end of the conversion of all injected channels in the group. It is cleared by software.

0: Conversion is not complete

1: Conversion complete

Bit 1 **EOC:** Regular channel end of conversion

This bit is set by hardware at the end of the conversion of a regular group of channels. It is cleared by software or by reading the ADC_DR register.

0: Conversion not complete (EOCS=0), or sequence of conversions not complete (EOCS=1)

1: Conversion complete (EOCS=0), or sequence of conversions complete (EOCS=1)

Bit 0 **AWD:** Analog watchdog flag

This bit is set by hardware when the converted voltage crosses the values programmed in the ADC_LTR and ADC_HTR registers. It is cleared by software.

0: No analog watchdog event occurred

1: Analog watchdog event occurred

11.15.2 ADC control register 1 (ADC_CR1)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					OVRIE	RES[1:0]		AWDEN	JAWDEN	Reserved				PDI	PDD
					rw	rw	rw	rw	rw					rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISCNUM[2:0]			JDISCEN	DISCEN	JAUTO	AWDSGL	SCAN	JEOCIE	AWDIE	EOCIE	AWDCH[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:27 Reserved, must be kept at reset value

Bit 26 **OVRIE:** Overrun interrupt enable

This bit is set and cleared by software to enable/disable the Overrun interrupt.
0: Overrun interrupt disabled
1: Overrun interrupt enabled. An interrupt is generated when the OVR bit is set.

Bits 25:24 **RES[1:0]**: Resolution

These bits are written by software to select the resolution of the conversion.
00: 12-bit (T_{CONV} = 12 ADCCLK cycles)
01: 10-bit (T_{CONV} = 11 ADCCLK cycles)
10: 8-bit (T_{CONV} = 9 ADCCLK cycles)
11: 6-bit (T_{CONV} = 7 ADCCLK cycles)
This bit must be written only when ADON=0.

Bit 23 **AWDEN:** Analog watchdog enable on regular channels

This bit is set and cleared by software.
0: Analog watchdog disabled on regular channels
1: Analog watchdog enabled on regular channels

Bit 22 **JAWDEN:** Analog watchdog enable on injected channels

This bit is set and cleared by software.
0: Analog watchdog disabled on injected channels
1: Analog watchdog enabled on injected channels

Bits 21:18 Reserved, must be kept at reset value

Bit 17 **PDI:** Power down during the idle phase

This bit is written and cleared by software. When ADON=1, it determines whether the ADC is powered up or down when not converting (waiting for a hardware or software trigger event).
0: The ADC is powered up when waiting for a start event
1: The ADC is powered down when waiting for a start event
Note: This bit must be written only when ADON=0.

Bit 16 **PDD:** Power down during the delay phase

This bit is written and cleared by software. When ADON=1, it determines whether the ADC is powered up or down between 2 conversions (or sequences of conversions) when a delay is inserted (DELS bits).
0: The ADC is powered up during the delay
1: The ADC is powered down during the delay
Note: This bit must be written only when ADON=0.

Bits 15:13 **DISCNUM[2:0]:** Discontinuous mode channel count

These bits are written by software to define the number of channels to be converted in discontinuous mode, after receiving an external trigger.

000: 1 channel

001: 2 channels

...

111: 8 channels

Note: This bit must be written only when ADON=0.

Bit 12 **JDISCEN:** Discontinuous mode on injected channels

This bit is set and cleared by software to enable/disable discontinuous mode on the injected channels of a group.

0: Discontinuous mode on injected channels disabled

1: Discontinuous mode on injected channels enabled

Note: This bit must be written only when ADON=0.

Bit 11 **DISCEN:** Discontinuous mode on regular channels

This bit is set and cleared by software to enable/disable Discontinuous mode on regular channels.

0: Discontinuous mode on regular channels disabled

1: Discontinuous mode on regular channels enabled

Note: This bit must be written only when ADON=0.

Bit 10 **JAUTO:** Automatic injected group conversion

This bit is set and cleared by software to enable/disable automatic injected group conversion after regular group conversion.

0: Automatic injected group conversion disabled

1: Automatic injected group conversion enabled

Note: This bit must be written only when ADON=0.

Bit 9 **AWDSGL:** Enable the watchdog on a single channel in scan mode

This bit is set and cleared by software to enable/disable the analog watchdog on the channel identified by the AWDCH[4:0] bits.

0: Analog watchdog enabled on all channels

1: Analog watchdog enabled on a single channel

Bit 8 **SCAN**: Scan mode

This bit is set and cleared by software to enable/disable the Scan mode. In the Scan mode, the inputs selected through the ADC_SQRx or ADC_JSQRx registers are converted.

0: Scan mode disabled

1: Scan mode enabled

Note: This bit must be written only when ADON=0.

Bit 7 **JEOCIE:** Interrupt enable for injected channels

This bit is set and cleared by software to enable/disable the end of conversion interrupt for injected channels.

0: JEOC interrupt disabled

1: JEOC interrupt enabled. An interrupt is generated when the JEOC bit is set.

Bit 6 **AWDIE:** Analog watchdog interrupt enable

This bit is set and cleared by software to enable/disable the analog watchdog interrupt. In Scan mode if the watchdog thresholds are crossed, scan is aborted only if this bit is enabled.
0: Analog watchdog interrupt disabled
1: Analog watchdog interrupt enabled

Bit 5 **EOCIE:** Interrupt enable for EOC

This bit is set and cleared by software to enable/disable the end of conversion interrupt.
0: EOC interrupt disabled
1: EOC interrupt enabled. An interrupt is generated when the EOC bit is set.

Bits 4:0 **AWDCH[4:0]:** Analog watchdog channel select bits

These bits are set and cleared by software. They select the input channel to be guarded by the analog watchdog.
00000: ADC analog input Channel0
00001: ADC analog input Channel1
...

11000: ADC analog input Channel24
11001: ADC analog input Channel25
11010: ADC analog input Channel26
Other values reserved.

Note: ADC1 analog inputs Channel16, Channel 17 and Channel26 are internally connected to the temperature sensor, to V_{REFINT} and to V_{COMP} respectively.

11.15.3 ADC control register 2 (ADC_CR2)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	SWSTART	EXTEN		EXTSEL[3:0]				Reserved	JSWSTART	JEXTEN		JEXTSEL[3:0]			
	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				ALIGN	EOCS	DDS	DMA	Res.	DELS			Res.	ADC_CFG	CONT	ADON
				rw	rw	rw	rw		rw	rw	rw		rw	rw	rw

Bit 31 Reserved, must be kept at reset value

Bit 30 **SWSTART:** Start conversion of regular channels

This bit is set by software to start conversion and cleared by hardware as soon as the conversion starts.
0: Reset state
1: Starts conversion of regular channels

Note: This bit must be set only when ADONS=1 and RCNR=0.

Bits 29:28 **EXTEN:** External trigger enable for regular channels

These bits are set and cleared by software to select the external trigger polarity and enable the trigger of a regular group.

00: Trigger detection disabled
01: Trigger detection on the rising edge
10: Trigger detection on the falling edge
11: Trigger detection on both the rising and falling edges

Note: The external trigger must be enabled only when ADONS=1.

Bits 27:24 **EXTSEL[3:0]:** External event select for regular group

These bits select the external event used to trigger the start of conversion of a regular group:

0000: TIM9_CC2 event
0001: TIM9_TRGO event
0010: TIM2_CC3 event
0011: TIM2_CC2 event
0100: TIM3_TRGO event
0101: TIM4_CC4 event
0110: TIM2_TRGO event
0111: TIM3_CC1 event
1000: TIM3_CC3 event
1001: TIM4_TRGO event
1010: TIM6_TRGO event
1011: Reserved
1100: Reserved
1101: Reserved
1110: Reserved
1111: EXTI line11

Bit 23 Reserved, must be kept at reset value

Bit 22 **JSWSTART:** Start conversion of injected channels

This bit is set by software and cleared by hardware as soon as the conversion starts.

0: Reset state
1: Starts conversion of injected channels

Note: This bit must be set only when ADONS=1 and JCNR=0.

Bits 21:20 **JEXTEN:** External trigger enable for injected channels

These bits are set and cleared by software to select the external trigger polarity and enable the trigger of an injected group.

00: Trigger detection disabled
01: Trigger detection on the rising edge
10: Trigger detection on the falling edge
11: Trigger detection on both the rising and falling edges

Note: The external trigger must be enabled only when ADONS=1.

Bits 19:16 **JEXTSEL[3:0]:** External event select for injected group

These bits select the external event used to trigger the start of conversion of an injected group.

0000: TIM9_CC1 event
0001: TIM9_TRGO event
0010: TIM2_TRGO event
0011: TIM2_CC1 event
0100: TIM3_CC4 event
0101: TIM4_TRGO event
0110: TIM4_CC1 event
0111: TIM4_CC2 event
1000: TIM4_CC3 event
1001: TIM10_CC1 event
1010: TIM7_TRGO event
1011: Reserved
1100: Reserved
1101: Reserved
1110: Reserved
1111: EXTI line15

Bits 15:12 Reserved, must be kept at reset value

Bit 11 **ALIGN:** Data alignment

This bit is set and cleared by software. Refer to *Figure 42* and *Figure 43*.

0: Right alignment
1: Left alignment

Bit 10 **EOCS:** End of conversion selection

This bit is set and cleared by software.

0: The EOC bit is set at the end of each sequence of regular conversions
1: The EOC bit is set at the end of each regular conversion

Bit 9 **DDS:** DMA disable selection

This bit is set and cleared by software.

0: No new DMA request is issued after the last transfer (as configured in the DMA controller)
1: DMA requests are issued as long as data are converted and DMA=1

Bit 8 **DMA:** Direct memory access mode

This bit is set and cleared by software. Refer to the DMA controller chapter for more details.

0: DMA mode disabled
1: DMA mode enabled

Bit 7 Reserved, must be kept at reset value

Bit 6:4 **DELS:** Delay selection

These bits are set and cleared by software. They define the length of the delay which is applied after a conversion or a sequence of conversions.

000: No delay

001: Until the converted data have been read (DR read or EOC=0 for regular conversions, JEOC=0 for injected conversions)

010: 7 APB clock cycles after the end of conversion

011: 15 APB clock cycles after the end of conversion

100: 31 APB clock cycles after the end of conversion

101: 63 APB clock cycles after the end of conversion

110: 127 APB clock cycles after the end of conversion

111: 255 APB clock cycles after the end of conversion

Note: 1- This bit must be written only when ADON=0.

2- Due to clock domain crossing, a latency of 2 or 3 ADC clock cycles is added to the delay before a new conversion can start.

3- The delay required for a given frequency ratio between the APB clock and the ADC clock depends on the activity on the AHB and APB busses. If the ADC is the only peripheral that needs to transfer data, then a minimum delay should be configured: 15 APB clock cycles if $f_{APB} < f_{ADCCLK}/2$ or else 7 APB clock cycles if $f_{APB} < f_{ADCCLK}$, otherwise no delay is needed.

Bit 3 Reserved, must be kept at reset value

Bit 2 **ADC_CFG:** ADC configuration

This bit is set and cleared by software. It selects the bank of channels to be converted.

0: Bank A selected

1: Bank B selected

Note: This bit must be modified only when no conversion is on going.

This bit is available in high and medium+ density devices only

Bit 1 **CONT:** Continuous conversion

This bit is set and cleared by software. If it is set, conversion takes place continuously until it is cleared.

0: Single conversion mode

1: Continuous conversion mode

Bit 0 **ADON:** A/D Converter ON / OFF

This bit is set and cleared by software.

0: Disable ADC conversion and go to power down mode

1: Enable ADC: conversions can start as soon as a start event (hardware or software) is received. When not converting, the ADC goes to the power up or power down mode depending on the PDI and PDD bits.

Note: This bit must be set only when ADONS=0 and cleared only when ADONS=1.

11.15.4 ADC sample time register 1 (ADC_SMPR1)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SMP29[2:0]			SMP28[2:0]			SMP27[2:0]			SMP26[2:0]			SMP25[2:1]	
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP25[0]	SMP24[2:0]			SMP23[2:0]			SMP22[2:0]			SMP21[2:0]			SMP20[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31: 30 Reserved, must be kept at reset value

Bits 29:0 **SMPx[2:0]:** Channel x sampling time selection

These bits are written by software to select the sampling time individually for each channel. During sampling cycles, the channel selection bits must remain unchanged.

000: 4 cycles
001: 9 cycles
010: 16 cycles
011: 24 cycles
100: 48 cycles
101: 96 cycles
110: 192 cycles
111: 384 cycles

Note: These bits must be written only when ADON=0.

11.15.5 ADC sample time register 2 (ADC_SMPR2)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SMP19[2:0]			SMP18[2:0]			SMP17[2:0]			SMP16[2:0]			SMP15[2:1]	
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP15[0]	SMP14[2:0]			SMP13[2:0]			SMP12[2:0]			SMP11[2:0]			SMP10[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:30 Reserved, must be kept at reset value

Bits 29:0 **SMPx[2:0]:** Channel x sampling time selection

These bits are written by software to select the sampling time individually for each channel. During sample cycles, the channel selection bits must remain unchanged.

000: 4 cycles
001: 9 cycles
010: 16 cycles
011: 24 cycles
100: 48 cycles
101: 96 cycles
110: 192 cycles
111: 384 cycles

Note: These bits must be written only when ADON=0.

11.15.6 ADC sample time register 3 (ADC_SMPR3)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SMP9[2:0]			SMP8[2:0]			SMP7[2:0]			SMP6[2:0]			SMP5[2:1]	
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP5[0]	SMP4[2:0]			SMP3[2:0]			SMP2[2:0]			SMP1[2:0]			SMP0[2:0]		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:30 Reserved, must be kept at reset value

Bits 29:0 **SMPx[2:0]:** *Channel x Sample time selection*

These bits are written by software to select the sampling time individually for each channel. During the sampling cycles, the channel selection bits must remain unchanged.

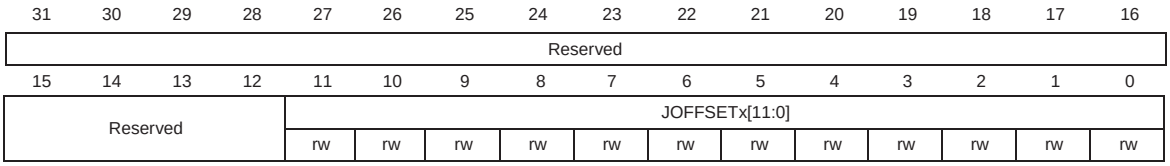
000: 4 cycles
001: 9 cycles
010: 16 cycles
011: 24 cycles
100: 48 cycles
101: 96 cycles
110: 192 cycles
111: 384 cycles

Note: These bits must be written only when ADON=0.

11.15.7 ADC injected channel data offset register x (ADC_JOFRx)(x=1..4)

Address offset: 0x18-0x24

Reset value: 0x0000 0000



Bits 31:12 Reserved, must be kept at reset value

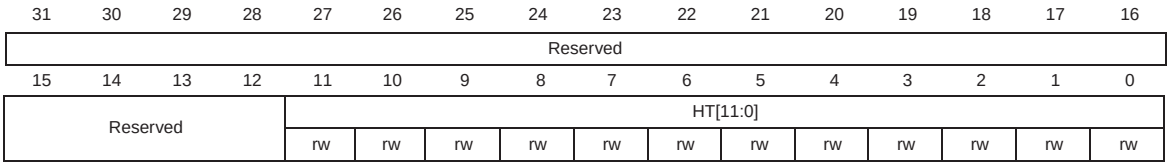
Bits 11:0 **JOFFSETx[11:0]:** Data offset for injected channel x

These bits are written by software to define the offset to be subtracted from the raw converted data when converting injected channels. The conversion result can be read from in the ADC_JDRx registers.

11.15.8 ADC watchdog higher threshold register (ADC_HTR)

Address offset: 0x28

Reset value: 0x0000 0FFF



Bits 31:12 Reserved, must be kept at reset value

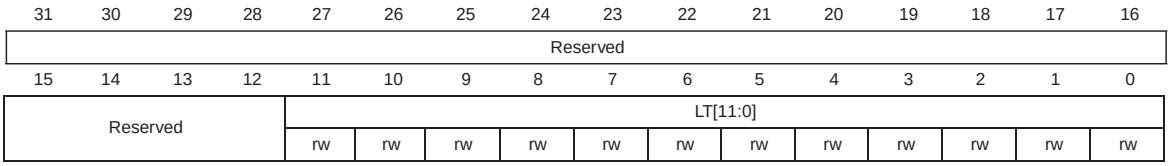
Bits 11:0 **HT[11:0]:** Analog watchdog higher threshold

These bits are written by software to define the higher threshold for the analog watchdog.

11.15.9 ADC watchdog lower threshold register (ADC_LTR)

Address offset: 0x2C

Reset value: 0x0000 0000



Bits 31:12 Reserved, must be kept at reset value

Bits 11:0 **LT[11:0]:** Analog watchdog lower threshold

These bits are written by software to define the lower threshold for the analog watchdog.

11.15.10 ADC regular sequence register 1 (ADC_SQR1)

Address offset: 0x30

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved							L[4:0]					SQ28[4:1]			
							rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ28[0]	SQ27[4:0]						SQ26[4:0]					SQ25[4:0]			
rw	rw	rw	rw	rw	rw	rw	rw				rw	rw	rw	rw	rw

Bits 31:25 Reserved, must be kept at reset value

Bits 24:20 **L[4:0]:** Regular channel sequence length

These bits are written by software to define the total number of conversions in the regular channel conversion sequence.

00000: 1 conversion
00001: 2 conversions
...
11010: 27 conversions
11011: 28 conversions (applicable in high and medium+ density devices only)

Bits 19:15 **SQ28[4:0]:** 28th conversion in regular sequence

These bits are written by software with the channel number (0..31) assigned as the 28th in the conversion sequence. The channel is selected in bank A or bank B depending on the ADC_CFG bit in the ADC_CR2 register.

Note: These bits are available in high and medium+ density devices only

Bits 14:10 **SQ27[4:0]:** 27th conversion in regular sequence

Medium density devices: These bits are written by software with the channel number (0..26) assigned as the 27th in the conversion sequence.

High and medium+ density devices: 27th conversion in regular sequence

Bits 9:5 **SQ26[4:0]:** 26th conversion in regular sequence

Bits 4:0 **SQ25[4:0]:** 25th conversion in regular sequence

11.15.11 ADC regular sequence register 2 (ADC_SQR2)

Address offset: 0x34

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ24[4:0]					SQ23[4:0]					SQ22[4:1]			
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ22[0]	SQ21[4:0]						SQ20[4:0]					SQ19[4:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:30 Reserved, must be kept at reset value

Bits 29:26 **SQ24[4:0]:** 24th conversion in regular sequence
These bits are written by software with the channel number (0.31) assigned as the 24th in the sequence to be converted.

Bits 24:20 **SQ23[4:0]:** 23rd conversion in regular sequence

Bits 19:15 **SQ22[4:0]:** 22nd conversion in regular sequence

Bits 14:10 **SQ21[4:0]:** 21st conversion in regular sequence

Bits 9:5 **SQ20[4:0]:** 20th conversion in regular sequence

Bits 4:0 **SQ19[4:0]:** 19th conversion in regular sequence

11.15.12 ADC regular sequence register 3 (ADC_SQR3)

Address offset: 0x38

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ18[4:0]					SQ17[4:0]					SQ16[4:1]			
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ16[0]	SQ15[4:0]						SQ14[4:0]					SQ13[4:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:30 Reserved, must be kept at reset value

Bits 29:25 **SQ18[4:0]:** 18th conversion in regular sequence
These bits are written by software with the channel number (0..31) assigned as the 18th in the sequence to be converted.

Bits 24:20 **SQ17[4:0]:** 17th conversion in regular sequence

Bits 19:15 **SQ16[4:0]:** 16th conversion in regular sequence

Bits 14:10 **SQ15[4:0]:** 15th conversion in regular sequence

Bits 9:5 **SQ14[4:0]:** 14th conversion in regular sequence

Bits 4:0 **SQ13[4:0]:** 13th conversion in regular sequence

11.15.13 ADC regular sequence register 4 (ADC_SQR4)

Address offset: 0x3C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ12[4:0]					SQ11[4:0]					SQ10[4:1]			
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ10[0]		SQ9[4:0]					SQ8[4:0]					SQ7[4:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:30 Reserved, must be kept at reset value

Bits 29:26 **SQ12[4:0]**: 12th conversion in regular sequence
These bits are written by software with the channel number (0..31) assigned as the 12th in the sequence to be converted.

Bits 24:20 **SQ11[4:0]**: 11th conversion in regular sequence

Bits 19:15 **SQ10[4:0]**: 10th conversion in regular sequence

Bits 14:10 **SQ9[4:0]:** 9th conversion in regular sequence

Bits 9:5 **SQ8[4:0]**: 8th conversion in regular sequence

Bits 4:0 **SQ7[4:0]**: 7th conversion in regular sequence

11.15.14 ADC regular sequence register 5 (ADC_SQR5)

Address offset: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ6[4:0]					SQ5[4:0]					SQ4[4:1]			
		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ4_0		SQ3[4:0]					SQ2[4:0]					SQ1[4:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:30 Reserved, must be kept at reset value

Bits 29:25 **SQ6[4:0]**: 6th conversion in regular sequence
These bits are written by software with the channel number (0..31) assigned as the 6th in the sequence to be converted.

Bits 24:20 **SQ5[4:0]:** 5th conversion in regular sequence

Bits 19:15 **SQ4[4:0]**: 4th conversion in regular sequence

Bits 14:10 **SQ3[4:0]**: 3rd conversion in regular sequence

Bits 9:5 **SQ2[4:0]:** 2nd conversion in regular sequence

Bits 4:0 **SQ1[4:0]**: 1st conversion in regular sequence

11.15.15 ADC injected sequence register (ADC_JSQR)

Address offset: 0x44

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										JL[1:0]		JSQ4[4:1]			
										rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JSQ4[0]	JSQ3[4:0]					JSQ2[4:0]					JSQ1[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:22 Reserved, must be kept at reset value

Bits 21:20 **JL[1:0]:** Injected sequence length

These bits are written by software to define the total number of conversions in the injected channel conversion sequence.

00: 1 conversion
01: 2 conversions
10: 3 conversions
11: 4 conversions

Bits 19:15 **JSQ4[4:0]:** 4th conversion in injected sequence (when JL[1:0]=3, see note below)

These bits are written by software with the channel number (0..31) assigned as the 4th in the sequence to be converted. The channel is selected in bank A or bank B depending on the ADC_CFG bit in the ADC_CR2 register.

Bits 14:10 **JSQ3[4:0]:** 3rd conversion in injected sequence (when JL[1:0]=3, see note below)

Bits 9:5 **JSQ2[4:0]:** 2nd conversion in injected sequence (when JL[1:0]=3, see note below)

Bits 4:0 **JSQ1[4:0]:** 1st conversion in injected sequence (when JL[1:0]=3, see note below)

Note: When JL[1:0]=3 (4 injected conversions in the sequencer), the ADC converts the channels in the following order: JSQ1[4:0], JSQ2[4:0], JSQ3[4:0], and JSQ4[4:0].

When JL=2 (3 injected conversions in the sequencer), the ADC converts the channels in the following order: JSQ2[4:0], JSQ3[4:0], and JSQ4[4:0].

When JL=1 (2 injected conversions in the sequencer), the ADC converts the channels in starting from JSQ3[4:0], and then JSQ4[4:0].

When JL=0 (1 injected conversion in the sequencer), the ADC converts only JSQ4[4:0] channel.

11.15.16 ADC injected data register x (ADC_JDRx) (x= 1..4)

Address offset: 0x48 - 0x54

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JDATA[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 31:16 Reserved, must be kept at reset value

Bits 15:0 **JDATA[15:0]:** Injected data

These bits are read-only. They contain the conversion result from injected channel x. The data are left -or right-aligned as shown in *Figure 42* and *Figure 43*.

11.15.17 ADC regular data register (ADC_DR)

Address offset: 0x58

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 31:16 Reserved.

Bits 15:0 **DATA[15:0]:** Regular data

These bits are read-only. They contain the conversion result from the regular channels. The data are left- or right-aligned as shown in *Figure 42* and *Figure 43*.

11.15.18 ADC sample time register 0 (ADC_SMPR0)

Address offset: 0x5C

Reset value: 0x0000 0000

Note: This register is available in high and medium+ density devices only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										SMP31[2:0]			SMP30[2:0]		
										rw	rw	rw	rw	rw	rw

Bits 31:6 Reserved, must be kept at reset value

Bits 5:0 **SMPx[2:0]:** *Channel x Sample time selection*

These bits are written by software to select the sampling time individually for each channel. During the sampling cycles, the channel selection bits must remain unchanged.

000: 4 cycles
001: 9 cycles
010: 16 cycles
011: 24 cycles
100: 48 cycles
101: 96 cycles
110: 192 cycles
111: 384 cycles

Note: These bits must be written only when ADON=0.

11.15.19 ADC common status register (ADC_CSR)

Address offset: 0x00 (this offset address is relative to the base address of ADC common registers, i.e. 0x300)

Reset value: 0x0000 0000

This register provides an image of the status bits of the different ADCs. Nevertheless it is read-only and does not allow to clear the different status bits. Instead each status bit must be cleared by writing it to 0 in the corresponding ADC_SR register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									ADONS1	OVR1	STRT1	JSTRT1	JEOC 1	EOC1	AWD1
									r	r	r	r	r	r	r

Bits 31:7 Reserved, must be kept at reset value

Bit 6 **ADONS1:** *ADON Status of ADC1*
This bit is a copy of the ADONS bit in the ADC_SR register.

Bit 5 **OVR1:** Overrun flag of the ADC
This bit is a copy of the OVR bit in the ADC_SR register.

Bit 4 **STRT1:** Regular channel Start flag of the ADC
This bit is a copy of the STRT bit in the ADC_SR register.

Bit 3 **JSTRT1:** Injected channel Start flag of the ADC
This bit is a copy of the JSTRT bit in the ADC_SR register.

Bit 2 **JEOC1:** Injected channel end of conversion of the ADC
This bit is a copy of the JEOC bit in the ADC_SR register.

Bit 1 **EOC1:** End of conversion of the ADC
This bit is a copy of the EOC bit in the ADC_SR register.

Bit 0 **AWD1:** Analog watchdog flag of the ADC
This bit is a copy of the AWD bit in the ADC_SR register.

11.15.20 ADC common control register (ADC_CCR)

Address offset: 0x04 (this offset address is relative to the base address of ADC common registers, i.e. 0x300)

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								TSVREFE	Reserved					ADCPRE[1:0]	
								rw						rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															

Bits 31:24 Reserved, must be kept at reset value

Bit 23 **TSVREFE:** Temperature sensor and V_{REFINT} enable

This bit is set and cleared by software to enable/disable the temperature sensor and the V_{REFINT} channel.

0: Temperature sensor and V_{REFINT} channel disabled

1: Temperature sensor and V_{REFINT} channel enabled

Bits 22:18 Reserved, must be kept at reset value

Bits 17:16 **ADCPRE:** ADC prescaler

Set and cleared by software to select the frequency of the clock to the ADC.

00: HSI divided by 1

01: HSI divided by 2

10: HSI divided by 4

11: Reserved

Bits 15:0 Reserved, must be kept at reset value