Paper Code : PCC- CS302/PCC-CS302/PCCCS302 Computer Organisation UPID : 003444

Group A

(I) **What are the different categories of memory/storage?**
Ans. Primary and Secondary

(II) **Write one advantage of pipelining.**
Ans. It reduces processor's cycle time.

(III) **Which type of program acts as an intermediary between a user of a computer and the computer hardware?**
Ans. Operating System

(IV) **The 2's complement of 15 is _____.**
Ans. 0001

(V) **Name some types of devices used for Auxiliary Memory.**
Ans. Magnetic Tapes, Magnetic Disks, Floppy Disks, Hard Disks and Drives, CD-ROM

(VI) **What is interpreter ?**
Ans. Translates at a time only one high level language instruction into machine level language.

(VII) **What is the functions of the operating system?**
Ans. An operating system is a piece of software that manages files, manages memory, manages processes, handles input and output, and controls peripheral devices like disk drives and printers, among other things.

(VIII) **Carry, Overflow are also called _____.**
Ans. Flag

(IX) **Which memory has the fastest speed in the computer memory hierarchy?**
Ans. Internal memory or Registers

(X) **What is the full form of CISC?**
Ans. Complex Instruction Set Computer

(XI) **Which bus is bidirectional ?**
Ans. Data Bus

(XII) **Which algorithms are based on add/subtract and shift category ?**
Ans. Restoring Division, Non Restoring Division, Booth's Multiplication.

Group B

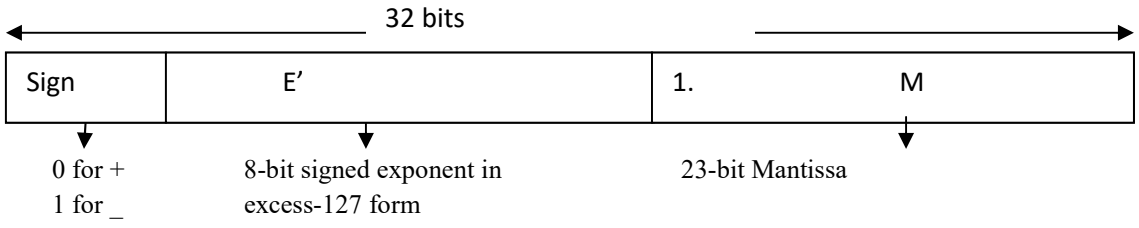
2. **What is Von Neumann bottleneck?**

Ans. Since, the CPU has much higher speed than the main memory (RAM), the CPU has to wait longer to obtain a data from the memory. This CPU – memory speed disparity is referred to as Von Neumann bottleneck. To reduce this Cache Memory and RISC was introduced.

3. **Describe IEEE 754 standard format for floating point representation.**

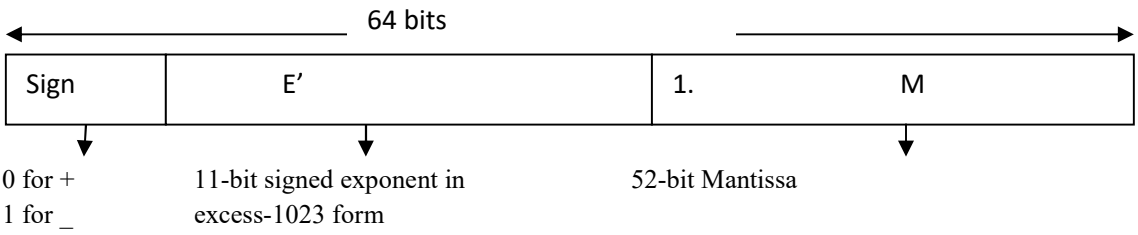
Ans. IEEE 754 standard has two formats: Single Precision Format and Double Precision Format
Single Precision Format: 32 bit format, 8bit for exponent, 23 bit for mantissa, 1 bit for sign of the number.

Value represented=$\pm 1.M \times 2^{E'-127}$



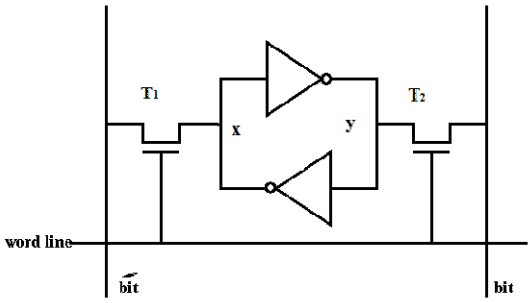
Double Precision Format:64 bit format, 11bit for exponent, 52 bit for mantissa, 1 bit for sign of the number.

Value represented=$\pm 1.Mx2^{E'-1023}$



4. Explain the reading and writing operations of a SRAM

Ans. The SRAM cell



SRAM cell is make up of 2 inverters are cross-connected to form a latch .The latch is connected to 2 bit line by transistor T1 and T2 . T1 and T2 can switch opened or closed under control of word line.When word line is ground level, the transistors are turned off and the latch retrains its state.
During the **Read Operation**, Word line is activated to close switches T1 and T2 .
If the cell is in state 1; the signal on b line is high and the signal on b' line is low.The opposite is true if the cell is in state 0.Thus, b and b' are always complements of each other's.
The sense /write circuit at the end of the two bit line monitors their state and sets the corresponding output accordingly.
While in **Write Operation** , the Sense/Write circuit drives bit lines b and b', instead of sensing their state. It places the appropriate value on bit line b and its complement on b' and activate the word line. This forces the cell into the corresponding state, which the cell retains when the word line is deactivated.

5. Explain DMA controller.

A DMA controller is a hardware device that is used to transfer data between devices without involving the CPU. It is a specialized microcontroller that acts as a mediator between the device and the memory, allowing for data to be moved quickly and efficiently. When a device such as a hard disk or network interface wants to transfer data to or from memory, it typically has to send a request to the CPU. The CPU then reads or writes the data to memory, which can be a time-consuming process, especially when dealing with large amounts of data. This is where the direct memory access controller comes in. Instead of going through the CPU, the device sends its data request directly to the direct memory access controller.

The DMA controller then takes control of the bus and begins transferring data between the device and memory. The CPU is only involved in setting up the DMA-controller and receiving an interrupt when the transfer is complete. This allows the CPU to perform other tasks while the data transfer is taking place, improving overall system performance.DMA controller operates by using DMA channels, which are specific paths for data transfer between the device and memory. These channels are programmed by the CPU with the necessary parameters, such as the source and destination addresses, and the transfer size. Once programmed, the direct memory access controller takes over and performs the data transfer autonomously. Overall, the direct memory access controller provides a faster and more efficient way of transferring data between devices and memory, reducing the load on the CPU and improving system performance.

6. Explain the concept of hand shaking in IO operation .

Two types of handshaking : Source initiated and Destination initiated

Must draw two timing diagrams for two types of handshaking (2+2)

Group C

7. What are the advantages of Carry Look Ahead(CLA) over ripple carry adder? Explain with diagram (7+8)

Ans. Discuss the principle of CLA and ripple carry adder with diagram (4+4).

Advantage of CLA over ripple carry adder in terms of speed by reduces delay to calculate the results of the larger value of the adder. The maximum delay of the n bit CLA is 6Δ but for n bit ripple carry adder is $n\Delta$. Proper explanation of calculation of this delay is required to get full marks (7).

8. Explain the concept of virtual memory. What do you understand by page fault?(8+7)

Ans. Only Virtual memory concept (3). Virtual memory concept with MMU (5).

Explain it with an example should get full marks (8).

Discuss a situation when page fault occurs should carry full marks.

9. Explain the difference between instruction pipeline and arithmetic pipeline.

Ans. First should explain in detail about instruction pipeline and arithmetic pipeline (4+4) and after that the explain the differences (7)

Instruction Pipeline	Arithmetic pipeline
1.It is used to process all type of instructions	1.It is used to process arithmetic type instructions such as addition, multiplication
2.The execution of a steam of instructions can be pipelined by overlapping the execution of the current instruction with fetch, decode and operand fetch of subsequent instructions	2.It divides an arithmetic an arithmetic operations, such as a multiply, into multiple arithmetic steps each of which is executed one-by-one in different arithmetic stages in the ALU.
3.All high performance computers are equipped with instruction pipeline.	3. the number of arithmetic pipelines varies from processor to processor

10. What is Operating System ? What are the different roles of an Operating System?

Ans. Definition of OS (5). Different roles of OS (10).

The primary roles of an operating system

Process Management.
Memory Management.
File Systems Management.
Device Management.
Security and Privacy.
Only these 5 names carry 5marks and explain these all should carry extra marks.

11. Explain the difference between full associative and direct mapped cache mapping approaches . Explain "write through" and "write back" policies in cache (8+7)

Ans. The full associative cache memory uses the fastest most flexible mapping method, in which both address and data of the memory word are stored. This mapping is expensive because of additional storage of address with data in the cache.
The direct cache mapping, instead of storing total address information with data in cache, only part of address bits is stored with data. This is the simplest and fastest cache mapping, since only tag field is required to match. It is less expensive cache relative to the associative cache.
Difference with one example of both mapping is required to get full marks (8).Write through and write back policies: for getting full marks explain it with its merits and demerits. (7)