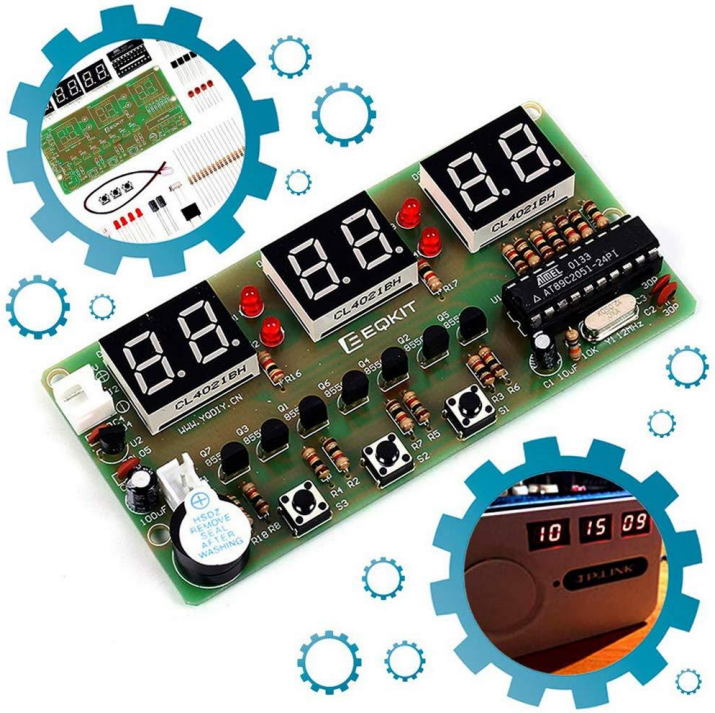


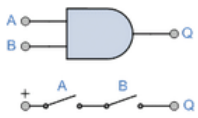
Dr. Hiran Ekanayake

DIGITAL ELECTRONIC FUNDAMENTALS – PART 1

References

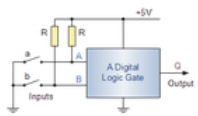
- Tutorials on Logic Gates
  - https://www.electronics-tutorials.ws/category/logic

Logic Gates (12)



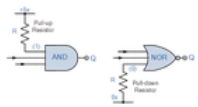
Universal Logic Gates

Individual logic gates can be connected together to form a variety of different switching functions and combinational logic circuits. As we have seen throught this Digital Logic tutorial section, the three most basic logic gates are the: AND, OR and NOT gates, and given this set ...



Pull-up Resistors

Digital logic gates can be used for connection to external circuits or devices but care must be taken to ensure that their inputs or outputs function correctly and provide the expected switching condition. Modern digital logic gates, IC's and micro-controllers contain many input...



Digital Logic Gates Summary

We have also seen that each gate has an opposite or complementary form of itself in the form of the NAND Gate, the NOR Gate and the Buffer respectively, and that any of these individual gates can be connected together to form more complex Combinational Logic circuits. We have al...

Lesson Outline

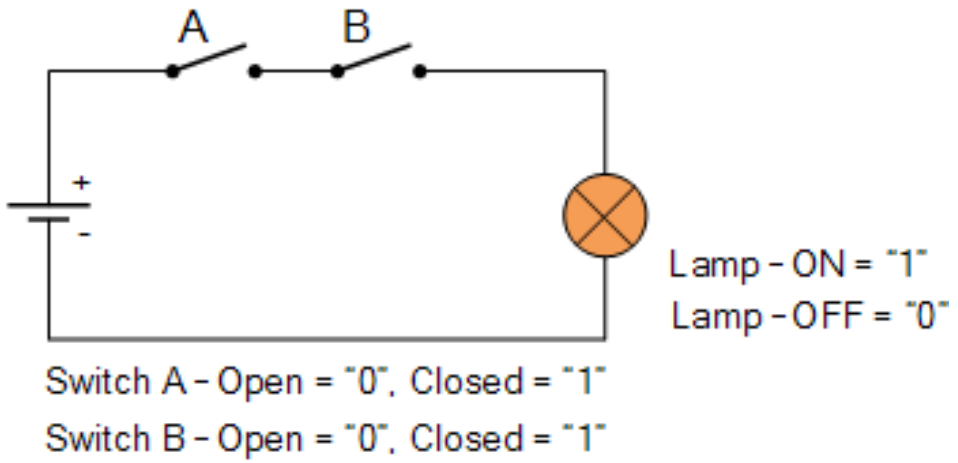
- AND, OR, and NOT logic functions
- Digital logic ICs

LOGIC AND

Logic AND Function

- Describe the logic AND function.
  - The Logic AND Function output is only true when all of its inputs are true, otherwise the output is false.
  - It states that two or more events must occur together and at the same time for an output action to occur. The order in which these actions occur is unimportant.
- Give an example to demonstrate the logic AND function.

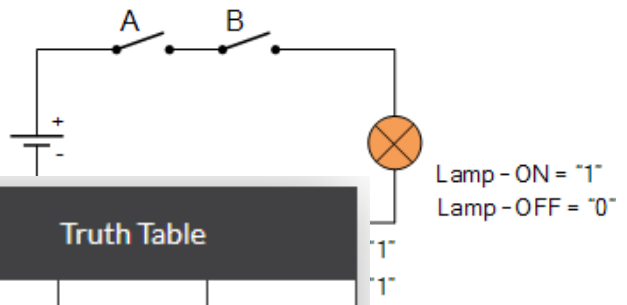
In the given series circuit, both switch A AND switch B must be closed (Logic “1”) in order to put the lamp on.



Logic AND Function

- Give the truth table of the logic AND function.

Switch A	Switch B	Output	Description
0	0	0	A and B are both open, lamp OFF
0	1	0	
1	0	0	
1	1	1	
Boolean Expression (A AND B)			

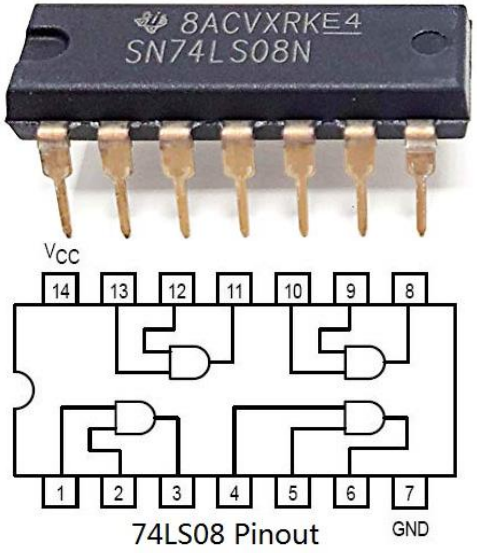


Symbol	Truth Table		
	B	A	Q
	0	0	0
	0	1	0
	1	0	0
	1	1	1
Boolean Expression **Q = A.B**	Read as A **AND** B gives Q		

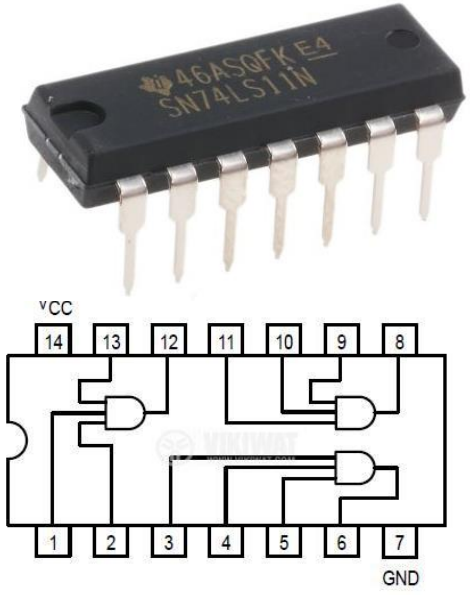
2-input AND Gate

Logic AND Function

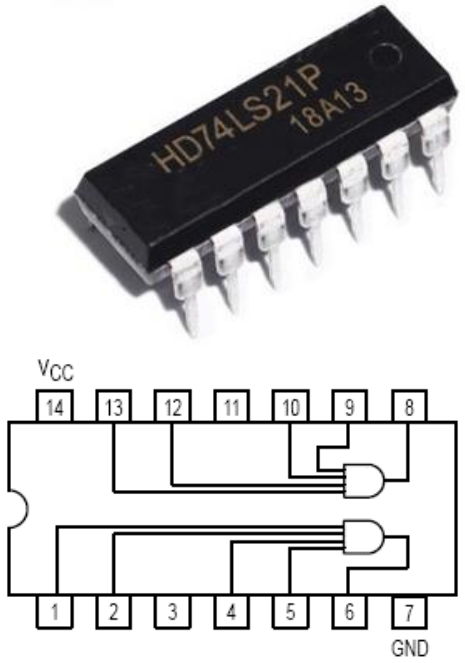
- Which electronic component provides logic AND function?
  - IC (integrated circuit) packages



Quad 2-Input AND Gates



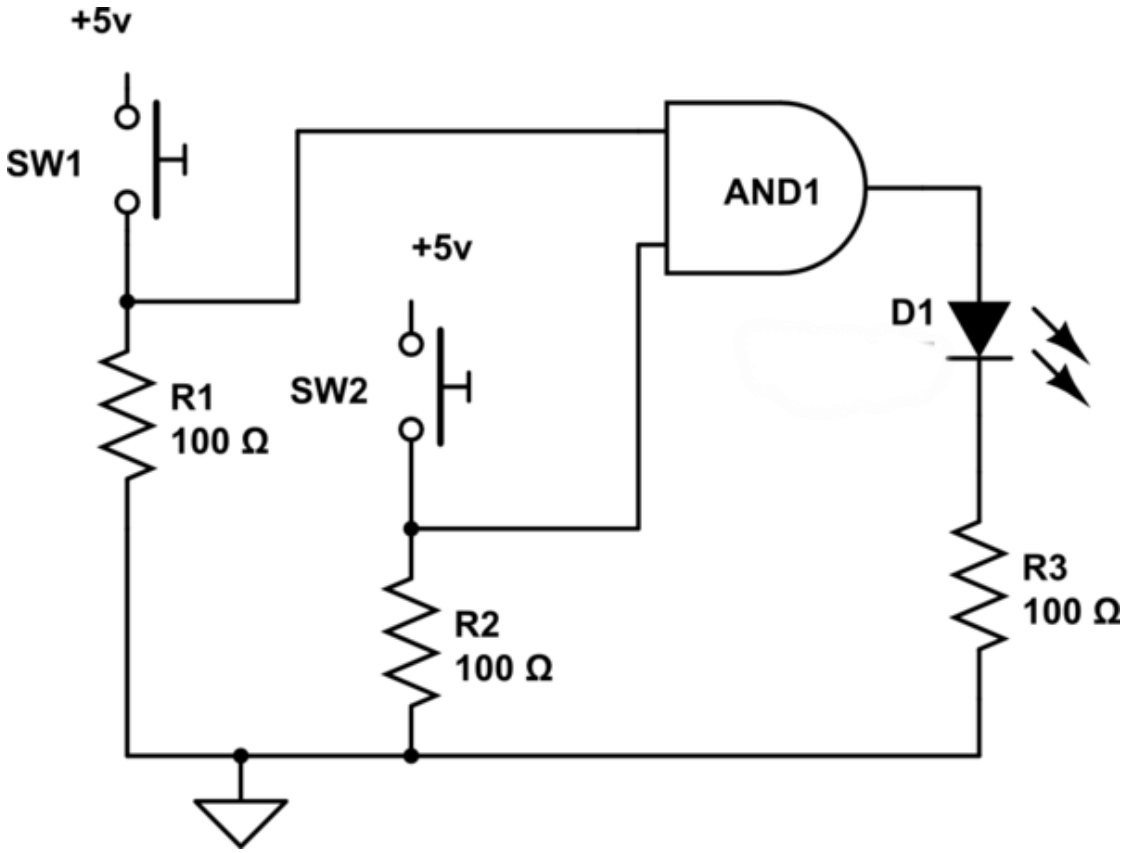
Triple 3-Input AND Gates



Dual 4-Input AND Gates

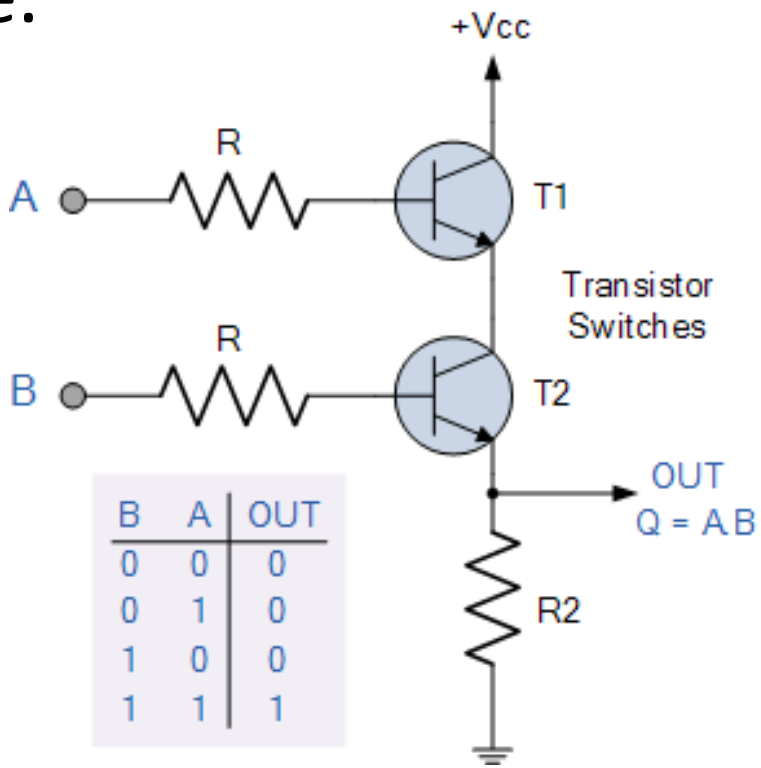
Logic AND Function

- Give a test circuit to test a 2-input AND gate.



Logic AND Function

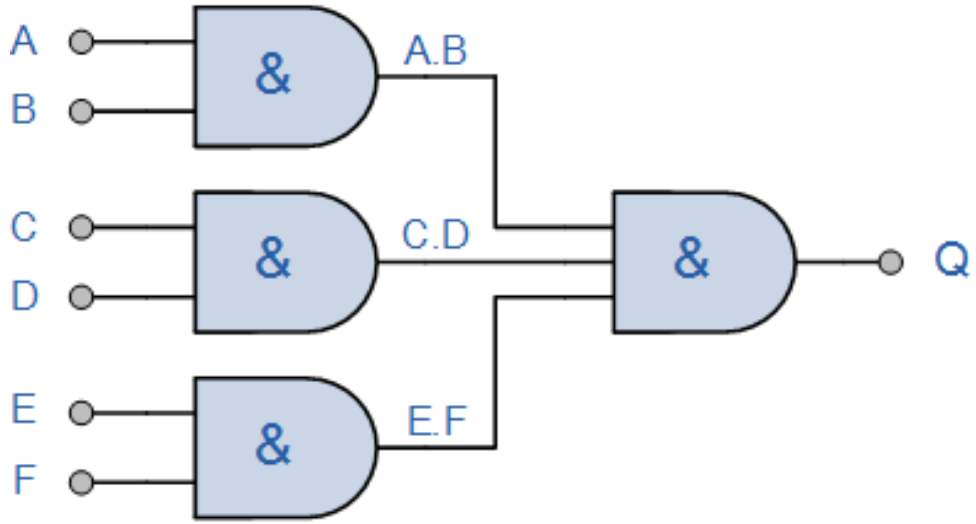
- Give an equivalent transistor-based circuit for the AND gate.



B	A	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Logic AND Function

- How would you construct a 6-input AND gate using 2-input and/or 3-input AND gates?



Boolean Expression:

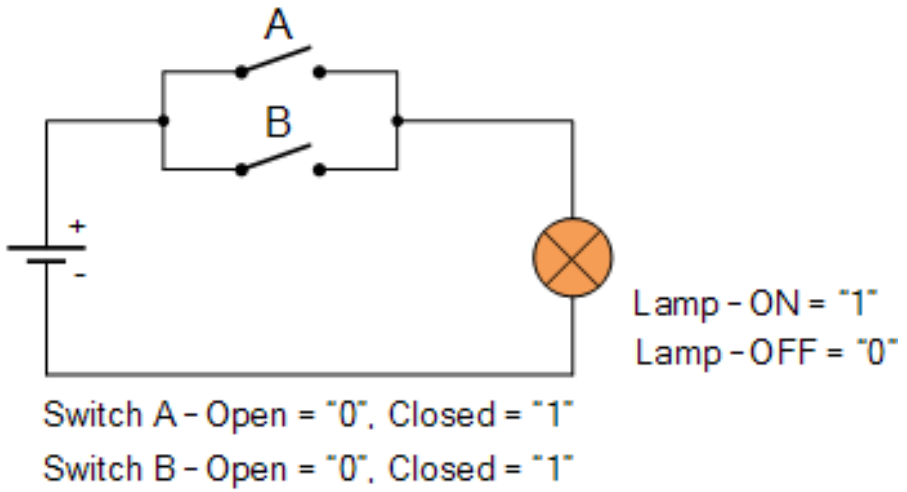
$Q = (A.B).(C.D).(E.F)$

LOGIC OR

Logic OR Function

- Describe the logic OR function.
  - The Logic OR function output is only true if one or more of its inputs are true, otherwise the output is false.
  - Also called “Inclusive-OR”
- Give an example to demonstrate the logic OR function.

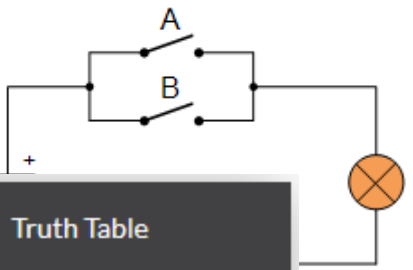
Here the two switches A and B are connected in parallel and either Switch A OR Switch B can be closed in order to put the lamp on.



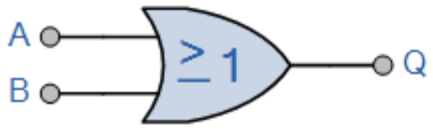
Logic OR Function

- Give the truth table of the logic OR function.

Switch A	Switch B	Output	Description
0	0	0	A and B are both open, lamp OFF
0	1	1	
1	0	1	
1	1	1	
Boolean Expression (A OR B)			



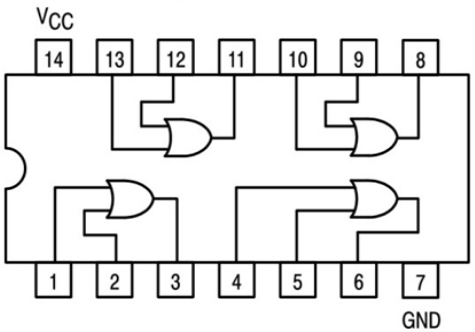
Symbol	Truth Table		
	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	1
Boolean Expression **Q = A+B**	Read as A **OR** B gives Q		



2-input OR Gate

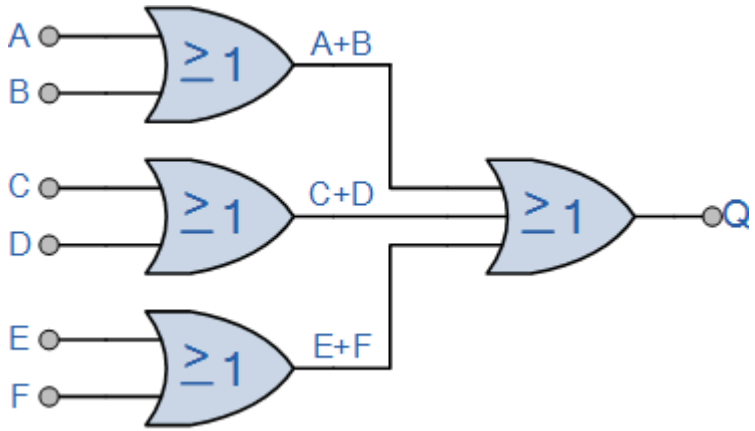
Logic OR Function

- Which IC packages provide the logic OR function?



Quad 2-Input OR Gates

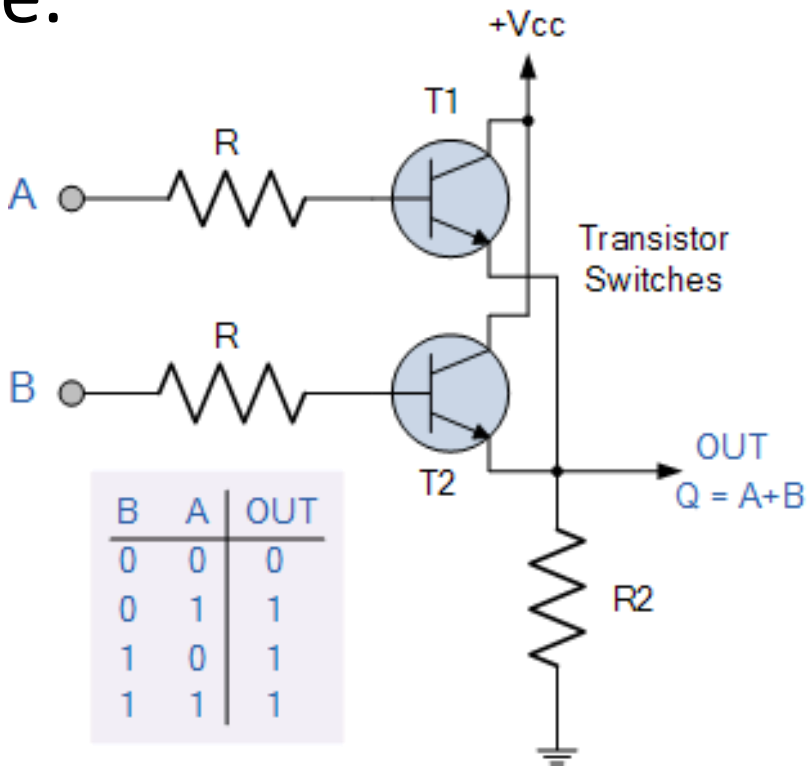
- How would you construct a 6-input OR gate using 2-input and/or 3-input OR gates?



$Q = (A+B)+(C+D)+(E+F)$

Logic OR Function

- Give an equivalent transistor-based circuit for the OR gate.

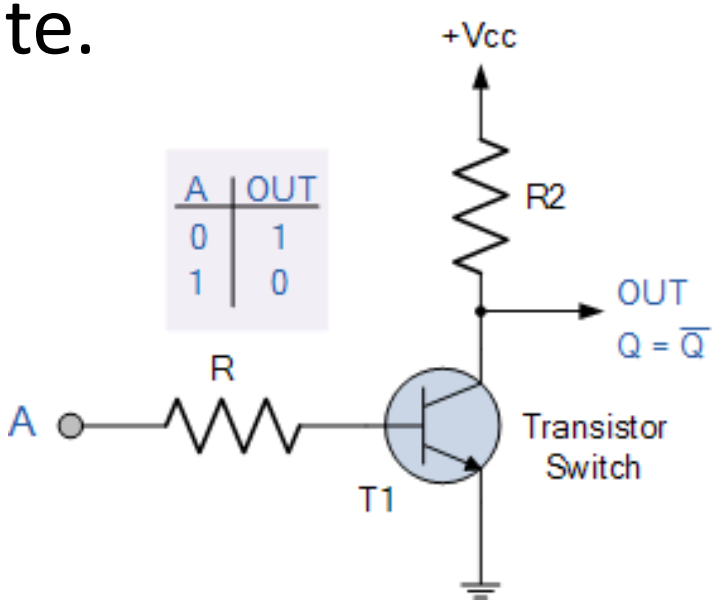


B	A	OUT
0	0	0
0	1	1
1	0	1
1	1	1

LOGIC NOT (INVERTER)

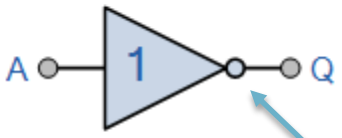
Logic NOT Function

- Describe the logic NOT function.
  - It “inverts” (complements) its input signal.
- Give an equivalent transistor-based circuit for the NOT gate.



Logic NOT Function

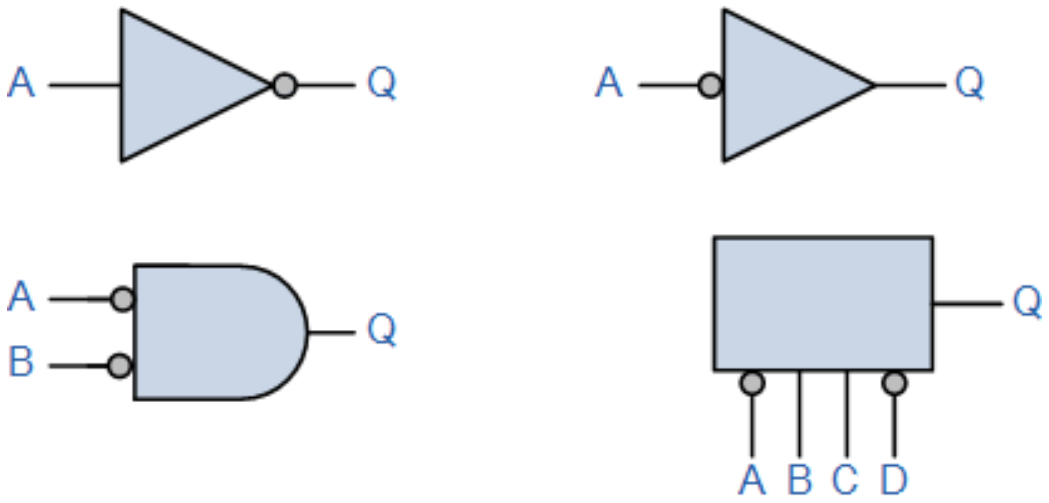
- Give the truth table of the logic NOT function.

Symbol	Truth Table	
 Inverter or NOT Gate	A	Q
	0	1
	1	0
Boolean Expression **Q = not A or $\overline{A}$**	Read as inverse of **A** gives Q	

Inversion Bubble

Input/Out Inversion

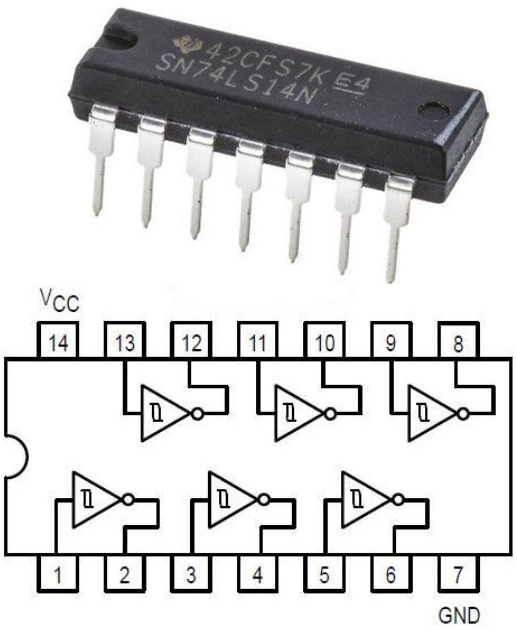
- Describe the use of inversion bubble in the following logic elements.



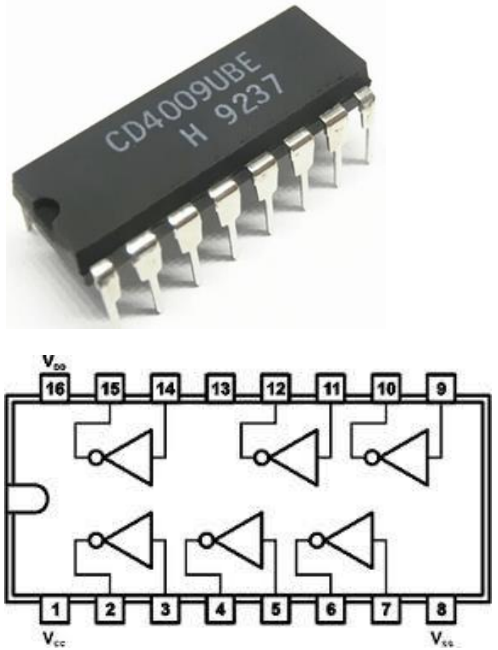
Logic NOT Function

- Which IC packages provide the logic NOT function?

Hex Inverter



Hex Schmitt Inverter



Hex Inverter

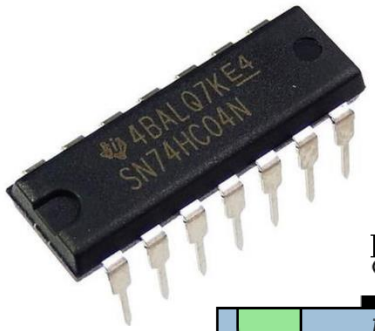
DIGITAL ICS

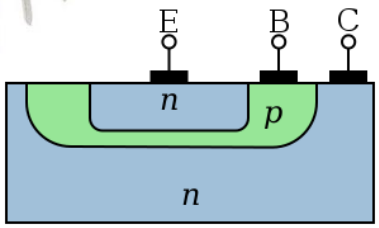
Digital Logic Gates

- What is the difference between 74XX and 4XXX IC packages?
  - Are they compatible with each other?
- What is the convention used in the labelling of IC packages?

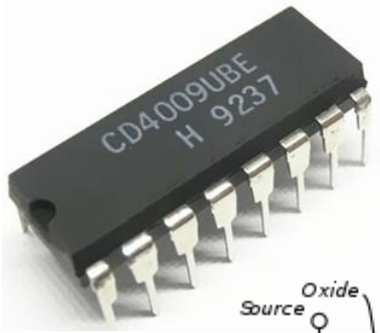
Main Families of Logic Gates

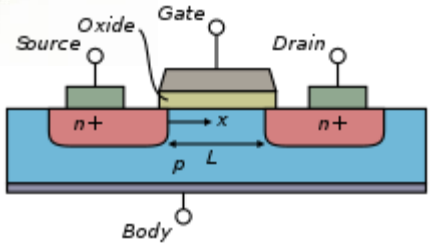
- Transistor-Transistor Logic (TTL)
  - Mainly the 7400 series of chips
  - Use NPN and PNP type Bipolar Junction Transistors to implement the logic





- Complementary Metal-Oxide-Silicon (CMOS)
  - Mainly the 4000 series of chips
  - Use complementary MOSFET or JFET type Field Effect Transistors





Classification of ICs

- Small Scale Integration or (SSI)
  - 10 or few transistors in a package to form simple gates like AND, OR, and NOT
- Medium Scale Integration or (MSI)
  - 10 – 100 transistors to perform digital operations such as adders, decoders, counters, flip-flops and multiplexers
- Large Scale Integration or (LSI)
  - 100 – 1,000 transistors to perform specific digital operations such as I/O chips, memory, arithmetic and logic units

Classification of ICs

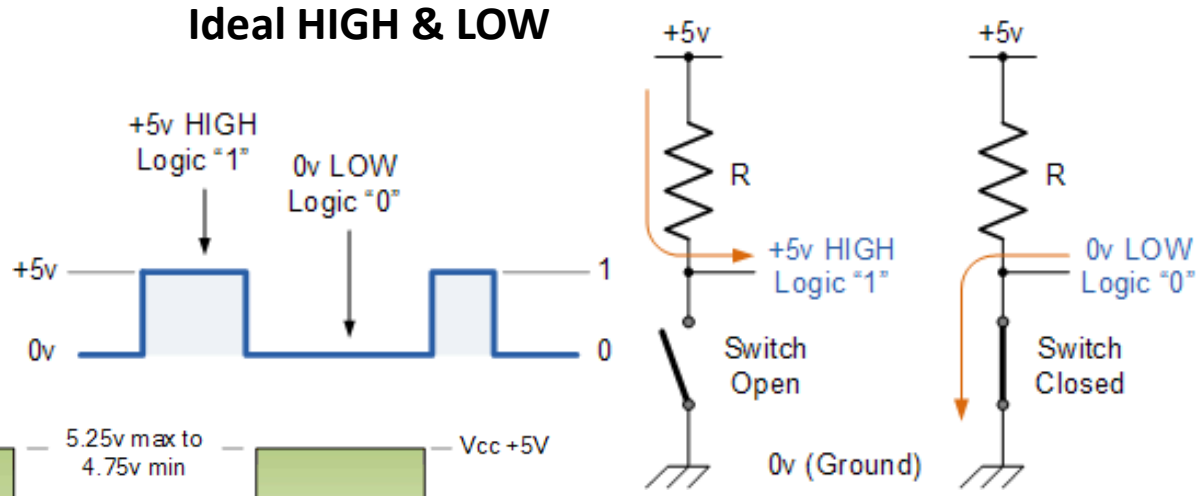
- Very-Large Scale Integration or (VLSI)
  - 1,000 – 10,000 transistors to perform computational operations such as processors, large memory arrays and programmable logic devices
- Super-Large Scale Integration or (SLSI)
  - 10,000 – 100,000 transistors to perform computational operations such as microprocessor chips, micro-controllers, basic PICs and calculators

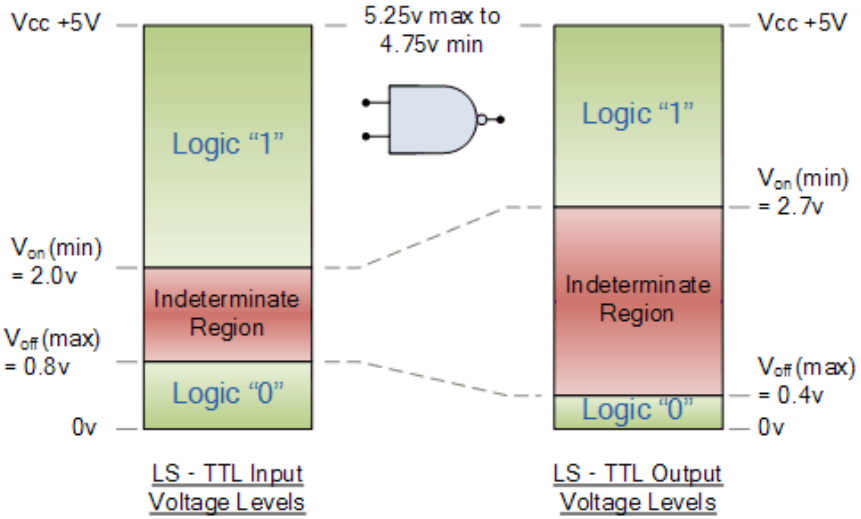
Classification of ICs

- Ultra-Large Scale Integration or (ULSI)
  - More than 1 million transistors in a package, used in computers CPUs, GPUs, video processors, micro-controllers, FPGAs and complex PICs

E.g., Intel Core2 Duo Processor E8500 uses 410 million transistors

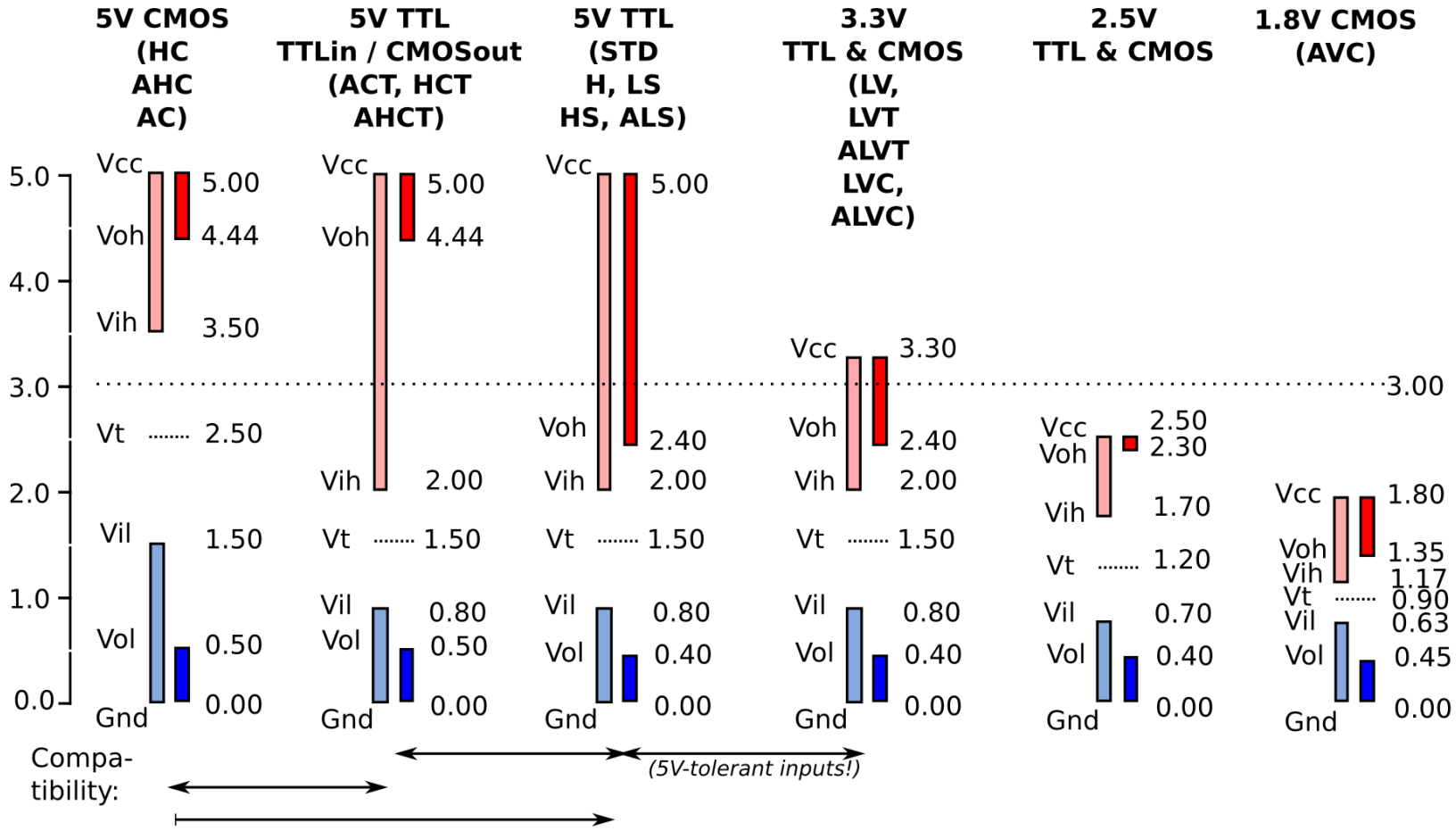
Voltage Levels





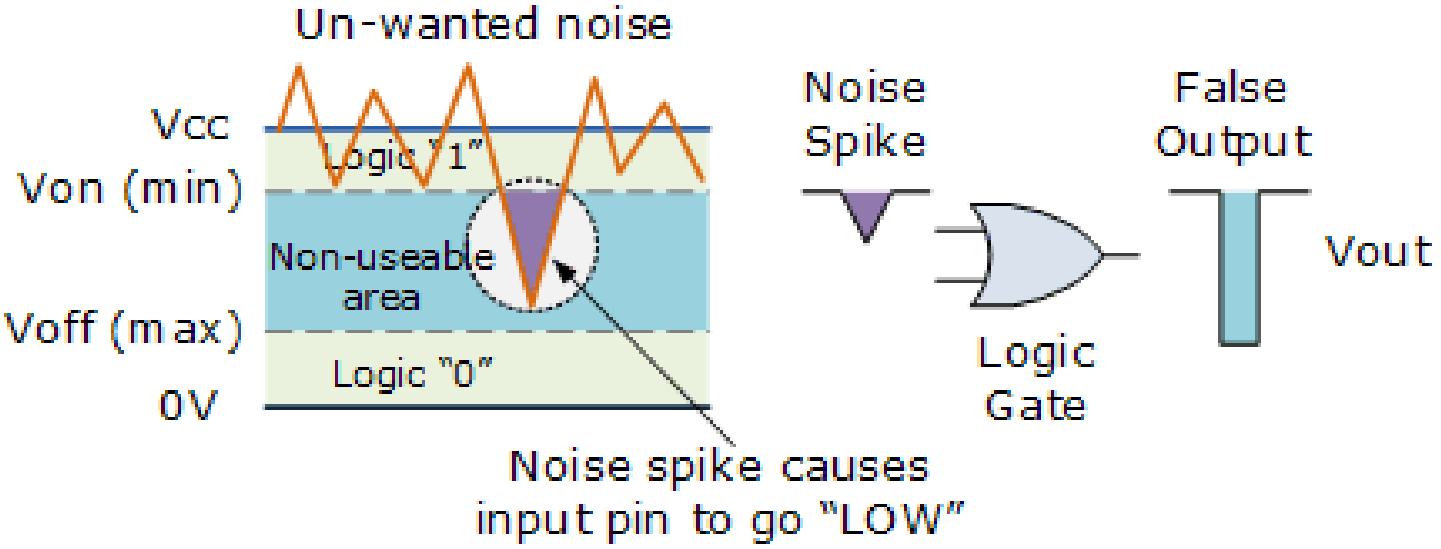
Device Type	Logic 0	Logic 1
TTL	0 to 0.8v	2.0 to 5v (V_{CC})
CMOS	0 to 1.5v	3.0 to 18v (V_{DD})

Voltage Levels



Data source: EETimes, A brief recap of popular logic standards (Mark Pearson, Maxim).

The Intermediate Region ("no-man's land")

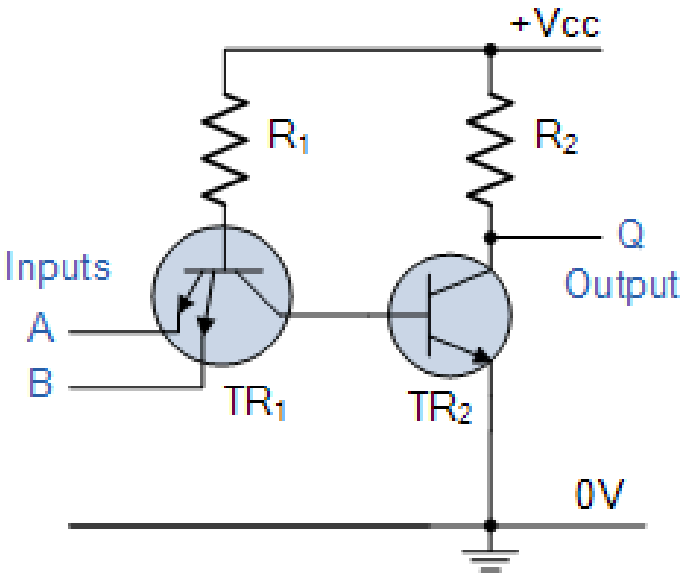


- Noise immunity of a gate
  - For a logic gate not to be affected by noise it must be able to tolerate a certain amount of unwanted noise on its input without changing the state of its output.

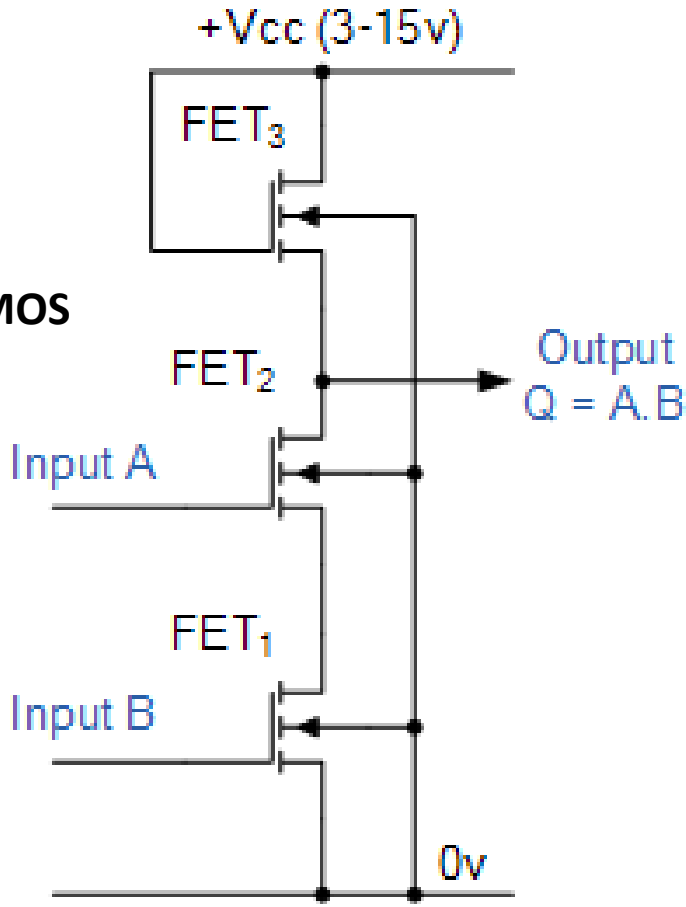
TTL/CMOS Logic Gates

2-input NAND Gate

TTL



CMOS

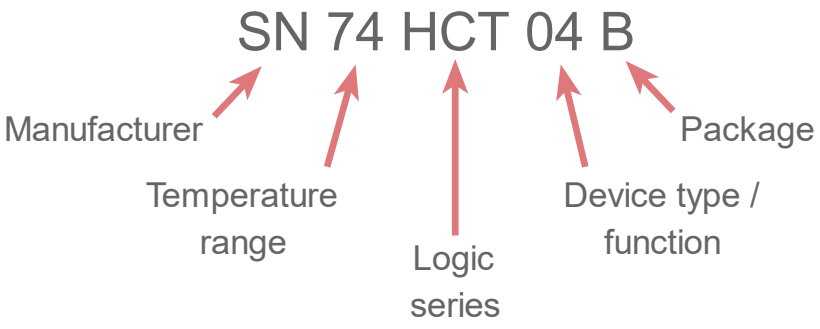


TTL/CMOS Logic Gates

- TTL Limitations:
  - Since bipolar transistors are current operated, their current consumption is very high
  - Limited operating speed due to slow rise/fall time (propagation delay)
- CMOS Strengths:
  - Near zero power consumption (1-2 uA)
  - High-speed switching (>100MHz)

TTL Numbering

https://www.electronics-notes.com/articles/electronic_components/logic-ic-families-technologies/ic-numbering-schemes.php

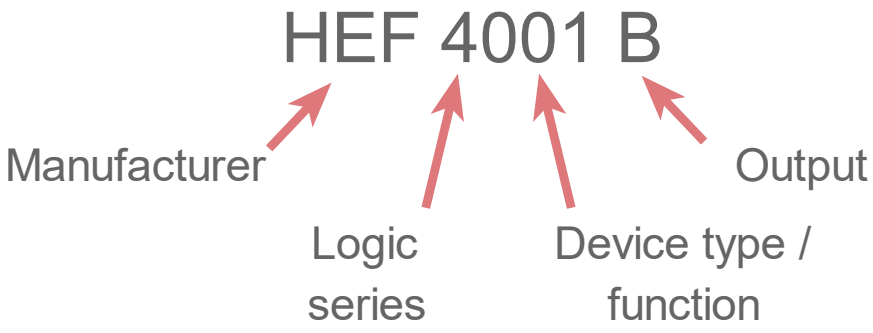


PART NUMBERING SCHEME FOR 74XX00 SERIES LOGIC ICS

Manufacturer	This code normally consists of two letters and is a code normally used by a given manufacturer. SN is one used by Texas Instruments. Other manufacturers have their own codes that they place here.
Temperature range	This is indicated by these two figures. 74 indicates 0°C to 70°C commercial and 54 military: -55°C to +125°C. For most applications the 74 series is perfectly acceptable and this series will be found in consumer devices.
Logic series	This is the sub-family. 7400 for example is the basic series, but there are many others.
Device	This indicates the device function / type. For example devices with 04 are hex inverters, etc. They are the common across all sub-families.
Package code	This is the package suffix. It is necessary to refer to the manufacturers datasheets as these codes vary between manufacturers.

CMOS Numbering

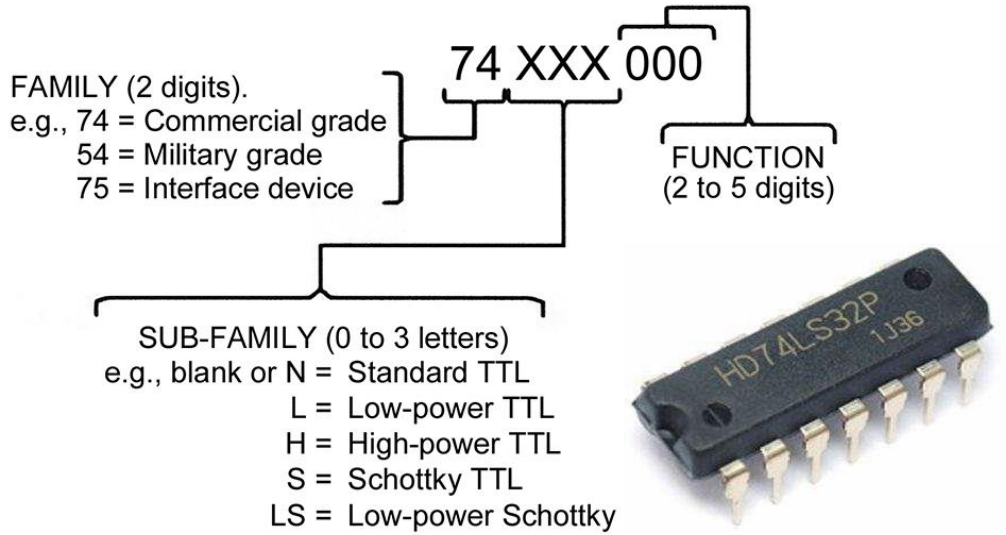
https://www.electronics-notes.com/articles/electronic_components/logic-ic-families-technologies/ic-numbering-schemes.php

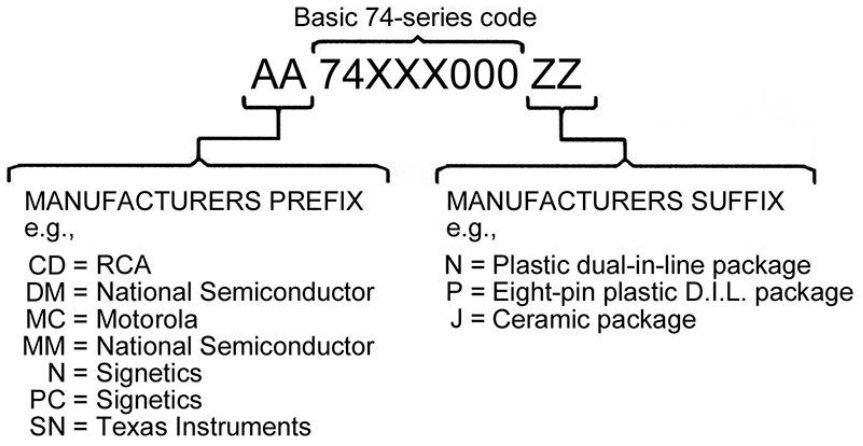


PART NUMBERING SCHEME FOR 4000 SERIES LOGIC ICS

Manufacturer	This code normally consists of two letters and is a code normally used by a given manufacturer. HEF is what used to be Mullard / Phillips.
Series	This is indicated by these the 4 in the 4000 figure.
Device	This indicates the device function / type. For example devices the 01, i.e. 4001 is a quad 2-input NOR.
Output	Early devices did not have any output buffering and were lacking in drive. Later versions were buffered and these chips had the "B" suffix added to the part number.

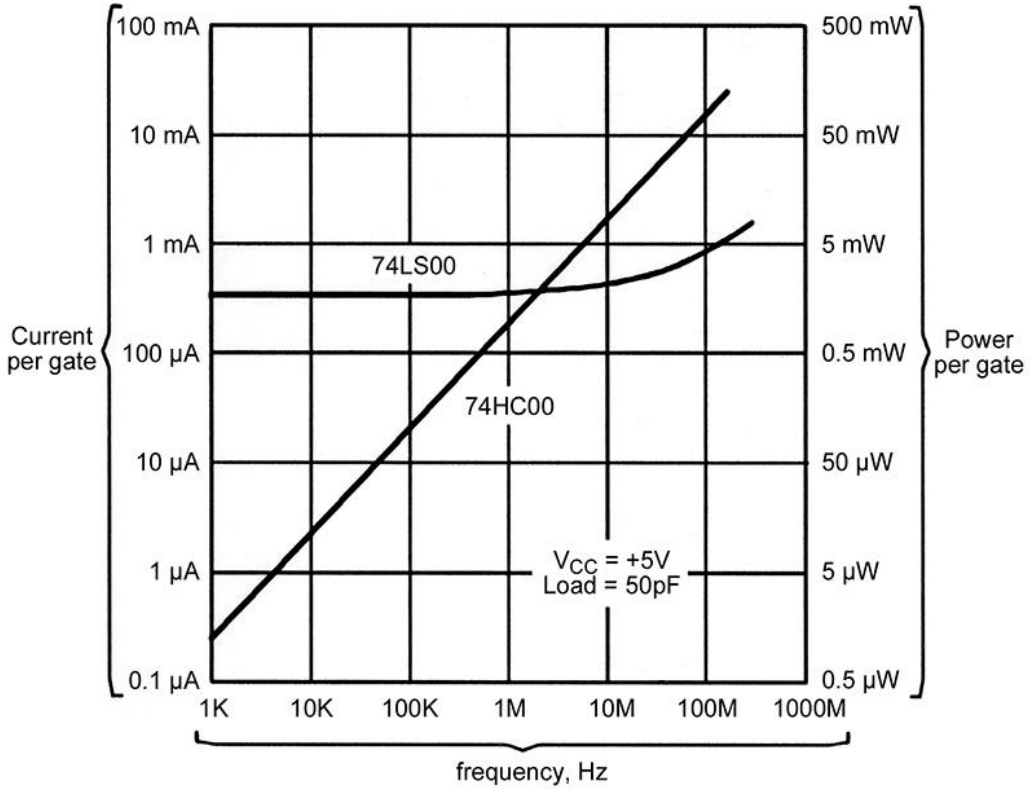
TTL Sub-Families

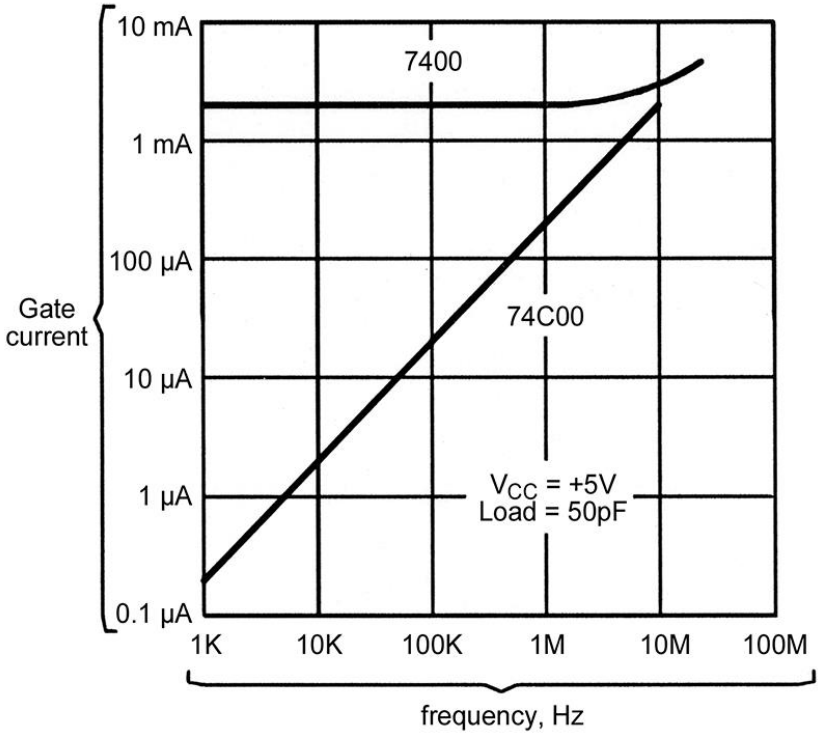




PARAMETERS	74-Series TTL Sub-families							UNITS
	Standard	L	H	S	LS	AS	ALS	
Propagation Delay (2-input NAND gate)	9nS	33	6	3	8	2	4	nS
Power Dissipation (per gate)	10 mW	1	22	20	2	22	1	mW
V_{IH}	2.0V	2.0	2.0	2.0	2.0	2.0	2.0	V
V_{OH}	2.4V	2.4	2.4	2.7	2.7	V_{DD}-2V	V_{DD}-2V	V
NM-H	400 mV	400	400	700	700	700	700	mV
V_{IL}	0.8V	0.7	0.8	0.8	0.8	0.8	0.8	V
V_{OL}	0.4V	0.3	0.4	0.5	0.5	0.5	0.5	V
NM-L	400 mV	300	400	300	300	300	300	mV

Comparing the Frequency vs. Power Consumption



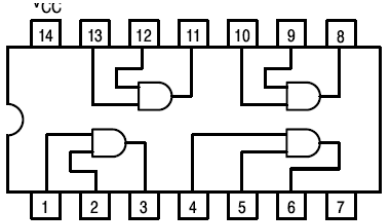


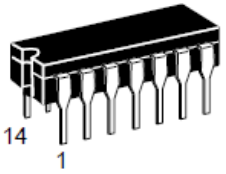
Inspecting Datasheets

MOTOROLA

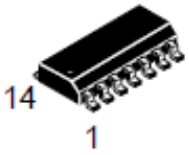
QUAD 2-INPUT AND GATE

SN54/74LS08

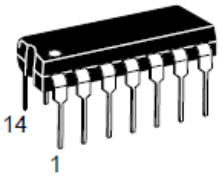




J SUFFIX
CERAMIC
CASE 632-08



D SUFFIX
SOIC
CASE 751A-02



N SUFFIX
PLASTIC
CASE 646-06

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				4.8	mA	V_{CC} = MAX	
	Total, Output LOW				8.8			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		8.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		10	20	ns	

Inspecting Datasheets

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised July 2001

DM7408
Quad 2-Input AND Gates

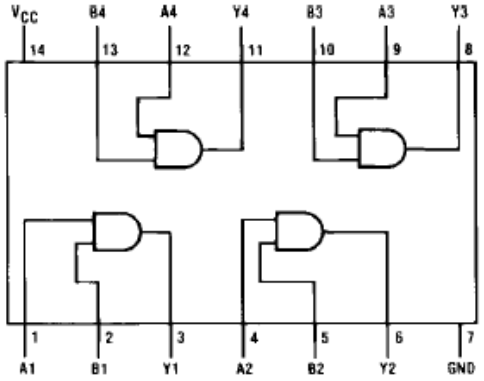
General Description

This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM7408N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.8	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−18		−55	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		11	21	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		20	33	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF, R_L = 400Ω		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Exercise

- Develop an Arduino based system to discover the truth table (logic function) of an unknown logic element (e.g., IC tester). State any assumptions you make.