Name: Dinyar Islam GTID: 903586823

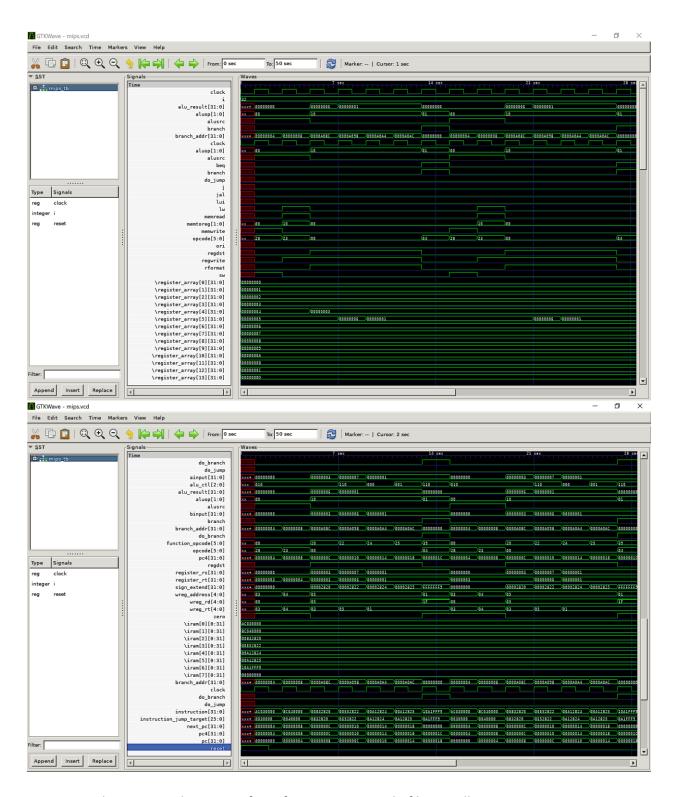


Figure 1. Lab 1 Q1: resulting waveform from running makefile initially.

Name: Dinyar Islam GTID: 903586823

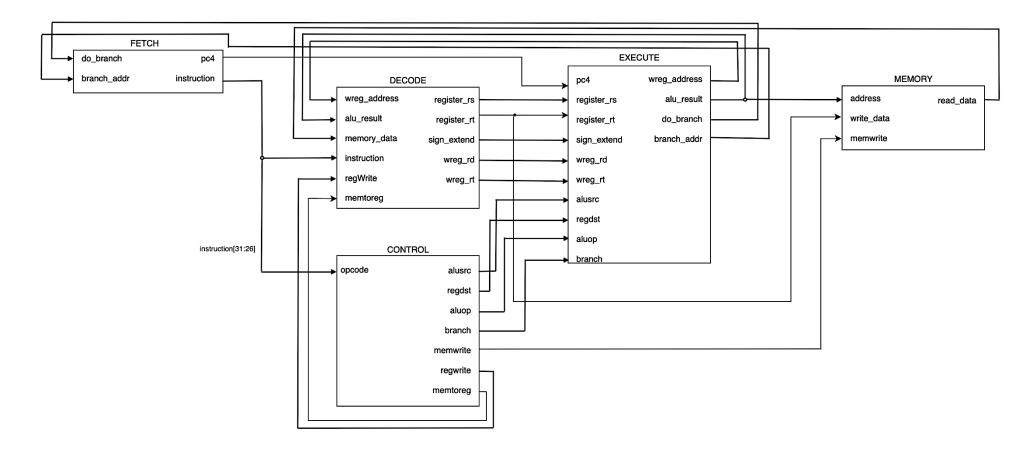


Figure 2. Lab 1 Q2: module-connection diagram

Name: Dinyar Islam GTID: 903586823

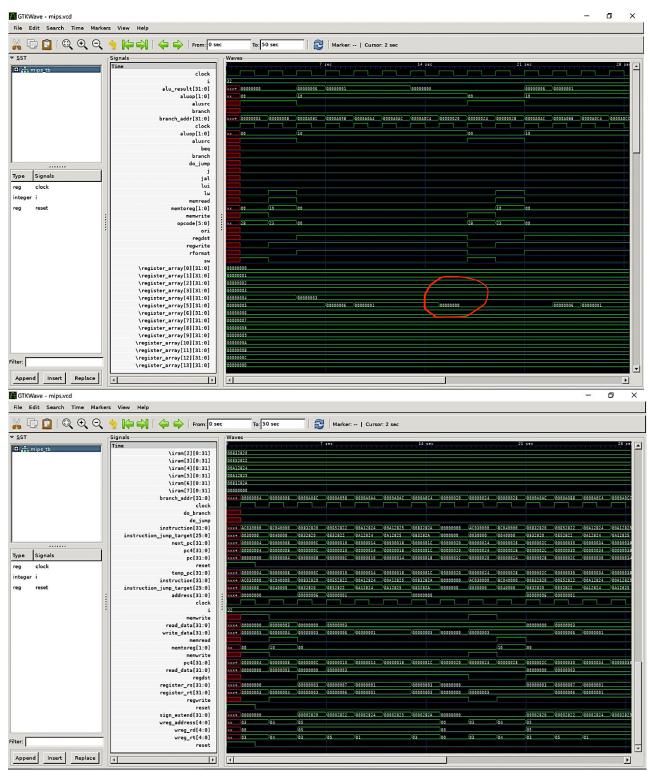


Figure 3. Lab 1 Q4: slt instruction waveform. The instruction that is being run is slt \$5,\$4,\$3. The slt instruction is running after a number of other instructions are executed after which the value of registers \$3 and \$4 are 0x3 and 0x3 respectively. Since, register \$4 and register \$3 are equal, \$4 is not less than \$3 meaning \$5 is set to 0x0 (around the 15 second mark in the first graph figure).