TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

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Audio Amplifier

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Contents

1 Introduction

The objective of this laboratory assignment is to build an amplifying circuit based on an OP-AMP component.

In Section **??**, a theoretical analysis of the circuit is presented. In Section **??**, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section **??**. The conclusions of this study are outlined in Section **??**.

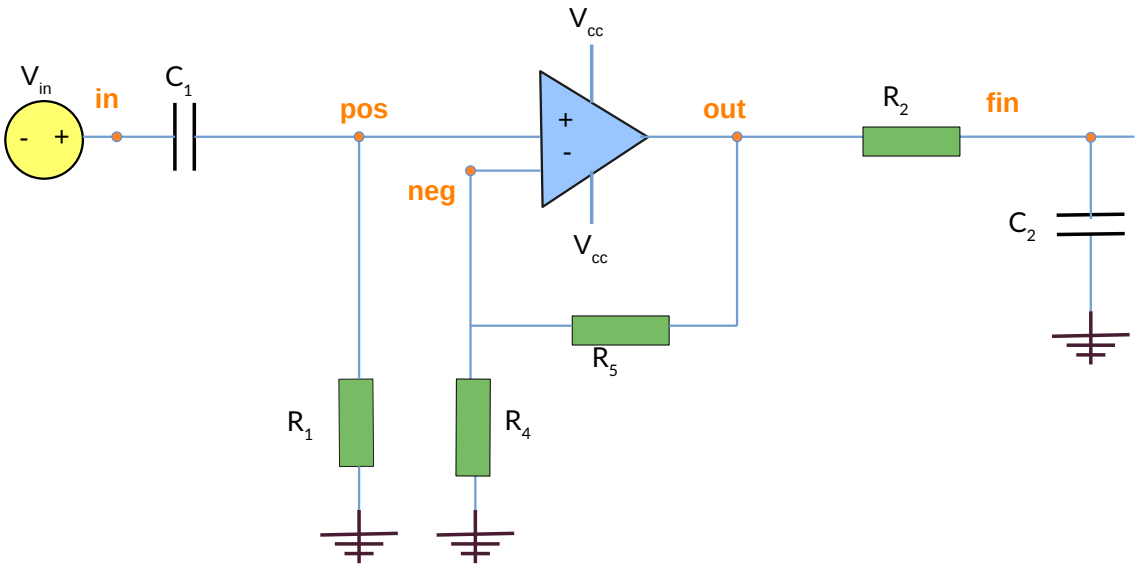


Figure 1: OP-AMP Circuit

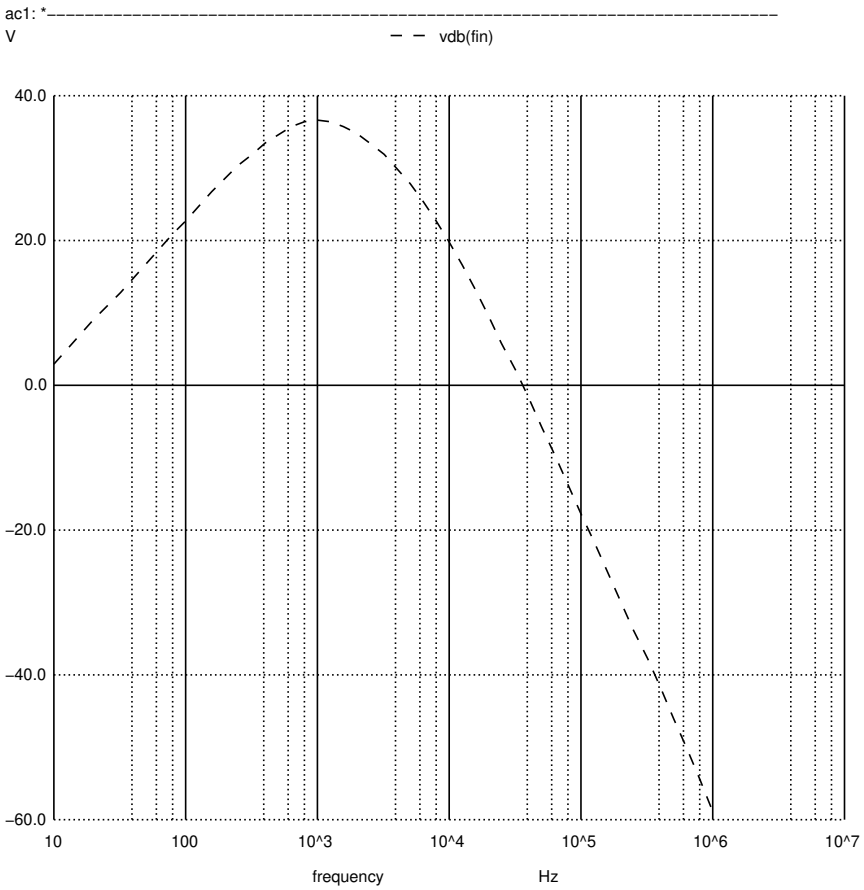
2 Simulation Analysis

We simulated the circuit using frequency analysis, using the supplied model of the OP-AMP:

Table 1: Values of capacitances and resistances for various circuit components

Vcc	10.0 V
Vee	10.0 V
C1	220 nF
C2	220 nF
R1	1000 Ohm
R2	500 Ohm
R3	100 kOhm
R4	1000 Ohm

We simulate the circuit using frequency analysis and max(vin(t))=1, obtaining the following gain in v_fin, which is the gain at the end of the circuit:



The calculated input impedance is $(0.99001 + i \cdot 0.00732)Ohm$. A different setup was used to calculate the output impedance which yielded $(-9.519 \cdot 10^{-5} + i \cdot 7.234 \cdot 10^{-3})Ohm$.

This circuit has a cost of 113.44, a maximum gain of $36.55dB$, central frequency of $1006.5Hz$. The calculated merit is therefore $3.9375 \cdot 10^{-4}$.

3 Theoretical Analysis

For the theoretical simulation, we used the dependent voltage source model of the transistors, with Bf1=178.7 and Bf2=227.3.

The bias circuit, which is constituted by V_c, R_{B1} and R_{B2}, will determine V_b.

To simplify the bias circuit, we can ignore the capacitors and make a Thevenin equivalent. This yields:

$$R_B = \frac{R_{B1}R_{B2}}{R_{B1} + R_{B2}} \tag{1}$$

$$V_{eq} = \frac{R_{B2}}{R_{B1} + R_{B2}} V_c \tag{2}$$

To calculate the current that passes through the node 8 we know that $I_E = (1 + \beta_f)I_B$.
The mesh equation for the bias circuit is $V_{eq} + R_B I_B + V_{Beon} + R_E I_E = 0$
Substituting the equation of I_E, we now have an expression for I_B:

$$I_B = \frac{V_{eq} - V_{ON}}{R_B + (1 + \beta_F)R_E} \tag{3}$$

The equation for I_C, which is the current that passes trough node 2, is simply $I_C = \beta_F I_B$.
Then, looking at the other mesh, constituted by R_E, Q_1, R_C andV_c, we have the equation:

$$V_o = V_c - R_C I_C \tag{4}$$

By Ohm's Law we also know that $V_E = R_E I_E$ so the voltage between R_C and R_E is: $V_{CE} = V_o - V_E$

We now have all the static voltages and cuurents computed.

For the results of the OP analysis we obtain:

Table 2: Some values of the operating point analysis

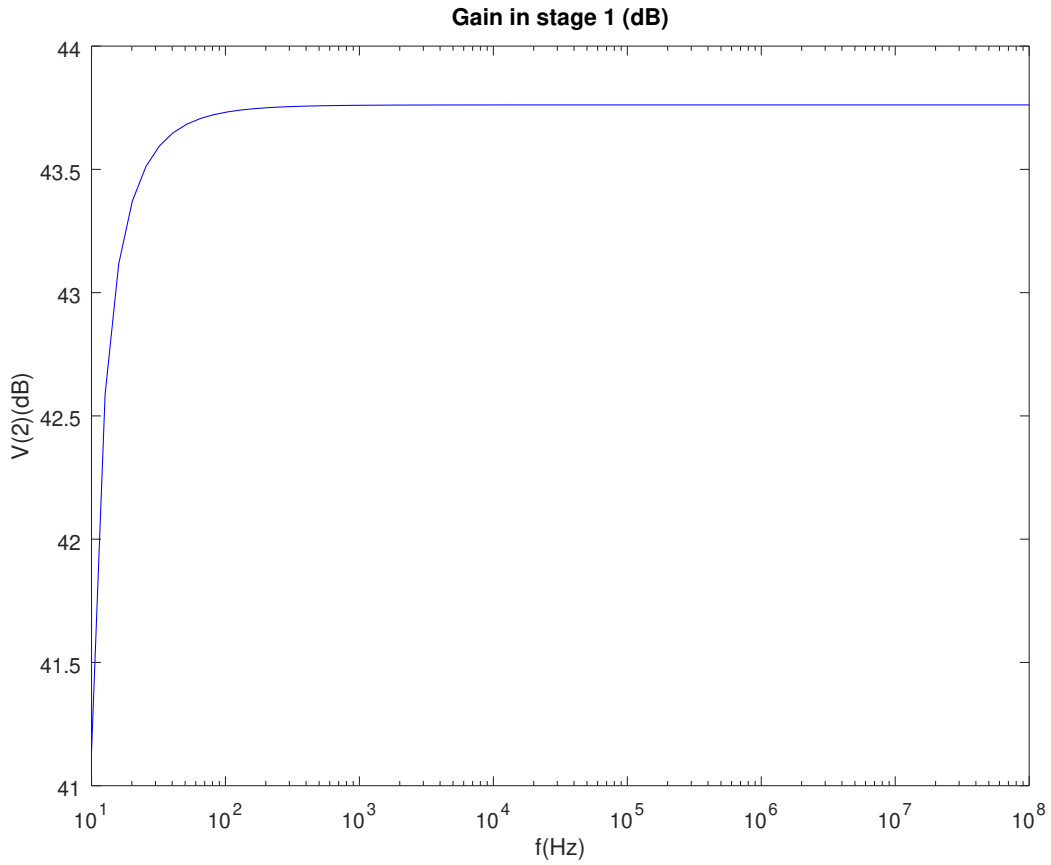
I_{b1}	$5.0044e-05$
I_{e1}	0.0089929
I_{c1}	0.0089429
V_{CE1}	2.1578
I_{b2}	$3.610556e-04$
I_{e2}	0.082429
I_{c2}	0.082068
V_{CE2}	4.4858

The incremental model of the transistor was used to calculate the input and output impedances, as well as the gain on both stages of the circuit. The capacitors were modelled as short circuits in this stage. This yields:

Table 3: Gains and Impedances

Z_{i1}	484.43
Z_{o1}	886.28
Z_{i2}	8598.9
Z_{o2}	0.30217
$Gain_1$	-262.79
$Gain_2$	0.99195
$Gain_{Total}$	-260.67

Lastly, the capacitors were re-introduced in order to calculate the gain as a function of the frequency after each stage. The results are graphed below:


Gain in stage 1 (dB)
44
43.5
43
42.5
42
41.5
41
V(2)(dB)
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
f(Hz)

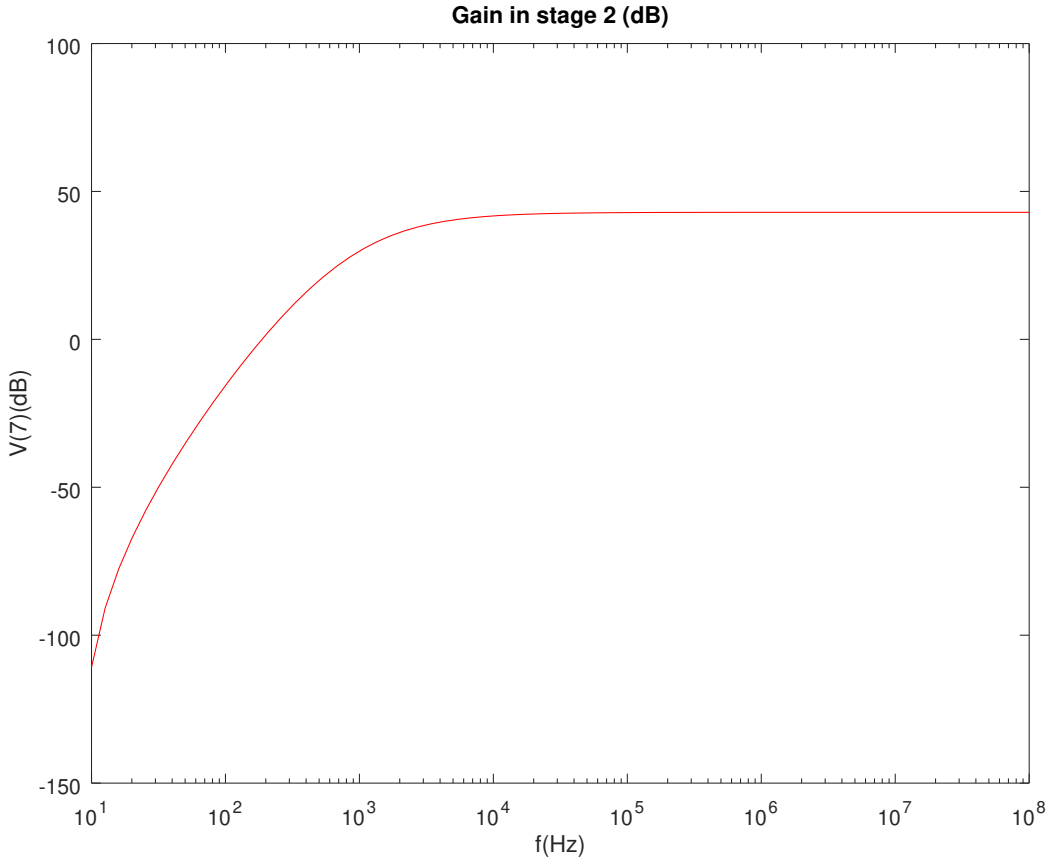

Gain in stage 2 (dB)
100
50
0
-50
-100
-150
V(7)(dB)
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
f(Hz)

Table 4: Gain as a function of frequency

f(Hz)	$V_L(mV)$	f(Hz)	$V_L(mV)$
50.0	98	1600.0	660
75.0	133	1700.0	640
100.0	173	1800.0	630
125.0	209	1900.0	610
150.0	249	2000.0	590
200.0	318	2200.0	540
225.0	346	2600.0	510
250.0	378	3000.0	470
275.0	406	3300.0	430
300.0	440	3600.0	400
325.0	462	3900.0	380
350.0	500	4200.0	350
375.0	520	4500.0	330
400.0	540	5000.0	300
450.0	580	5500.0	277
500.0	610	6000.0	257
550.0	640	6500.0	241
600.0	670	7000.0	225
700.0	710	7500.0	213
800.0	720	8000.0	197
900.0	730	9000.0	181
1000.0	740	10000.0	165
1100.0	720	12000.0	141
1200.0	720	15000.0	117
1300.0	710	20000.0	88
1400.0	690	50000.0	38
1500.0	680		

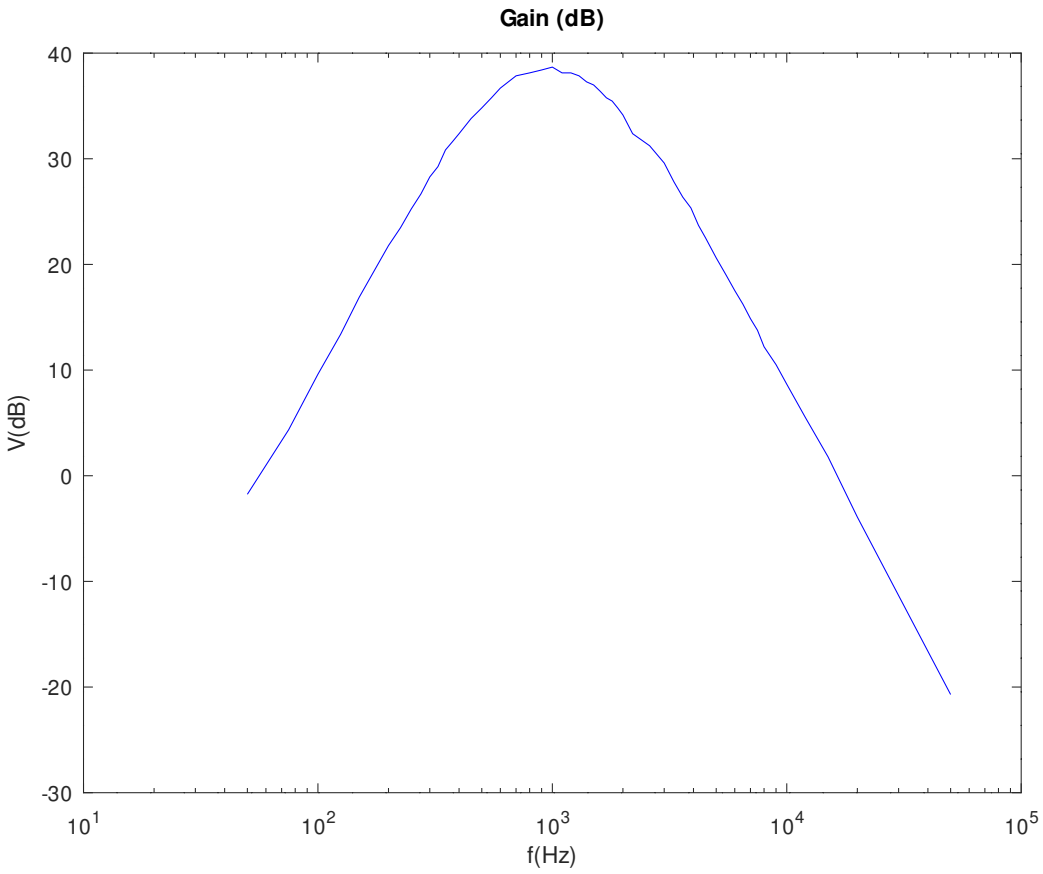
The lower 3dB cut-off point is at $f = 5484.4Hz$ As we can see, the lower cut-off point is accurrate, but this model does not deal well with the higher cut-off point.

4 Experimental Results

We were able to build the circuit presentially utilizing a breadboard and the various components.

Then, the frequency of the input voltage source was ajusted, from $50Hz$ to $50kHz$, at various increments and, for each value, the value of the output voltage was measured. The results are in the following table:

These results were graphed below as to compare them to the theoretical analysis and simulation done above:



5 Conclusion