TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

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Audio Amplifier

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1 Introduction

The objective of this laboratory assignment is to build an audio amplifier

In Section 3, a theoretical analysis of the circuit is presented. In Section 2, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 3. The conclusions of this study are outlined in Section 4.

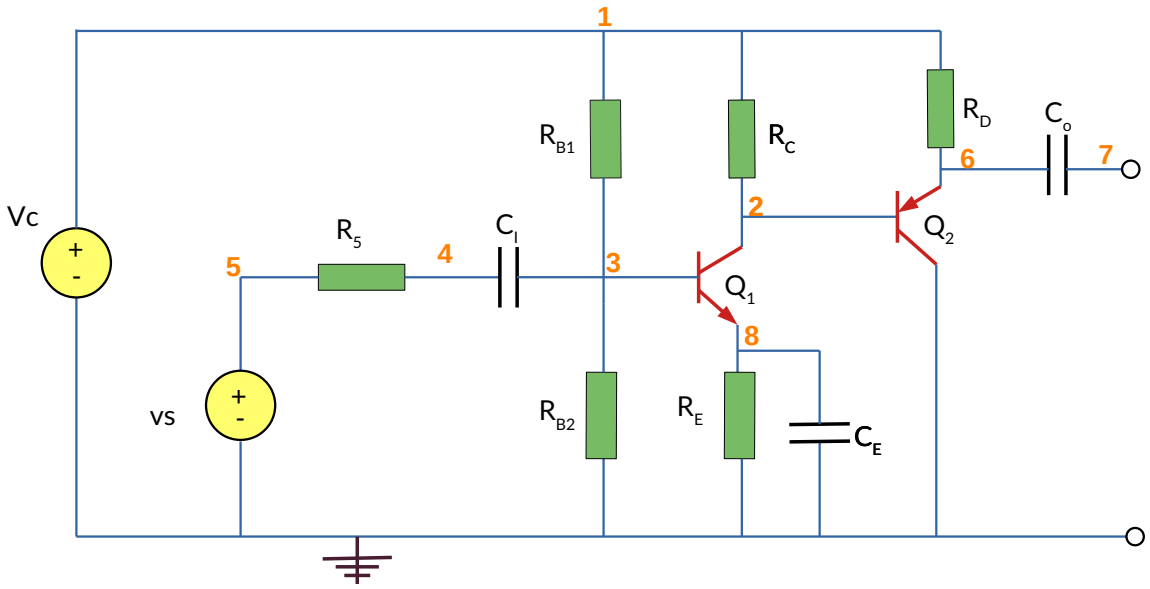


Figure 1: Audio Amplifier Circuit

2 Simulation Analysis

2.1 Transient analysis

We simulated the circuit using transient and frequency analysis, using the supplied model of transistors:

Table 1: Values of capacitances and resistances for various circuit components

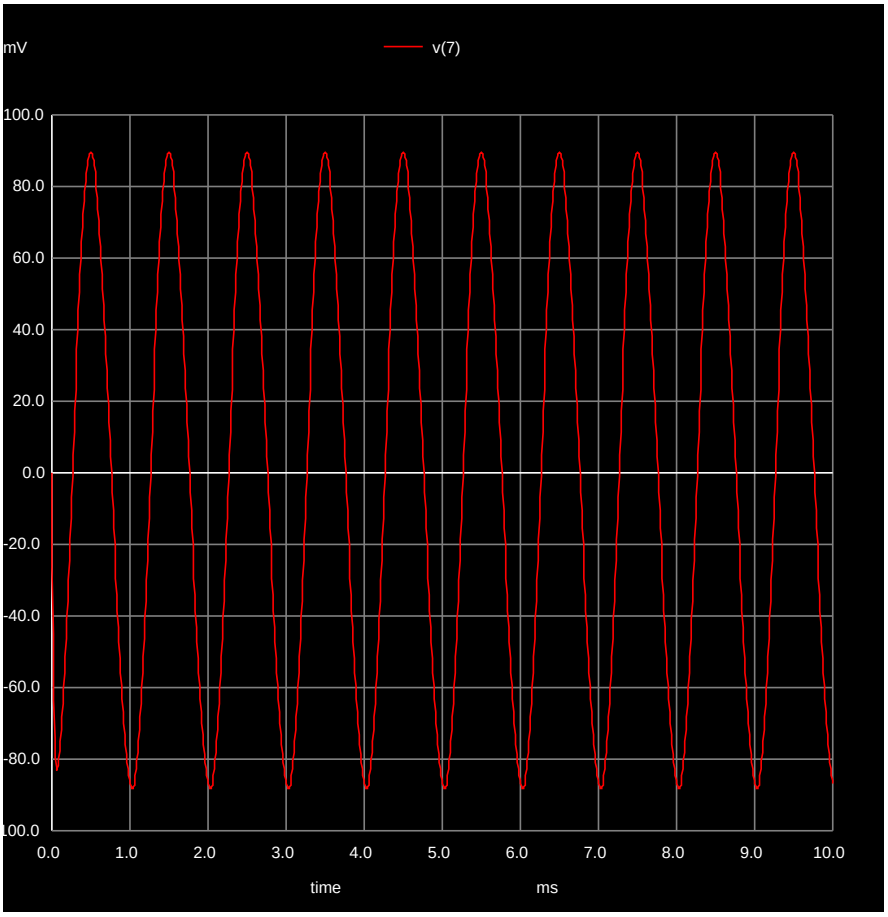
Vc	12.0 V
Vs	10e-3 V
Rs	100 Ohm
Ci	1e-3 F
Rb1	80e3 Ohm
Rb2	20e3 Ohm
Rc	1e3 Ohm
Re	100 Ohm
Ce	1e-3 F
Von	0.7 V
Vt	25e-3 V
Va1	69.7 V
Va2	37.2 V
Rd	100 Ohm
Co	1e-6 F
Rl	8 Ohm

Firstly, we performed an operating point analysis, some of the relevant results obtained are below:

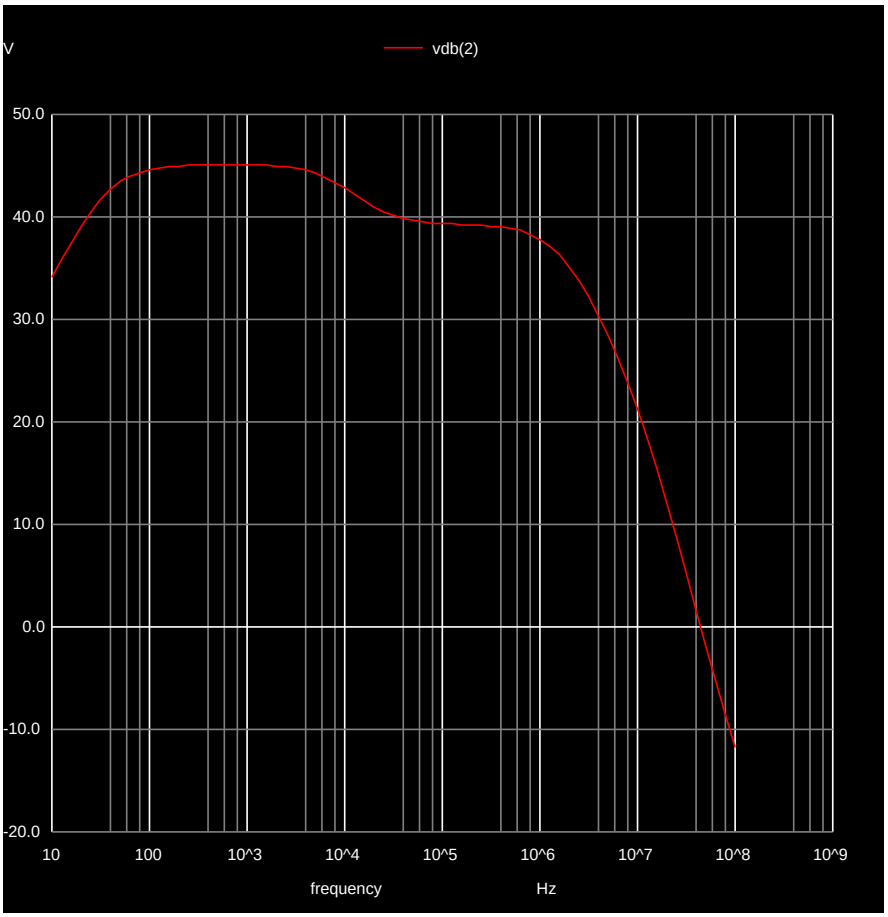
Table 2: OP simulation

I_{e1}	$8.72642e-03$
I_{c1}	$8.675224e-03$
I_{b1}	$5.119304e-05$
V_{CE1}	3.0214713
I_{e2}	$7.29143e-02$
I_{c2}	$7.234499e-02$
I_{b2}	$5.693370e-04$
V_{CE2}	4.708568

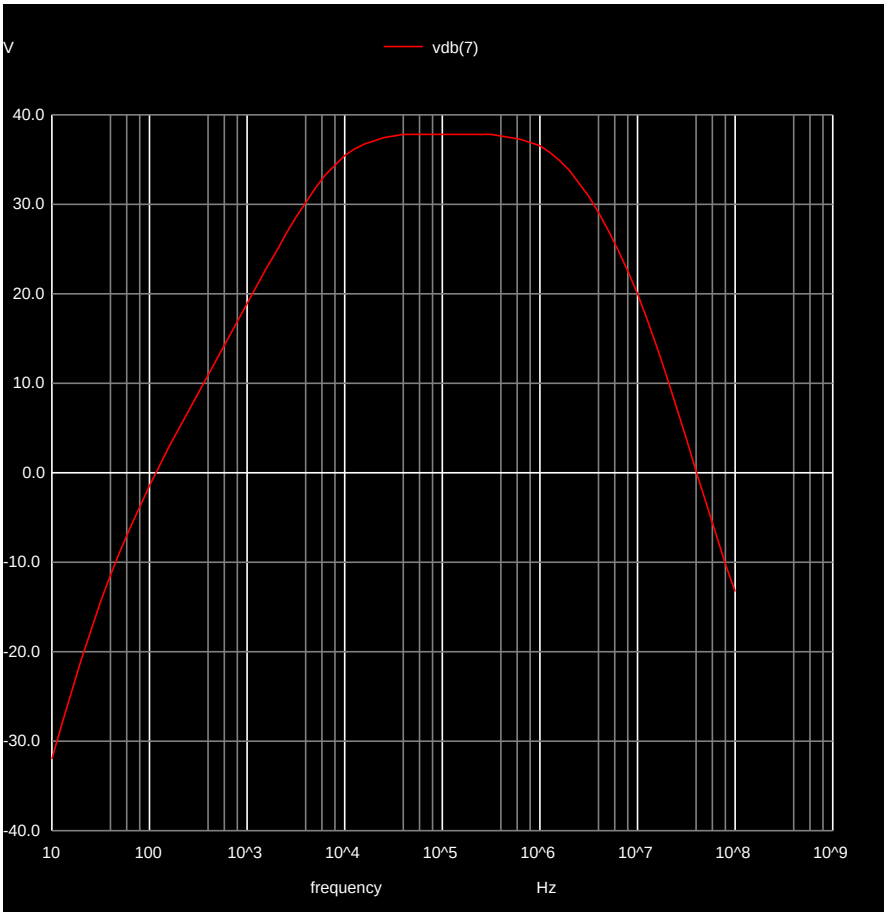
Using transient analysis, and frequency f=1e3 Hz, we simulate the circuit, which yields the following $v_7(t)$:



We simulate the circuit using frequency analysis and max(vs(t))=1, obtaining the following gain in v_2, which is the gain after the gain stage:



And the gain in v_7,which is the gain after the output stage:



This circuit has a cost of 2102.508, voltage gain 3.790425e+01, bandwidth 1.594837e+06, minimum voltage cuttoff 8.880395e+03 and the calculated Merit is 3.238.

3 Theoretical Analysis

For the theoretical simulation, we used the dependent voltage source model of the transistors, with Bf1=178.7 and Bf2=227.3.

The bias circuit, which is constituted by V_c, R_{B1} and R_{B2}, will determine V_b.

To simplify the bias circuit, we can ignore the capacitors and make a Thevenin equivalent. This yields:

$$R_B = \frac{R_{B1}R_{B2}}{R_{B1} + R_{B2}} \tag{1}$$

$$V_{eq} = \frac{R_{B2}}{R_{B1} + R_{B2}} V_c \tag{2}$$

To calculate the current that passes through the node 8 we know that $I_E = (1 + \beta_f) I_B$.
The mesh equation for the bias circuit is $V_{eq} + R_B I_B + V_{Beon} + R_E I_E = 0$
Substituting the equation of I_E, we now have an expression for I_B:

$$I_B = \frac{V_{eq} - V_{ON}}{R_B + (1 + \beta_F) R_E} \tag{3}$$

The equation for I_C, which is the current that passes trough node 2, is simply $I_C = \beta_F I_B$.
Then, looking at the other mesh, constituted by R_E, Q_1, R_C andV_c, we have the equation:

$$V_o = V_c - R_C I_C \tag{4}$$

By Ohm's Law we also know that $V_E = R_E I_E$ so the voltage between R_C and R_E is: $V_{CE} = V_o - V_E$

We now have all the static voltages and cuurents computed.

For the results of the OP analysis we obtain:

Table 3: Some values of the operating point analysis

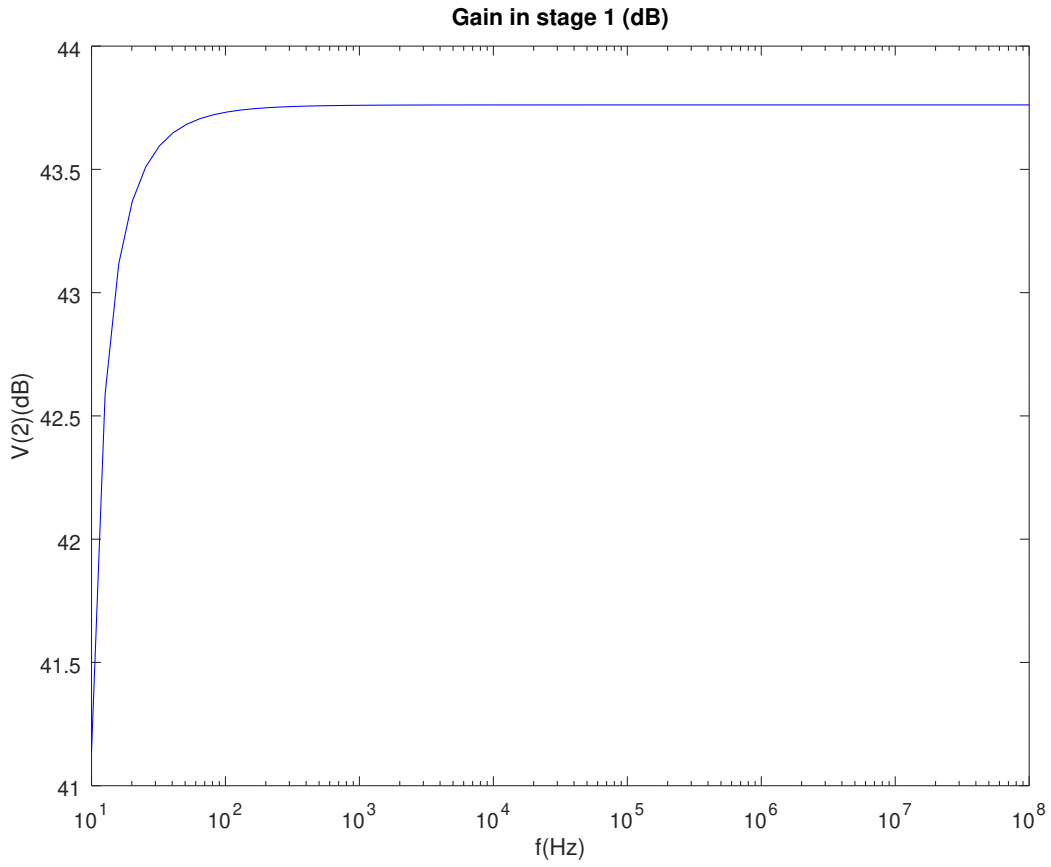
I_{b1}	$5.0044e-05$
I_{e1}	0.0089929
I_{c1}	0.0089429
V_{CE1}	2.1578
I_{b2}	$3.610556e-04$
I_{e2}	0.082429
I_{c2}	0.082068
V_{CE2}	4.4858

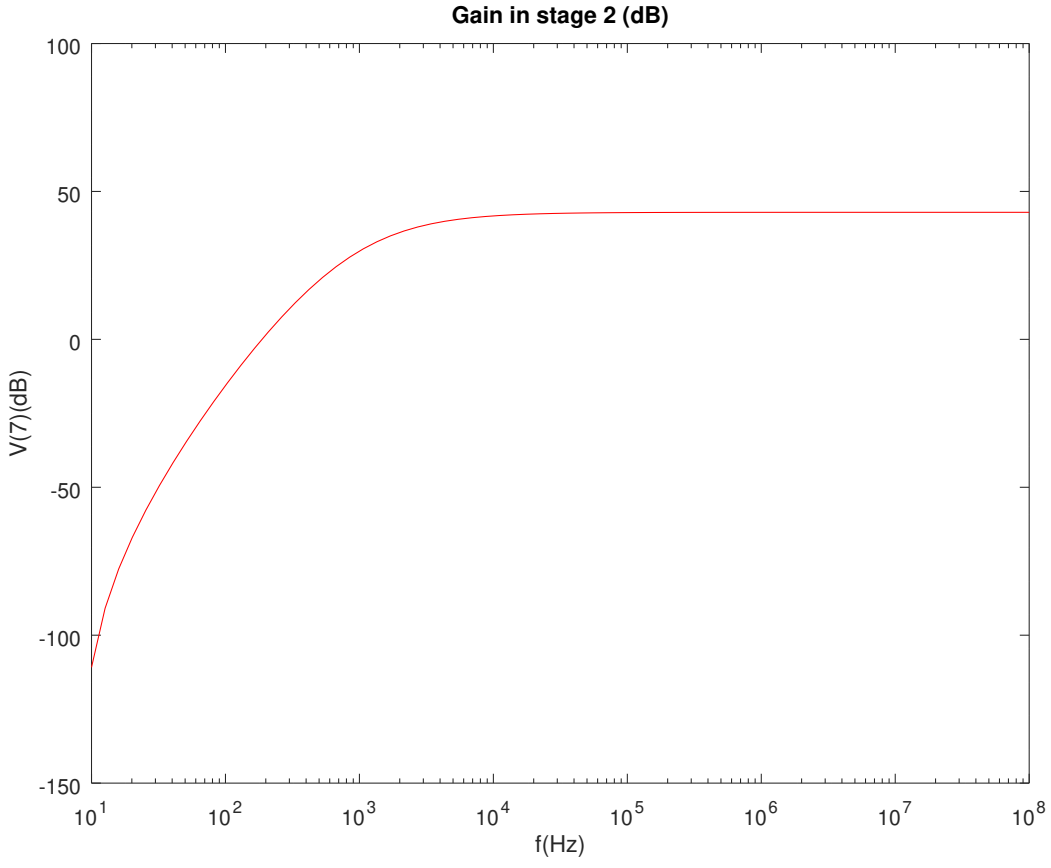
The incremental model of the transistor was used to calculate the input and output impedances, as well as the gain on both stages of the circuit. The capacitors were modelled as short circuits in this stage. This yields:

Table 4: SGains and Impedances

Z_{i1}	484.43
Z_{o1}	886.28
Z_{i2}	8598.9
Z_{o2}	0.30217
$Gain_1$	-262.79
$Gain_2$	0.99195
$Gain_{Total}$	-260.67

Lastly, the capacitors were re-introduced in order to calculate the gain as a function of the frequency after each stage. The results are graphed below:


Gain in stage 1 (dB)
44
43.5
43
42.5
42
41.5
41
V(2)(dB)
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
f(Hz)

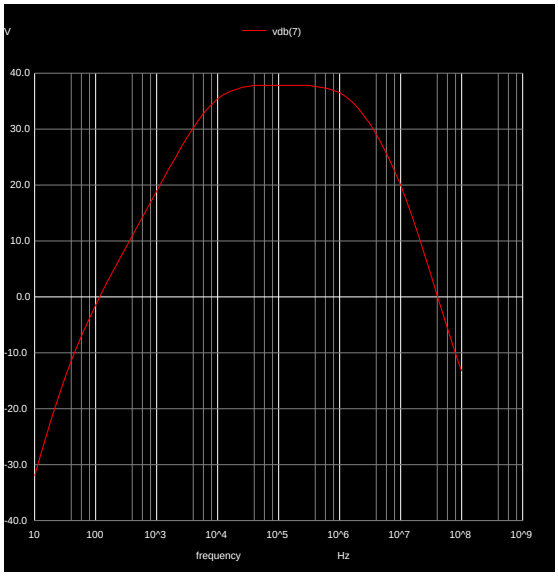

Gain in stage 2 (dB)
100
50
0
-50
-100
-150
V(7)(dB)
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
f(Hz)

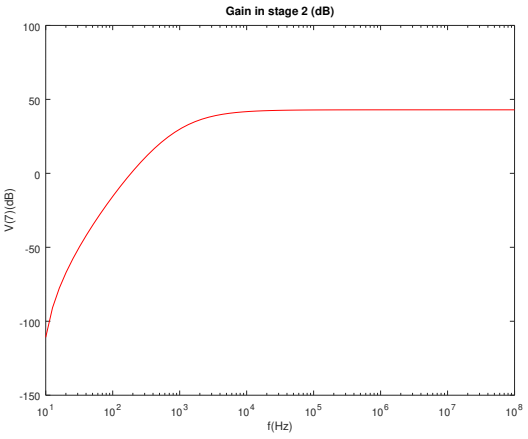
The lower 3dB cut-off point is at $f = 5484.4Hz$ As we can see, the lower cut-off point is accurrate, but this model does not deal well with the higher cut-off point.

4 Conclusion

In this laboratory assignment the objective of building an audio amplifier was achieved. The cost of the circuit was of $2102.508MU$ and the merit 3.238.

The results from both the theoretical analysis using octave and the circuit simulation using ngspice appear to roughly match, as we can see in the following figure and table:





We can see that the gain for the second stage is fairly different. The simulation has a drop at around 10^6 Hz, while the theoretical model mantains steadily at around 45dB.

Comparing all of the other values, we get the following table:

Table 5: Values of gain and input and output impedance for theoretical and simulation analysis

	Mat	Sim
Zi1	484.43	563.83
Zo1	886.28	-
Zi2	8598.9	-
Zo2	0.30217	10.07
Gain1	48.392 dB	-
Gain2	-0.0702 dB	-
GainT	48.322 dB	37.904 dB
LowCOP	5.48 kHz	8.88 kHz
BdWth	-	1.60 MHz
Cost	2102.508 MU	2102.508 MU

We can compare directly the input impendance for stage 1, Zi1: The theoretical model gives a lower value, about 86% of the simulated one. Same goes for the output impedance, Zo2, where the theoretical analysis gives ≈ 0.3, which is only around 3% of what the simulation gives.

We can conclude that there are various differences between the theoretical and simulation analysis. These can be attributed to the various aproximations made in the theoretical analysis, in the ideal transistor model for example, while the simulation uses a comparatively accurate spice model. The simulation therefore gives more credible values, closer to reality.