Exercícios

Analise fragmentos de código seguintes, detete os erros e indique que circuitos lógicos resultarão da síntese.

Exercício 1

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity 123_unknown is
  generic (N : positive := 8);
  port(sel : std_logic;
       input0 : std_logic_vector(n-1 downto 0);
       input1 : std_logic_vector(n-1 downto 0);
       output : std_logic_vector(n-1 downto 0));
end 123_unknown;

architecture Behavioral of 123_unknown is
begin
    if (sel = '0') then
      output <= input0;
    else
      output <= input1;
    end if;
end Behavioral;
```

3 tipos de erros

Exercício 2

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity unknown2 is
  port(enable  : in  std_logic;
       inputs  : in  std_logic_vector (1 downto 0);
       outputs : out std_logic_vector (1 downto 0));
end unknown2;

architecture BehavAssign of unknown2 is
begin
    outputs <= "0000" when (enable = '0')  else
               "0001" when (inputs = "00") else
               "0010" when (inputs = "01") else
               "0100" when (inputs = "10") else
               "1000" when (inputs = "11");
end BehavAssign;
```

2 tipos de erros

Exercício 3

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity unknown3 is
    port(operand0 : in  std_logic_vector(3 downto 0);
         operand1 : in  std_logic_vector(3 downto 0);
         result   : out std_logic_vector(7 downto 0));
end unknown3;

architecture Behavioral of unknown3 is
begin
 result <= unsigned(operand0) + unsigned(operand1);
end Behavioral;
```

3 tipos de erros

Exercício 4

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity unknown4 is
  generic(N    : positive := 4);
  port(  reset, clk, enable        : in  std_logic;
         dataIn                    : in  std_logic(N-1 downto 0);
         dataOut                   : out std_logic(N-1 downto 0));
end unknown4;

architecture Behav of unknown4 is
begin
  process(clk, reset)
  begin
    if (rising_edge(clk)) then
      if (enable = '1') then
        if (reset = '1') then      dataOut <= "0000";
        else                       dataOut <= dataIn;
        end if;
      end if;
    end if;
  end process;
end Behav;
```

2 tipos de erros

Exercício 5

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity unknown5 is
  port(  clk, loadEn, dirLeft      : in  std_logic;
         dataIn                    : in  std_logic_vector(7 downto 0);
         dataOut                   : out std_logic_vector(7 downto 0));
end unknown5;
architecture RTL of unknown5 is
begin
  process(clk)
  begin
    if rising_edge(clk) then
      if (loadEn = '1') then
        dataOut <= dataIn;
      elsif (dirLeft = '1') then
        dataOut <= dataOut & '0';
      else
        dataOut <= dataOut(7) & dataOut;
      end if;
    end if;
  end process;
end RTL;
```

2 tipos de erros