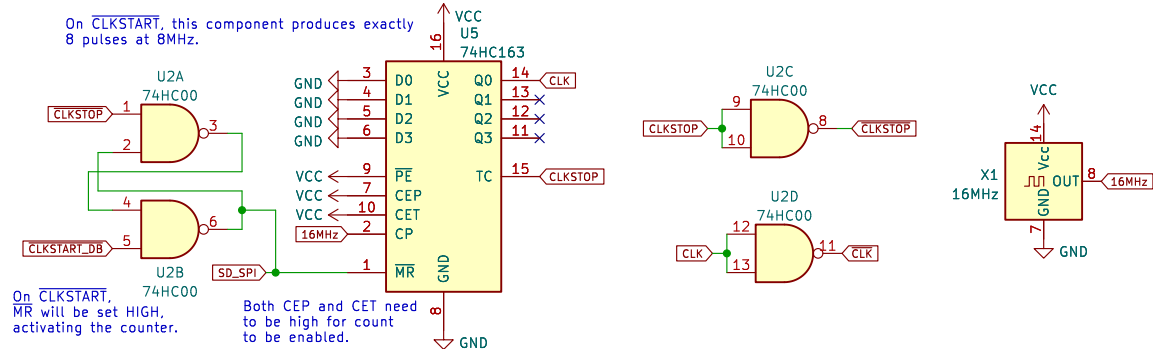
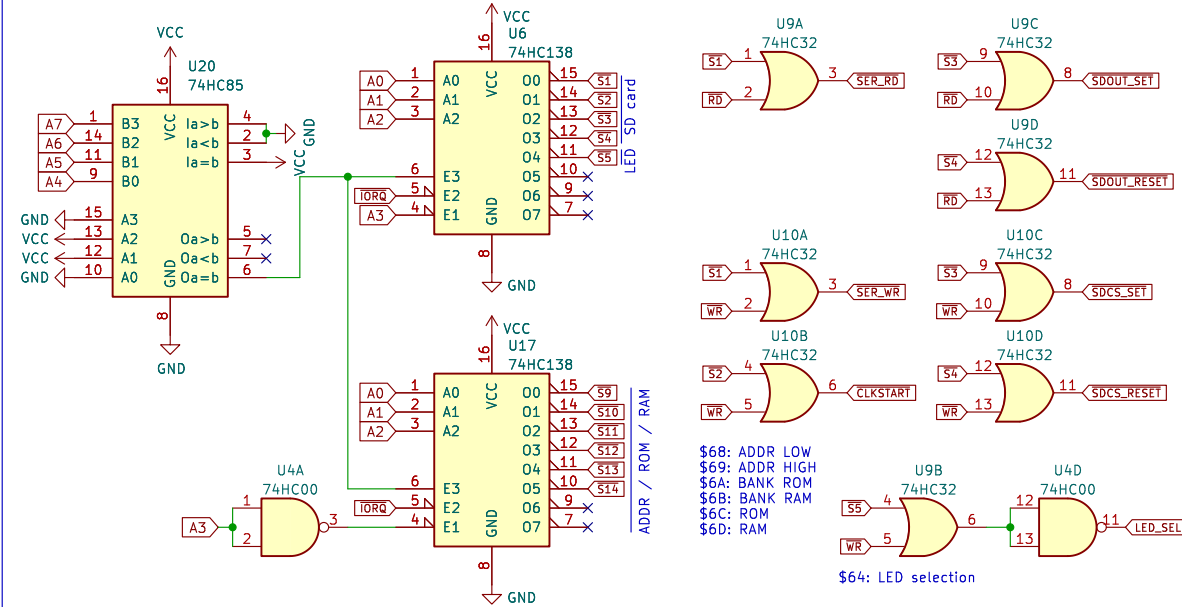


CLOCK COMPONENT



SELECTION COMPONENT



```

out $60: SEB_WR is pulled low, loading the values on the data bus into the out register.
out $61: CLKSTART is pulled low, starting the counter circuit and pushing a byte into the SD card while simultaneously reading a byte.
out $62: SDCS_SET is pulled low, pulling CS low, activating the SD card.
out $63: SDCS_RESET is pulled low, pulling CS high, deactivating the SD card.

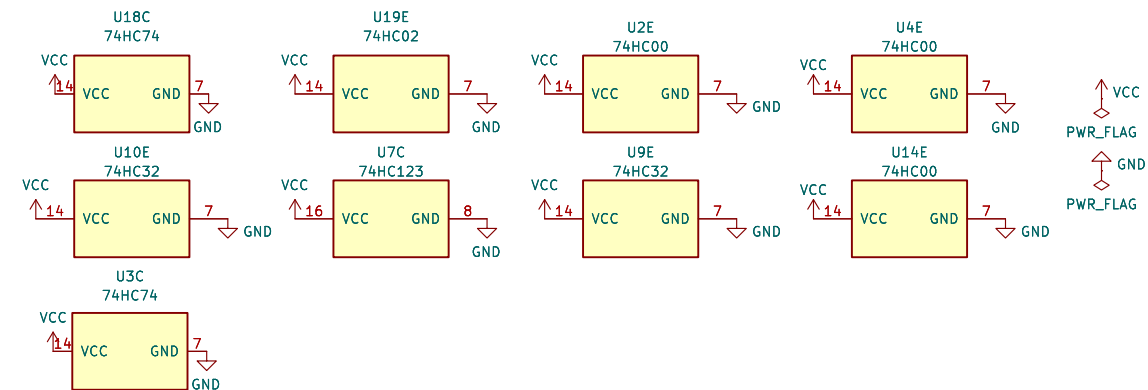
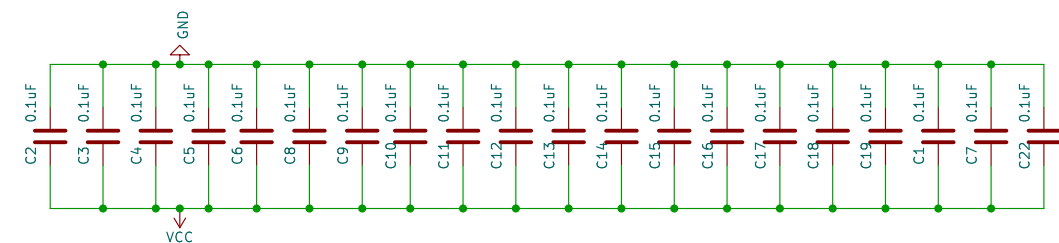
```

```

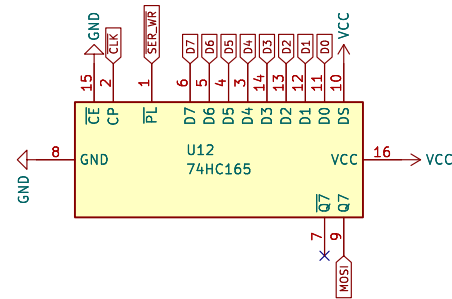
in $60: SER_RD is pulled low, reading from the in register.
in $61: Does nothing
in $62: SDOUT_SET is pulled low, pulling MISO low via a 10k resistor.
in $63: SDOUT_RESET is pulled low, pulling MISO high via a 10k resistor.

```

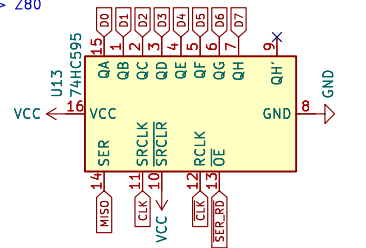
When no card is present, the output of the SD card will follow the output of the SET/RESET latch, however if a card is present, though unresponsive, it will not follow and the same (high) output will be received.



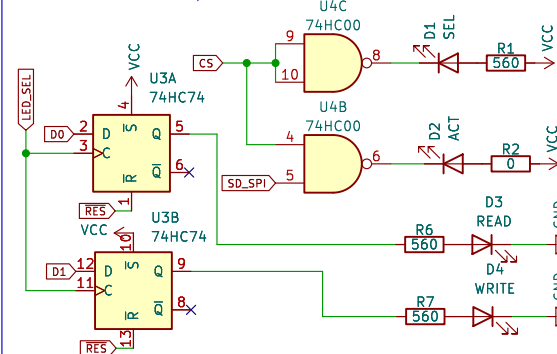
SHIFT REGISTER Z80 -> SD
OUT REGISTER



SHIFT REGISTER SD → Z80
IN REGISTER



Two LEDs show whether the SD card is selected via the CS line and whether signals are sent to the SD card. Another two LEDs show I/O on the RAM and ROM chips.



Set 16 bit address for the ROM and RAM chips. The logic circuitry for the \overline{CP} signal uses the remaining gates on the 74HC04, 74HC00 and 74HC21 chips.

- * $\overline{S5}$ and \overline{WR} both LOW, CP for lower byte ADDR HIGH
- * $\overline{S6}$ and \overline{WR} both LOW, CP for upper byte ADDR HIGH

