CLOCK COMPONENT

On $\overline{\text{CLKSTART}}$, this component produces exactly 8 pulses at 8MHz.

U2A 74HC00 — CLKSTOP, CLKSTART_DB

U2B 74HC00

On $\overline{\text{CLKSTART}}$, $\overline{\text{MR}}$ will be set HIGH, activating the counter.

U5 74HC163 — SD_SPI, 16MHz, CLK, CLKSTOP

Both CEP and CET need to be high for count to be enabled.

U2C 74HC00 — CLKSTOP

U2D 74HC00 — CLK

X1 16MHz — 16MHz

SHIFT REGISTER Z80 –> SD OUT REGISTER

U12 74HC165 — SER_WR, MOSI

SD CARD S/R LATCHES

U14A 74HC00 — SDOUT_SET

U14B 74HC00 — SDOUT_RESET, R4 10k, MISO

U14C 74HC00 — SDCS_SET, CS

U14D 74HC00 — SDCS_RESET, CS

ROM and RAM chips

Expose 2x64kb of memory via bank switching

Addresses are set via two 74HC273 buffers
Bank switching via two D-type flip-flops

U15 SST39SF010 — ROM16, WR, S13, RD

U1 CY62128ELL-45SXI — RAM16, CS1, CS2, OE, WE, S14

SELECTION COMPONENT

U20 74HC85

U6 74HC138 — IORQ, A3, LED SD card

U17 74HC138 — IORQ, A3, ADDR / ROM / RAM

U4A 74HC00

U9A 74HC32 — SER_RD

U9C 74HC32 — SDOUT_SET

U9D 74HC32 — SDOUT_RESET

U10A 74HC32 — SER_WR

U10C 74HC32 — SDCS_SET

U10B 74HC32 — CLKSTART

U10D 74HC32 — SDCS_RESET

$68: ADDR LOW
$69: ADDR HIGH
$6A: BANK ROM
$6B: BANK RAM
$6C: ROM
$6D: RAM

U9B 74HC32

U4D 74HC00 — LED_SEL

$64: LED selection

out $60: $\overline{\text{SER\_WR}}$ is pulled low, loading the values on the data bus into the out register.
out $61: $\overline{\text{CLKSTART}}$ is pulled low, starting the counter circuit and pushing a byte into the SD card while simultaneously reading a byte.
out $62: $\overline{\text{SDCS\_SET}}$ is pulled low, pulling $\overline{\text{CS}}$ low, activating the SD card.
out $63: $\overline{\text{SDCS\_RESET}}$ is pulled low, pulling CS high, deactivating the SD card.

in $60: $\overline{\text{SER\_RD}}$ is pulled low, reading from the in register.
in $61: Does nothing
in $62: $\overline{\text{SDOUT\_SET}}$ is pulled low, pulling MISO low via a 10k resistor.
in $63: $\overline{\text{SDOUT\_RESET}}$ is pulled low, pulling MISO high via a 10k resistor.

When no card is present, the output of the SD card will follow the output of the SET/RESET latch, however if a card is present, though unresponsive, it will not follow and the same (high) output will be received.

SHIFT REGISTER SD –> Z80 IN REGISTER

U13 74HC595

Two LEDS show whether the SD card is selected via the CS line and whether signals are sent to the SD card. Another two leds show I/O on the RAM and ROM chips.

U3A 74HC74 — LED_SEL, D0

U3B 74HC74 — D1

U4C 74HC00 — CS, D1 SEL, R1 560

U4B 74HC00 — SD_SPI, D2 ACT, R2 0

D3 READ, R6 560

D4 WRITE, R7 560

MULTIVIBRATOR DELAY COMPONENT

10k resistor with 22pF cap gives
t = 0.45RC = 0.1us delay between consecutive pulses

R3 10k, C20 22pF, U7A 74HC123 — CLKSTART

1k resistor with 22pF cap gives
0.45*RC = 0.01us active low pulse

R5 1k, C21 22pF, U7B 74HC123 — CLKSTART_DB

Set 16 bit address for the ROM and RAM chips. The logic circuitry for the CP signal uses the remaining gates on the 74HC04, 74HC00 and 74HC21 chips.

* $\overline{\text{S5}}$ and $\overline{\text{WR}}$ both LOW, CP for lower byte ADDR HIGH
* $\overline{\text{S6}}$ and $\overline{\text{WR}}$ both LOW, CP for upper byte ADDR HIGH

U8 74HC273 — Lower address byte

U11 74HC273 — Upper address byte

U19A 74HC02

U19C 74HC02

U18A 74HC74 — ROM16

U19B 74HC02

U18B 74HC74 — RAM16

U19D 74HC02

0.1uF: C2, C3, C4, C5, C6, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C1, C7, C22

U18C 74HC74

U19E 74HC02

U2E 74HC00

U4E 74HC00

U10E 74HC32

U7C 74HC123

U9E 74HC32

U14E 74HC00

U3C 74HC74

PWR_FLAG, PWR_FLAG

SD CARD

J3 SD Card — CS, SCK, MOSI, MISO, VCC, GND

PORT 2 CARTRIDGE SLOT

J2 P2000T Port 2

Sheet: /
File: port2-sdcard-interface.kicad_sch

Title: Philips P2000T SD-CARD SLOT2 cartridge

Size: A3	Date: 2024-04-09	Rev: rev4
KiCad E.D.A. kicad 7.0.10		Id: 1/1