

## ■ Features, Benefits and Applications

- Any frequency between 1 and 80 MHz with 6 decimal places of accuracy
- 100% pin-to-pin drop-in replacement to quartz-based TCXO
- Ultra low phase jitter: 0.5 ps (12 kHz to 20 MHz)
- Frequency stability as low as  $\pm 10$  PPM
- LVCMOS/LVTTL compatible output
- Standby or output enable modes
- Three industry-standard 4-pin packages: 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm
- Contact SiTime for the following options:
  - SoftEdge™ configurable rise/fall time for EMI reduction or driving higher loads
  - 2.5 x 2.0 footprint compatible package
- Outstanding silicon reliability of 2 FIT (10x improvement over quartz-based devices)
- Ultra short lead time
- Ideal for high-speed serial protocols such as: SATA, SAS, Ethernet, PCI Express, etc.

## ■ Specifications

## Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	–	80	MHz	
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of Initial tolerance at 25 °C, operating temperature, rated supply voltage variation and load variation (15% pF $\pm 10\%$ )
		-20	–	+20	PPM	
		-25	–	+25	PPM	
		-50	–	+50	PPM	
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	Any supply voltage between 2.5 V and 3.3V is supported in increment of 0.1 V. Contact SiTime for guaranteed performance specs for supply voltages not specified in this table.
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	31	33	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	29	31	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
Standby Current	I_std	–	–	70	$\mu$ A	Vdd = 2.5 V, 2.8V or 3.3V, $\overline{ST}$ = GND, output is Weakly Pulled Down
		–	–	10	$\mu$ A	Vdd = 1.8 V, $\overline{ST}$ = GND, output is Weakly Pulled Down
Duty Cycle	DC	45	–	55	%	All Vdds.
Rise/Fall Time	Tr, Tf	–	1.5	2	ns	15 pF load, 10% - 90% Vdd, all Vdds
		–	3.6	–	ns	30 pF load, 10% - 90% Vdd, all Vdds
		–	4.6	–	ns	45 pF load, 10% - 90% Vdd, all Vdds
Output Voltage High	VOH	90%	–	–	Vdd	IOH = -7 mA, IOL = 7 mA, (Vdd = 3.3 V)
Output Voltage Low	VOL	–	–	10%	Vdd	IOH = -4 mA, IOL = 4 mA, (Vdd = 2.8 V and Vdd = 2.5 V)
		–	–	–	Vdd	IOH = -2 mA, IOL = 2 mA, (Vdd = 1.8 V)
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z_in	–	100	250	k $\Omega$	
Startup Time	T_start	–	6	10	ms	Measured from the time Vdd reaches its rated minimum value
OE Enable/Disable Time	T_oe	–	–	150	ns	f=80 MHz, all Vdds. For other frequencies, T_oe = 100 ns + 3 cycles
Resume Time	T_resume	–	6	10	ms	Measured from the time ST pin crosses 50% threshold
RMS Period Jitter	T_jitt	–	1.5	2	ps	f = 75 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	2	3	ps	f = 75 MHz, Vdd = 1.8 V
RMS Phase Jitter (random)	T_phj	–	0.5	1	ps	f = 75 MHz, Integration bandwidth = 12 kHz to 20MHz, All Vdds
Aging	F_aging	–	$\pm 1$	–	PPM	1 <sup>st</sup> year, 25°C

## Note:

1. All electrical specifications in the above table are measured with 15pF output load, unless stated otherwise in the Condition.

## ■ Specifications (Cont.)

## Pin Description Tables

Pin #1 Functionality
<b>OE</b>
H or Open <sup>[2]</sup> : specified frequency output
L: output is high impedance. Only output driver is disabled.
<b><math>\overline{\text{ST}}</math></b>
H or Open: specified frequency output
L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I <sub>std</sub>

Pin Map	
Pin	Connection
1	OE/ $\overline{\text{ST}}$
2	GND
3	CLK
4	VDD

## Absolute Maximum Table

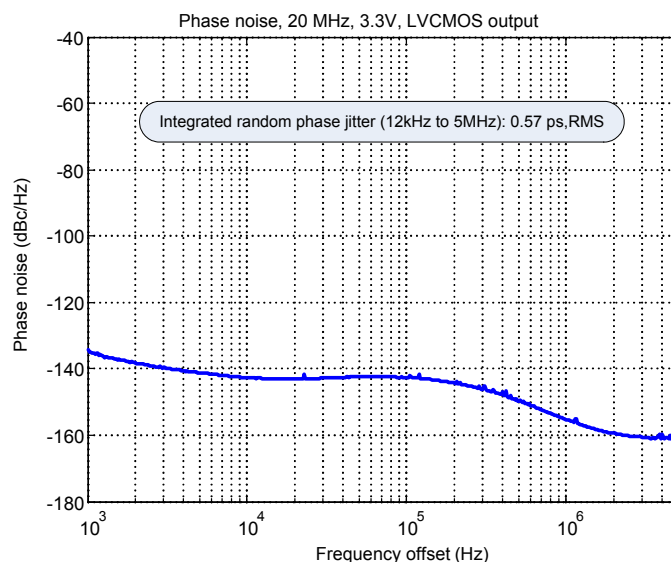
Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125°C, Process, VDD (0 to 3.65 V)	1,000+	–	years

## Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

## Phase Noise Plot



## Note:

- A resistor of <100 kΩ between OE/ $\overline{\text{ST}}$  pin and VDD is recommended for all voltages.

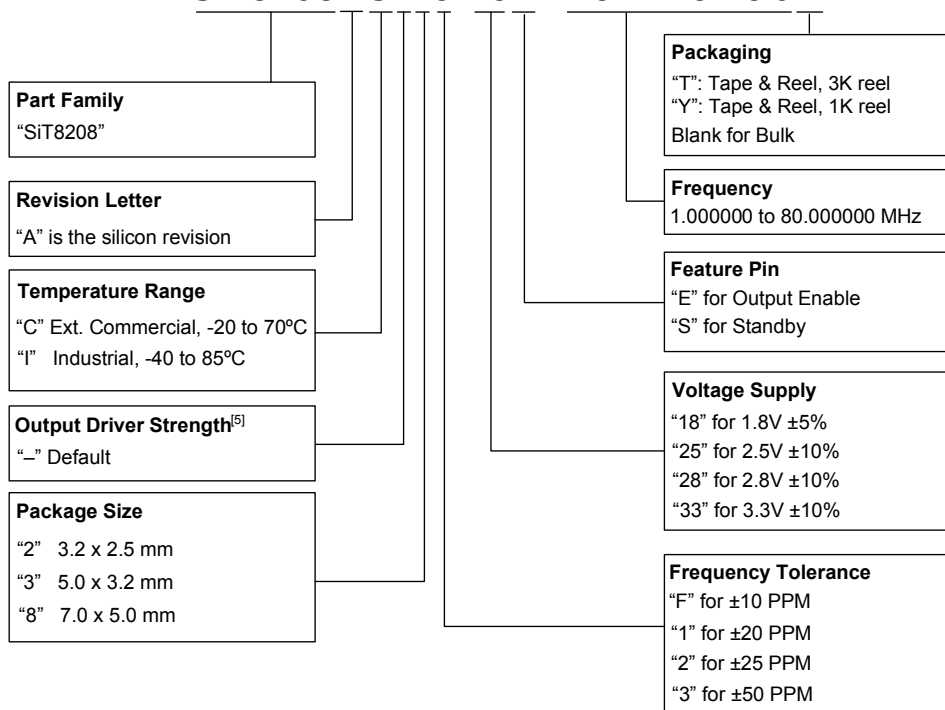
## ■ Dimensions and Land Patterns

Package Size – Dimensions (Unit: mm) <sup>[3]</sup>	Recommended Land Pattern (Unit: mm) <sup>[4]</sup>
<p><b>3.2 x 2.5 x 0.75 mm</b></p>	
<p><b>5.0 x 3.2 x 0.75 mm</b></p>	
<p><b>7.0 x 5.0 x 0.90 mm</b></p>	

**Notes:**

- Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
- A capacitor of value 0.1  $\mu$ F between Vdd and GND is recommended.

## SiT8208AC-23-25E-75.123456T

**Note:**

5. Contact SiTime for different drive strength options for driving higher loads or reducing EMI.

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