INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR
Department of Computer Science and Engineering
CSL 203: **Computer System Organization**
End Sem Exam
Semester -III

Date: 18/11/2022 (Friday)
Time: 10:00 AM to 01:00 pm

Duration: 3 Hours

Max. Marks: **50**

Important Instructions:

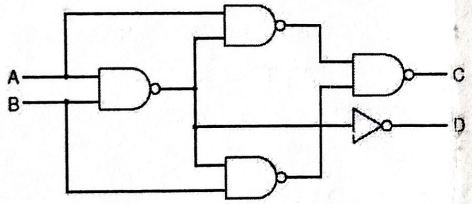
- All the questions are compulsory.
- Write all the subparts of each question together.

Q1 (a) Consider two system implementations T1,T2 of the same ISA. Here instructions are divided into four classes I1,I2,I3,I4 as per their CPI. 3 [CO2]
T1= clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3
T2=clock rate of 3 GHz and CPIs of 2, 2, 2, and 2
Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster? What is the global CPI for each implementation? Find the clock cycles required in both cases.

(b) Consider a processor supporting 12 bit long instructions and 1KB memory space. If there exists two 1-address instructions, then how many 0-address instructions can be formulated? 2 [CO4]

(c) Answer the following: 5 [CO4]
(i) Why is it necessary to save and restore the value of Frame Pointer in processor stack?
(ii) Why number of misses in cache decrease by increasing associativity?
(iii) Why is there a need to match the tag bits while locating a cache line in cache memory?
(iv) Why is micro-programmed control implementation of control unit efficient than the hardwired implementation?
(v) Why is multiple bus data-path design of a processor better than single bus data-path design?

Q2 (a) What does this circuit do? Elaborate. 3 [C01]



(b) A 16-bit ALU is built up of 16 1-bit ALUs, each one having an add time of 10 nsec. If there is an additional 1 nsec delay for propagation from one ALU to the next, how long does it take for the result of a 16-bit add to appear? 2 [CO3]

(c) Perform the following using Booths Multiplication. (-100)*52. Show all the intermediate steps clearly. Also use modified Booth's algorithm and justify its advantage over Booth's Algorithm. 5 [CO1]

Q3 (a) A computer has a two-level cache. Suppose that 60% of the memory references hit on the first level cache, 35% hit on the second level, and there is 5% miss. The access times are 5 nsec, 15 nsec, and 60 nsec, respectively, where the counting of time for the level 2 cache and memory start as soon as they are required (e.g., a level 2 cache access does not start until the level 1 cache miss occurs). What is the average access time? 3 [CO3]

(b) Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8, 12,0, 12,8 — 3 [CO3]

(c) A RAM chip has a capacity of 1024 words of 8 bits each. What is the number of 2-to-4 decoders with enable lines needed to construct a 16K x 16 RAM system? Show with neat diagram. — 4 [CO3]

Q4 (a) Assume there is a list of n records in memory starting at location N where each student record contains (Studenty Id, TestScore 1, TestScore 2,...TestScore k) i.e. k scores for each student. Assume memory to be byte addressable and each field of a record occupies 8 bytes. Write a RISC-style program for computing the sum of the scores on each test and store these sums in memory word locations at addresses Total, Total+8, ... and so on. The number of tests k is larger than the number of register in the processor.
Using nested loops and assuming the memory area used to store the sums is not initially cleared, write the RISC-style program and clearly comment the steps of execution. — 5 [CO4]

(b) A single bus CPU consists of four general purpose registers, namely, R0.....R3, ALU, MAR, MDR, PC, ALU, and IR (Instruction Register). Assuming suitable microinstructions, write a micro-routine for the instruction, ADD R0, R1. State the design changes for the same using hardwired control. — 5 [CO1]

Q5 (a) The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction.
Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. What is the number of clock cycles required for completion of execution of the sequence of instructions. Show the detailed steps. — 5 [CO2]

(b) Write control steps for the instruction "SUB R1,R2,R3". Write microroutine for the corresponding control steps of this instruction. The set of control signals are given in the table below: — 5 [CO2]

Micro - instruction	..	PC_{in}	PC_{out}	MAR_{in}	Read	MDR_{out}	IR_{in}	Y_{in}	Select	Add	Z_{in}	Z_{out}	$R1_{out}$	$R1_{in}$

****