INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR

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B. Tech. Subject Name: Digital Electronic Circuits

Instructions: This question paper consists of **three** pages. Answers to parts of one question must be written in one place. Otherwise, they will **not** be checked. Answer **all five** questions. All questions have been adequately explained and need no further clarification.

1 (a) The state able of a synchronous sequential circuit with one input and one output is shown in Table 1. You must **not** perform any state reduction of this fsm (finite state machine). For the state assignment **A = 001**; **B = 010**; **C = 011**; **D = 100**; and **E = 101**, obtain a realization of the circuit using negative edge-triggered ***SR*** flip-flops. Write the excitation table of an ***SR*** flip-flop. Write the state transition table, the binary excitation table and the output table for the given circuit. Minimize each excitation input and the output function of the required combinational logic. Draw the circuit diagram. [14]

Present State	Next state, output	
	x = 0	*x = 1*
A	A, 0	B, 0
B	C, 0	D, 0
C	A, 0	D, 0
D	E, 0	D, 1
E	A, 0	D, 1

Table 1: State table for a synchronous sequential circuit (Question 1 (a)).

(b) Show how an ***SR*** flip-flop (FF) can be converted to a ***JK*** FF. That is, you have actually an *SR* FF which will be made to behave as a *JK* FF. For this, you have to add two external inputs *J* and *K* and a combinational circuit which drives the excitation inputs of the existing *SR* FF. Write the complete conversion table and design the combinational circuit with minimum possible size. Draw the logic diagram of the complete circuit. [6]

2 (a) Design and implement a **synchronous modulo-5 up/down** counter using he minimum number of negative edge-triggered ***JK*** flip-flops (FFs). Let there be a control signal ***UP*** such that when ***UP=1***, the count progresses in the order 0,1,2,3,4,0, …; whereas, with ***UP=0***, the count will advance in the reverse order (i.e. 0,4,3,2,1,0, …). Write the excitation table of a *JK* FF. Derive the minimized equations for all the excitation inputs, showing all individual steps. Draw all relevant waveforms, showing the clock as the reference. Assume that **no lockout** will ever occur as the counter operates in any mode. [12]

P.T.O.

(b) Fibonacci sequence is represented by the series of numbers 0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233 ... where the next number (or term) is computed as the sum of previous two terms. That is, $\mathbf{t_n = t_{n-1} + t_{n-2}}$ where $\mathbf{t_0 = 0}$ and $\mathbf{t_1 = 1}$. Consider the control unit of a Fibonacci sequence generator which computes the value of $\mathbf{t_n}$ for a given value of $\mathbf{n \leq 13}$ (so that the result can be stored in an 8-bit register). You can assume the presence of an 8-bit adder and 8-bit registers with active low parallel (load) enable signal. As soon as power is switched on, the circuit starts operation by loading two registers with values of $\mathbf{t_0}$ and $\mathbf{t_1}$. A halt signal would indicate the end of the process when the value of $\mathbf{t_n}$ will be available in a register. Noting that iterative addition is involved, draw the block diagram of the overall architecture. Next, show the behavior of the Fibonacci sequence generator by an **ASM** (Algorithmic State Machine) diagram. Clearly mention the operations taking place during each of the states of the Fibonacci sequence generator which is modeled as a **Moore** machine. [8]

3.(a) Draw the complete circuit of a two-input TTL (transistor-transistor logic) **NOR** gate with a totem-pole configuration at the output stage. You must **not** draw a NAND gate with inverted variables (e.g. $\overline{A}$ and $\overline{B}$) as inputs to realize OR/NOR gate. What role do the phase-splitter transistors play? Also explain the need of the diode in the pull-up element of the totem-pole output stage. [8]

(b) Define fan-out of a TTL gate. You are asked to find how many standard TTL 2-input NAND gates can be driven by an LS-TTL 2-input NAND gate. Given that for an LS-TTL 2-input NAND gate, the maximum vales of the currents are as follows: $I_{OH} = -400\,\mu A$; $I_{OL} = 8\ mA$; $I_{IH} = 20\,\mu A$ and $I_{IL} = -0.4\,mA$. Whereas, for a standard TTL 2-input NAND gate, the maximum vales of the currents are as follows: - $I_{OH} = -400\,\mu A$; $I_{OL} = 16\ mA$; $I_{IH} = 40\,\mu A$ and $I_{IL} = -1.6\,mA$. [4]

(c) Draw the circuit diagram for a 5-bit shift register made of ***D*** FFs such that the complementary output ($\overline{Q}$) of the *rightmost* FF is connected to the *D* input of the *leftmost* FF. Assume that the initial state of this synchronous sequential circuit is one in which the **leftmost** FF is in **set** state while all the remaining FFs are in **reset** states. Write the complete state table for this sequential circuit, starting with the given initial state. Mention the length of a cycle, if any exists in the state transition diagram of the circuit. Derive the minimum decoding logic for the initial state (do not simply state it). [8]

4 (a) Draw the complete gate diagram of a ***positive edge-triggered D***-type flip-flop (*D* FF) constructed using only NAND gates. Show that with the *D* input either at 0 or 1, when the clock **changes** from 0 to1, the output *Q* will certainly follow the input *D*. **Also** show that now with the clock **remaining** at 1, **even if** *D* changes from 1 to 0 or from 0 to 1, the output *Q* will remain **unchanged**. Show how active **low asynchronous preset** and **clear** signals can be provided for this FF, which would cause the output *Q* to go to 1 and 0 respectively, regardless of all other inputs. [10]

(b) Draw the complete transistor diagram of a 4-transistor **MOS** dynamic memory cell. Briefly explain the read and the write operations of this cell. Also, explain how data refreshing operation is performed. [10]

5 (a) How does a **Moore model** of a synchronous sequential circuit differ from a **Mealy model**? Consider a sequence detector that produces an output 1 each time the sequence 1010 or 1011 appears at the input. Overlapping is allowed. For example, a valid input-output pattern may be as follows:

input x : 0 0 1 1 0 1 0 1 1 0 1 1 0 1 1 0 1 0 1 0 0 ...
output z : 0 0 0 0 0 0 1 0 1 0 0 1 0 0 1 0 0 1 0 1 0 ...

Draw the state diagram and write the state table of such a sequence detector if **Mealy model** is followed to describe the behavior of the circuit. Write the meaning of each state of this Mealy fsm in terms of past inputs associated with it. For example, state A: is the initial state in which the fsm is yet to get the start of either of the two given sequences. Finally, derive the state transition table and diagram of the above sequence detector corresponding to its **Moore model**. [10]

(b) A 2-input, 1-output synchronous sequential circuit is specified by the following state (and output) table (Table 2). Reduce the number of states by applying the **Partitioning** technique. Clearly show and explain in detail how successive partitions are generated at consecutive steps. Finally, determine the **equivalence partition** and write the **reduced state table** (with renamed states) for the given completely specified sequential circuit. [10]

Present State	Next state and output for different input conditions			
	$x_1x_2 = 00$	$x_1x_2 = 01$	$x_1x_2 = 11$	$x_1x_2 = 10$
A	A/0	A/0	B/0	B/0
B	G/0	G/0	D/0	B/0
C	F/0	G/1	H/1	B/0
D	G/0	G/0	B/0	D/0
E	E/0	G/1	H/1	B/0
F	E/0	G/1	H/1	D/0
G	G/0	F/0	B/0	D/0
H	E/0	D/1	H/1	B/0

Table 2: State table for a sequential circuit (Question 5 (b)).

***** End of the Question Paper *****