Autobalancing Analog Front End for Full-Range Differential Capacitive Sensing

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***Abstract*— The authors here propose an analog interface for differential capacitance estimation, able to reveal and quantify capacitive variations. Different from other works in the literature, the proposed interface can operate on a full-range scale. This solution takes inspiration from a preliminary work of the same authors, whose working principle is based on a modified De-Sauty AC bridge configuration; in particular, two (differential) capacitors and two resistors are employed, one of which is implemented by a voltage-controlled resistor (VCR). In this paper, the electronic interface has been redesigned to obtain full-range operation and a linear input–output characteristic. The implemented autobalancing mechanism controls the VCR generating a reference voltage following the sensor output. Simulation results in two different circuit configurations performed by OrCAD PSpice have shown a very good agreement with a theoretical model implemented in MATLAB/Simulink environment. In addition, an evaluation of the goodness of the experimental measurements at steady and unsteady conditions is given. Experimental tests on a discrete-component prototype have been carried out using an automated test equipment including National Instruments tools and a dedicated software in the LabVIEW environment. Measurements have shown satisfactory results, the standard deviation being on the order of 0.01, in the worst case. The linearity error has been evaluated as well, resulting in lower than 1% full scale.**

***Index Terms*— Analog circuits, bridge-based circuits, calibration, differential capacitive sensor, electronic interfaces.**

I. Introduction

CAPACITIVE sensors are able to sense and evaluate changes in physical or chemical quantities of interest through capacitive value variations related to modifications of the sensor geometry (e.g., distance between two capacitor plates/electrodes, overlapped area) or in the dielectric material (permittivity). In recent years, they have become progressively popular due to their versatility and suitability to perform simple and low cost measurements [1]–[6].

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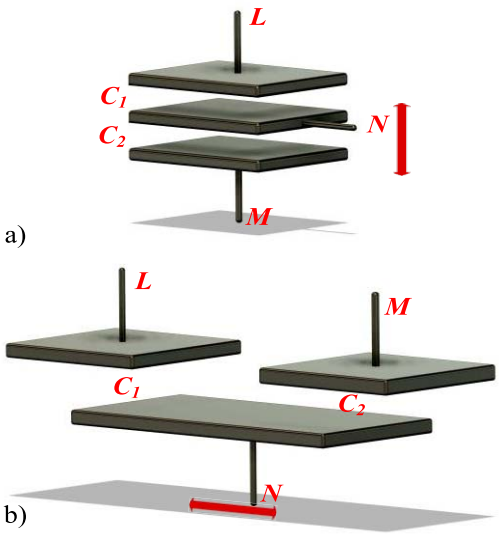

Fig. 1. Differential capacitive sensor structure (a) when the measurand influences the distance between plates and (b) when the measurand influences the overlapping area of plates.

Differential capacitive sensors are a subset of this kind of transducers showing an improved rejection of common mode interference in the case of low capacitive variations [7]. Accelerometers [8] and position sensors [9] are application fields where differential capacitive sensors are also employed. Fig. 1 shows two typical structures of differential capacitive sensors, consisting of a three-plate capacitive system where two of them are fixed and the third one is movable; in these cases, a geometric parameter variation occurs. Particularly, Fig. 1(a) is an example of a configuration where the measurand affects the distance between plates, whereas in Fig. 1(b), the variation is related to the overlapping area of plates.

Considering Fig. 1, it is possible to define the term x as a dimensionless variable, referred to the relative position of the sensor movable plate (connected to the output terminal N) with respect to the full scale (FS) [10]. In particular, the movable plate is either at the uppermost position in Fig. 1(a) or the leftmost position in Fig. 1(b) when $x = 1$, whereas it is either at the lowermost position in Fig. 1(a) or the rightmost position in Fig. 1(b) when $x = -1$. Clearly, $x = 0$ when the movable plate is in the central location. The value of C_1 and C_2 capacitances can be expressed as a function of the x-parameter according to (1) for plate distance variations and

to (2) for plate area variations, respectively

$$C_{1,2} = \frac{C_0}{(1 \mp x)} \tag{1}$$

$$C_{1,2} = C_0(1 \pm x). \tag{2}$$

The C_0 term is the nominal value of the C_1 and C_2 capacitances when the movable plate is at the rest position. Therefore, the two relative capacitors change their values in a complementary way with respect to the measurand. In differential capacitive systems, the readout circuit evaluates the difference between two capacitances rather than an absolute value of a single capacitance, so that the x parameter can be expressed as in (3), which is valid for both the configurations shown in Fig. 1 [10]

$$x = \frac{C_1 - C_2}{C_1 + C_2}. \tag{3}$$

II. Application Scenario

Capacitive sensing is typically performed by an indirect measurement through suitable interface electronic circuits for signal analysis and processing. Capacitive sensor front ends are implemented in a wide variety of topologies depending on the desired output signal. The interfaces presented in the literature are typically based on the following methods: capacitance-to-voltage conversion [11], capacitance-to-current conversion [12], capacitance-to-frequency or capacitance-to-time conversion [13], and switched-capacitor-based analog-to-digital conversion [14], [15]. Some of them are also performing a direct analog-to-digital conversion of the output signal [16], [17].

Bridge-based front ends have been employed for capacitive sensors in some dedicated topologies where sensor variations cause the bridge unbalance [18]. A recent work has demonstrated that high sensitivity and other features of the classical Wheatstone bridge can be improved by using an "autobalancing" architecture [19].

Concerning differential capacitive sensing, many interfaces have recently proposed, mainly based on either operational amplifiers [16], [20] or capacitance-to-voltage conversions [21]. Bridge-based differential capacitive circuits have been employed, for instance, to reject common-mode noise [22]. Impedance measurements might require AC excitation signals due to their transfer function dependence on frequency [23]. In this case, the sensor plates are driven by a square/sinusoidal wave signal [24] which serves as reference generator in a synchronous demodulator system, in order to be able to measure signals with a reduced signal-to-noise ratio [25].

Recently, Ferri *et al.* [26], [27] have presented works about differential capacitance evaluation. In this paper, the most important improvement is the effective redesign of the electronic interface that, by including a different feedback mechanism, allows to obtain a full-range linear input–output characteristic. In Sections III–V, a complete theoretical analysis and description of the, here, proposed interface is reported, and novel simulations and experimental results are shown.

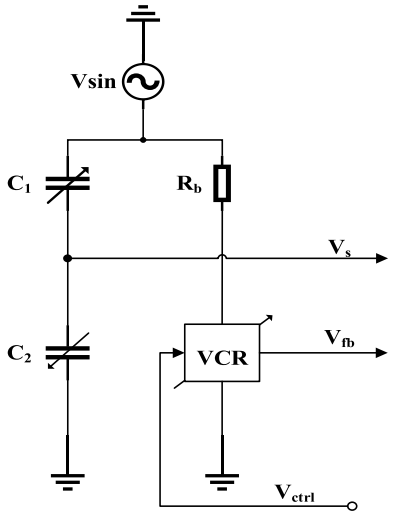

Fig. 2. Bridge-based (auto) balancing approach.

III. Proposed Approach

The works in [26] and [27] are based on an automatic modified De-Sauty AC bridge configuration, where two (differential) capacitors and two resistors are employed, one of which implemented by a voltage-controlled resistor (VCR), as shown in Fig. 2. A feedback loop, through tuning of the VCR, allows handling the bridge output voltage evaluating the differential capacitance variation.

The main issue of this solution is the nonlinear relation between the interface output signal V_{ctrl} and the measurand x which, together with a reduced "autobalance region," might limit the potential interface application fields.

The authors here propose a new architecture for an analog interface that overcomes these limitations. The proposed approach is here described, whereas experimental validation of a proof-of-concept implementation is given in Sections IV and V.

A. Working Principle

Due to the capacitive behavior of the considered differential sensor, sensor excitation is usually a (supply) sinusoidal signal $V_{\text{sin}}(t) = |V_{\text{sin}}| \cdot \sin(\omega_{\text{sin}} \cdot t)$ and the sensor output $V_S(t)$ is a sinusoidal signal as well. $V_S(t)$ ultimately depends on the measurand x as in

$$V_S(t) = (x + 1) \cdot \frac{1}{2} V_{\text{sin}}(t). \tag{4}$$

For the sake of simplicity, phasor notation can be adopted, i.e., $V_{\text{sin}}\angle 0^\circ = V_{\text{sin}} = |V_{\text{sin}}| \cdot \sin(\omega_{\text{sin}} \cdot t)$ and $V_S\angle 0^\circ = V_S = |V_S| \cdot \sin(\omega_{\text{sin}} \cdot t)$, encapsulating the frequency and time dependence and supposing that the phase offset of the sensor output is negligible.

Generally speaking, the autobalancing strategy can be considered a negative feedback-based system (as graphically depicted in Fig. 3(a), where G is an amplifying/attenuating block), whose aim is to minimize or null a certain error signal. In particular, the advantage of such a solution is that the actual input–output relationship only depends on the

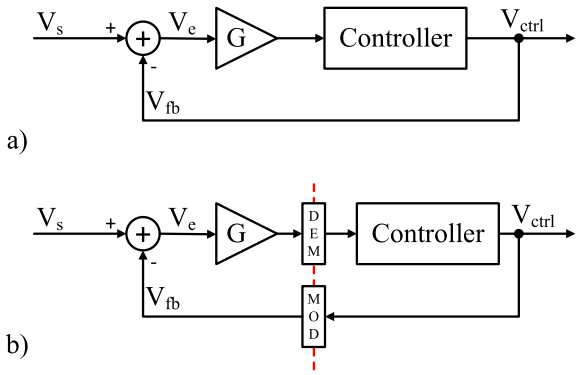

Fig. 3. (a) Schematic of the generic autobalancing system. (b) Baseband versus bandpass signals in the proposed autobalancing approach.

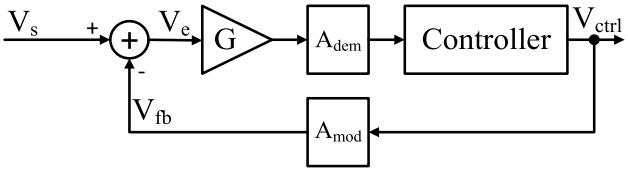

Fig. 4. Baseband simplification of the proposed feedback circuit in the time domain.

feedback gain; this can simplify the implementation of the integrated interface, where the VCR can easily be realized by means of a MOS transistor operating in the ohmic region. According to well-known results of the automatic control theory, such a nulling effect can be obtained using a very high open-loop gain and/or integral control strategy. If enough gain–bandwidth product is provided, the previously described feedback system can be used for bandpass signals as well (i.e., when signals of interest are phasors), but integral control strategy is no more applicable (it holds for baseband signal only). In particular, in the considered scenario, the error signal $V_e = V_S - V_{\rm fb} = (|V_S| - |V_{\rm fb}|) \cdot \sin(\omega_{\rm sin} \cdot t)$ is the difference between the differential capacitive sensor output V_S and a reference feedback signal $V_{\rm fb}$. If unitary feedback is considered, $V_{\rm fb} = V_{\rm ctrl}$, where $V_{\rm ctrl} = |V_{\rm ctrl}| \cdot \sin(\omega_{\rm sin} \cdot t)$ is the controller output signal. When the balance is reached, $V_{\rm ctrl} = V_S$ and $x \propto |V_{\rm ctrl}|$, as better detailed in the following.

Unfortunately, the information of interest, i.e., the amplitude of the phasor $V_{\rm ctrl}$, cannot be easily estimated or further processed. Since the excitation signal is readily available, the proposed solution uses a (synchronous) demodulator in the forward path and a modulator in the feedback path, as depicted in Fig. 3(b), allowing switching from bandpass to baseband domains and vice versa. The intrinsic advantage is that a high gain factor, which could be difficult to be realized for high operating frequencies of bandpass, is no longer needed and a regular integral control strategy can be applied to the baseband signal. Indeed, the information of interest is the amplitude of phasor V_S and, consequently, the two schemes in Fig. 3(a) and (b) can be merged as in Fig. 4, where the dependence on the sinusoidal excitation signal disappears and the MOD/DEM stages only affects signal amplitudes ($A_{\rm mod}$ and $A_{\rm dem}$ blocks). When integral control is applied and both the forward (i.e., $A = G \cdot A_{\rm mod} \cdot s^{-1}$ in Laplace domain) and feedback ($B = A_{\rm dem}$) paths are linear, the closed-loop transfer function is given by (5). In other words, the system behaves as a first-order low-pass filter whose cutoff angular frequency is $\omega_{C0} = A \cdot B$

$$H(s) = \frac{A \cdot \frac{1}{s}}{1 + A \cdot \frac{1}{s} \cdot B} = \frac{1}{B} \frac{1}{1 + s\frac{1}{A \cdot B}}. \tag{5}$$

B. Actual Implementation

The actual implementation of the realized proof-of-concept prototype is shown in Fig. 5, where discrete components are used for the different functional blocks of the proposed feedback system.

The sensor, represented by capacitors C_1 and C_2, constitutes the left leg of a bridge excited by the sinusoidal AC source $V_{\rm sin}$. Thus, at the rest position ($x = 0$), the sensor output is $V_S(t) = V_{\rm sin}(t)/2 = V_{\rm ref}(t)$ and the measurand range $x \in [-1, 1]$ results in $|V_S| \in [0, |V_{\rm sin}|]$, as in (4). The VCR in the right leg is controlled in order to generate the $V_{\rm fb}$ signal, following the V_S. The dashed box of Fig. 5 shows the VCR actual implementation, based on fixed resistor R_b and an analog multiplier AD633 (from Analog Devices).

The feedback signal summing node is implemented by an instrumentation amplifier, INA, providing buffering as well (INA128 from Texas Instruments), being configured for a unitary gain. The (synchronous) demodulation of the error signal V_e is performed by using another AD633 in the multiplier configuration, which outputs the signal $W = (1/10[\rm V]) \cdot X \cdot Y + Z$, where X and Y are two differential inputs, i.e., $X = (X_1 - X_2)$ and $Y = (Y_1 - Y_2)$. The multiplier output $V_{\rm mul}$ is shown in the following equation:

$$V_{\rm mul}(t) = \frac{1}{10\ [\rm V]} \cdot \frac{|V_{\rm sin}| \cdot |V_e|}{2}[1 - \cos(2 \cdot \omega_{\rm sin} t)]. \tag{6}$$

Signal $V_{\rm mul}$ feeds an inverting integrator based on the LF411 operational amplifier (from Texas Instruments) followed by a resistive voltage divider attenuating the $V_{\rm mul}$ signal by $D = R_{vd2}/(R_{vd1} + R_{vd2})$, thus generating the control signal $V_{\rm ctrl}$ shown in (7). Since the attenuating factor D is still in the forward path of the feedback scheme, it only affects the integrator output range and does not modify the overall input–output relationship. The final approximation holds when the residual ripple, due to the nonideal behavior of the integrator in removing unwanted high-frequency components of the demodulation process, is negligible. However, it can be removed by further postprocessing

$$\begin{aligned} V_{\rm ctrl}(t) &= -\frac{D}{RC}\int_t V_{\rm mul}(t)dt \\ &= -\frac{|V_{\rm sin}|}{20\ [\rm V]}\frac{D}{RC}\int_t |V_e|[1 - \cos(2 \cdot \omega_{\rm sin} t)]dt \\ &\approx -\frac{|V_{\rm sin}|}{20\ [\rm V]}\frac{D}{RC}\int_t |V_e|dt. \end{aligned} \tag{7}$$

It is interesting to note that the low-pass behavior of the integrator minimizes the $V_{\rm mul}$ term at $2 \cdot \omega_{\rm sin}$ and the demodulation process is achieved without any additional (low-pass) filter. The phase offset of the inverting integrator is

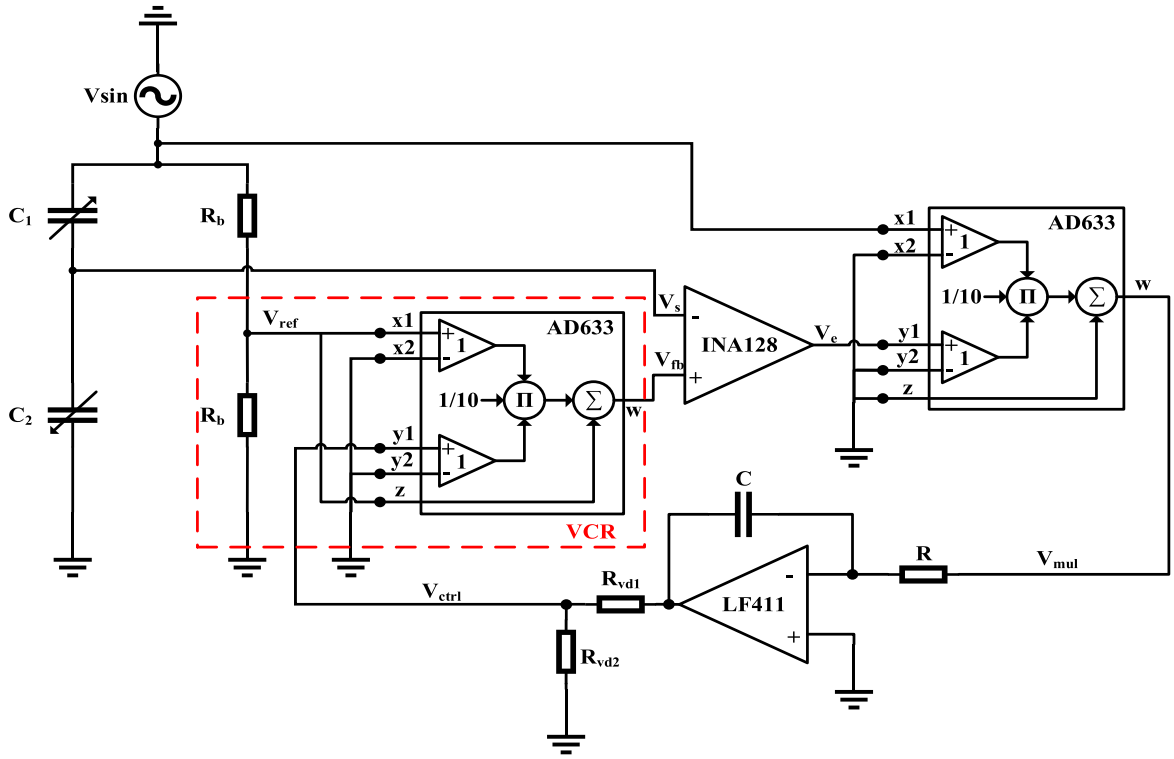

Fig. 5. Simplified schematic of the proposed interface.

compensated by swapping the inputs of the summing node implemented by the INA128, thus preserving the negative feedback.

Finally, the feedback signal V_{fb} is obtained modulating V_{ctrl} by means of another AD633, as in (8), where the resulting R_{VCR} value is shown as well

$$V_{\text{fb}} = V_{\text{ref}}\left(\frac{1}{10\ [\text{V}]}V_{\text{ctrl}} + 1\right)$$
$$R_{\text{VCR}} = R_b\frac{10\ [\text{V}] + V_{\text{ctrl}}}{10\ [\text{V}] - V_{\text{ctrl}}}. \tag{8}$$

As previously stated, when the system is balanced V_S equals V_{fb}; thus, combining (4) and (8), the relationship between V_{ctrl} and x is described by the very simple relation in the following equation:

$$V_{\text{ctrl}} = 10\ [\text{V}]\cdot x, \quad \text{i.e.,}\ \ x = \frac{1}{10\ [\text{V}]}V_{\text{ctrl}}. \tag{9}$$

Sensitivity $S_{\text{Vctrl},x}$ with respect to x is constant and in particular $S_{\text{Vctrl},x} = 10$ V and could be modified acting on the gain of the feedback path.

It has to be highlighted that the additive term V_{ref} in (8) is necessary to compensate for the equivalent term in (4); both can be ignored for evaluating the balanced closed-loop gain. Indeed, recalling Section III-A results, the implemented circuit can be schematized as in Fig. 6, where G_{ina} is the amplification factor of the INA128, set to 1, $A_{\text{dem}} = 1/20[\text{V}]$ (1/10[V] from the AD633 and 1/2 from the demodulation operation, as in (6)), A_{int} is the amplification factor of the integrator, set to $1/RC$, and $A_{\text{mod}} = 1/10[\text{V}]$ (from the AD633).

The forward and feedback gains A and B can be computed as in (10). Consequently, the (balanced) closed-loop gain is $G_{\text{CL}} = V_{\text{ctrl}}/|V_S| = 1/B$ and the cutoff angular frequency ω_{CO} can be roughly estimated as $A \cdot B$, as shown in the following equation:

$$A = \frac{|V_{\text{sin}}|}{20\ [\text{V}]}\frac{D}{RC}, \quad B = \frac{|V_{\text{ref}}|}{10\ [\text{V}]} = \frac{|V_{\text{sin}}|}{20\ [\text{V}]}$$
$$\omega_{\text{CO}} = \frac{|V_{\text{sin}}|^2}{400\ [\text{V}^2]}\frac{D}{RC}. \tag{10}$$

C. Parasitic Effects

As commonly known from [12], an equivalent model for differential capacitive sensors, which includes parasitic capacitances C_p, can be obtained by supposing these stray components all together connected between the sensor common node and ground, as shown in Fig. 7.

By taking into account C_p in the bridge configuration (see Fig. 2) in parallel with C_2, (9) becomes as in (11) if the sensor configuration of Fig. 1(a) is considered, otherwise, as in (12) if the setup of Fig. 1(b) is taken into account. The C_0 parameter is the sensor baseline value and derives from (1) and (2). It should be noted that the ideal situation, i.e., no parasitic capacitance C_p, corresponds to $\alpha = 0$

$$V_{\text{ctrl}} = 10\ [\text{V}]\cdot\frac{2}{2+\alpha\cdot(1-x^2)}\cdot x - \frac{10\ [\text{V}]\cdot\alpha\cdot(1-x^2)}{2+\alpha\cdot(1-x^2)}$$

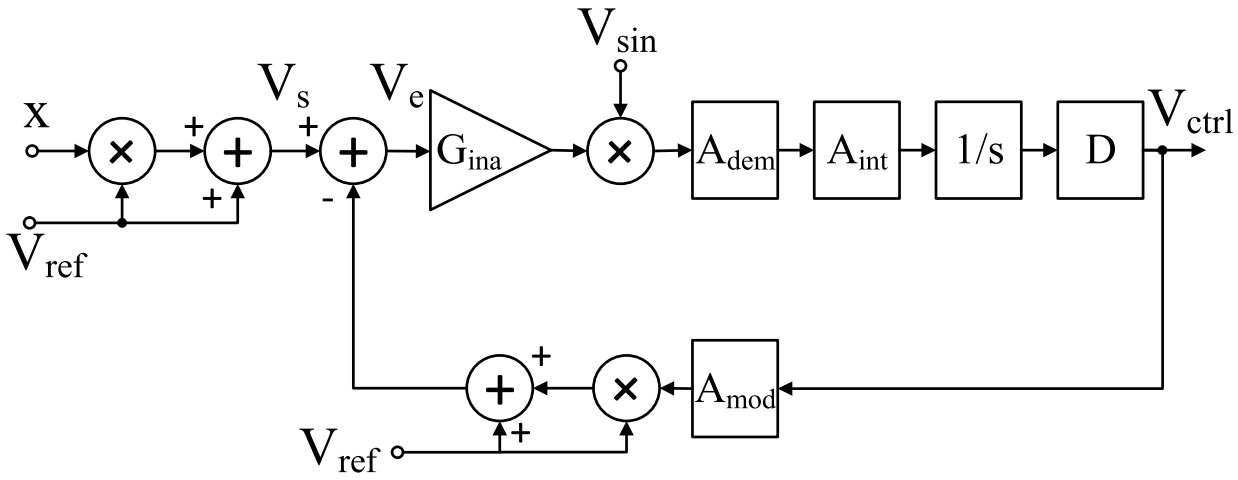

Fig. 6. Equivalent block diagram of the proposed interface.

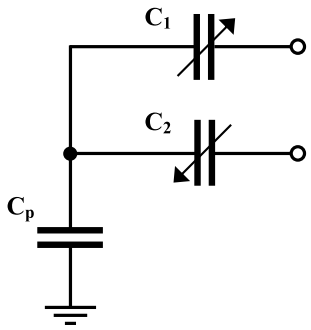

Fig. 7. Differential capacitance sensor with parasitic equivalent model.

with

$$\alpha = \frac{C_p}{C_o} \tag{11}$$

$$V_{\text{ctrl}} = 10\ [\text{V}] \cdot \frac{2}{2+\alpha} \cdot x - \frac{10\ [\text{V}] \cdot \alpha}{2+\alpha} \quad \text{with } \alpha = \frac{C_p}{C_o}. \tag{12}$$

In the latter case, parasitics have the overall effect of lowering the output signal V_{ctrl} with respect to the ideal one, hence, decreasing the interface sensitivity, still maintaining a linear behavior. Contrariwise, in the former situation, linearity is heavily affected, especially in the central part of the range. Such effects are much evident as α increases, i.e., when the sensor baseline value C_0 tends to be comparable with parasitic capacitance C_p. An overview of the parasitic effects can be visualized in Fig. 8, where the ideal behavior of V_{ctrl}, i.e., without parasitic effects, is compared with the estimated behavior by means of (11) and (12) with two different values of α. It is worth noting that when C_0 is ten times larger than C_p ($\alpha = 0.1$), parasitic effects already visibly deviate the real behavior with respect to the ideal one. An estimation of such deviations is about 2.3% FS for the configuration of Fig. 1(a) and about 4.8% FS for the configuration of Fig. 1(b).

A possible way to compensate for these unwanted effects is to balance the current drawn by C_p by injecting an equal current to the central sensor node; in such a way, it is possible to confirm that the same current flows through the two sensor

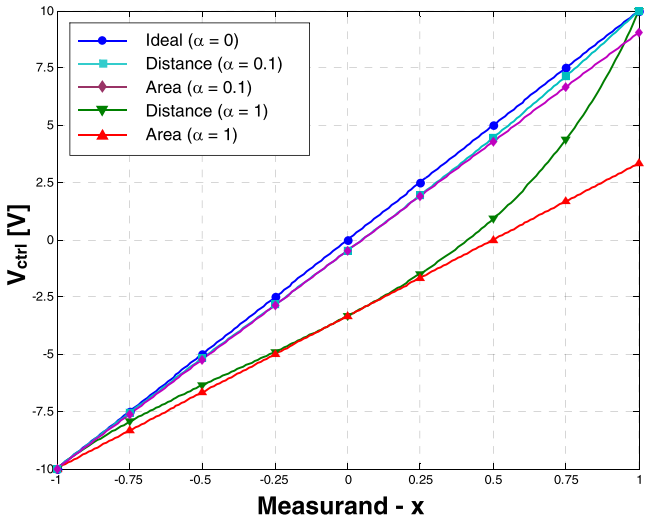

Fig. 8. Comparison among ideal behavior without parasitic effects and estimated behavior with two different values of α. "Distance" stands for the configuration in Fig. 1(a), whereas "Area" refers to the setup in Fig. 1(b).

capacitors C_1 and C_2 (actual series connection) [12]. This can be done, for example, by properly designing a negative impedance converter (NIC), in order to obtain an equivalent negative capacitor to be placed in parallel to both C_2 and C_p. Furthermore, it is possible to take advantage of a feedback circuitry to automatically and dynamically compensate for the aforementioned source of errors.

IV. Simulation Results

Some preliminary simulations have been performed in the MATLAB/Simulink environment in order to evaluate the system dynamic behavior, having considered the first-order model previously described (as in Fig. 6) in the equivalent phasor representation. In Fig. 9, the model is depicted, whereas in Fig. 10, simulation outputs are shown when the measurand varies from the rest position $x = 0$ to $x = 90\%$, and then down to $x = -90\%$. Two different circuit configurations are considered, that is, 1) V_{ctrl1} at $D = 2/3$, $C = 2$ nF, and

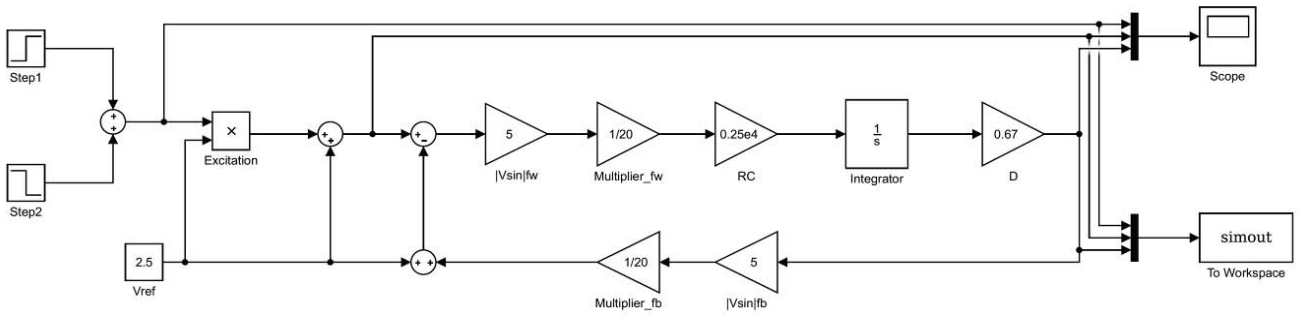

Fig. 9. Simulink model of the proposed system.

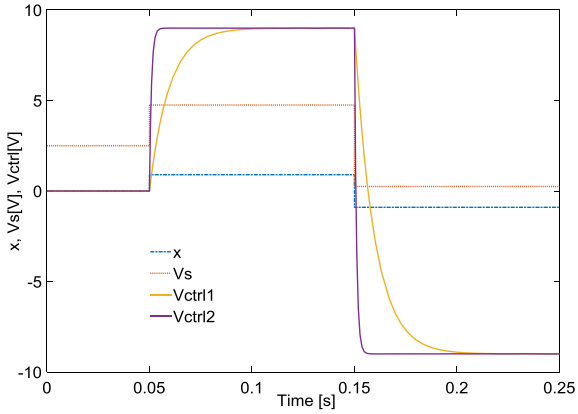

Fig. 10. Simulink simulation results for different cutoff frequencies (V_{ctrl1} at $\omega_{\text{CO1}} \approx 104$ rad/s and V_{ctrl2} at $\omega_{\text{CO2}} \approx 1040$ rad/s). The amplitude of the sinusoidal sensor output V_S is reported as a reference for comparison versus x.

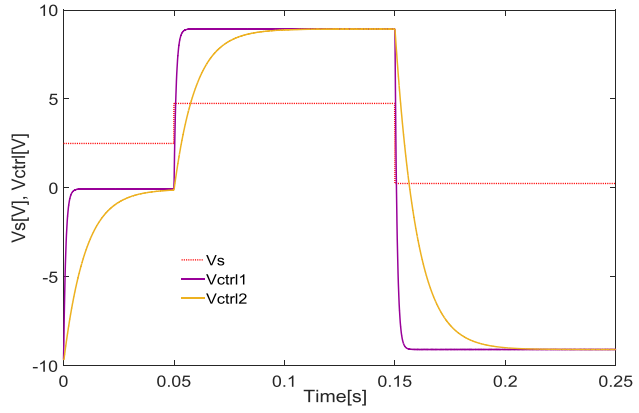

Fig. 11. PSpice simulation results for different cutoff frequencies (V_{ctrl1} at $R = 20$ kΩ and C =2 nF and V_{ctrl2} at $R = 200$ kΩ and $C = 2$ nF). The amplitude of the sinusoidal sensor output V_S is reported as a reference for comparison versus x.

$R = 200$ kΩ and 2) V_{ctrl2} at $D = 2/3$, $C = 2$ nF, and $R = 20$ kΩ. In the former case, the cutoff angular frequency is $\omega_{\text{CO1}} \approx 104$ rad/s, whereas in the latter, $\omega_{\text{CO2}} \approx 1040$ rad/s.

The same circuit configurations have been used for PSpice simulations as well. Simulation outputs (shown in Fig. 11) perfectly match results provided by the simplified Simulink model, thus confirming that, when the sinusoidal excitation angular frequency is $\omega_{\text{sin}} = 2\pi \times 10^3$ rad/s, nonidealities of components can be neglected and overall system actually behaves as a low-pass filter. It has to be highlighted that simulations start with different initial conditions, justifying the different behaviors between Figs. 10 and 11 in the first 50 ms of simulation.

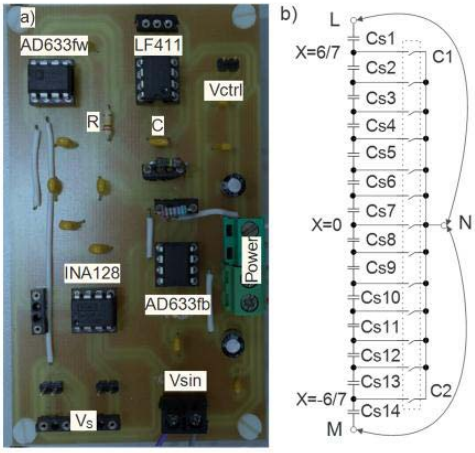

Fig. 12. (a) PCB of the realized prototype. (b) Differential capacitive sensor emulator; L, M, and N refer to the scheme in Fig. 1(a).

V. Experimental Results

As previously stated, a real-world proof-of-concept prototype has been realized using discrete components. The board is shown in Fig. 12(a). It has to be highlighted that the proposed architecture can easily be integrated in a single-chip solution since only well-proved and well-known function blocks are adopted. Thus, the use of a discrete-component solution allows estimating performance obtainable with an integrated implementation.

In order to finely control equivalent measurand variations, the transducer behavior has been emulated by a set of C_{Si}, $i = 1, \ldots, 14$, i.e., 14 capacitors connected in series, as shown in Fig. 12(b). Such a configuration interface mimics the sensor behavior depicted in Fig. 1(a) (i.e., when the measurand influences the distance between plates). All the C_{Si} have the same nominal value $C_S \in [1, 2.2, 4.7, 10, 100]$ nF, so that

variations in the value of the measurand have a resolution of 1/7 in the useful range $x \in [-6/7, 6/7]$. A set of programmable switches (based on solid-state relay) used for selecting the desired output is shown in Fig. 12(b). In order to consider possible delays introduced by these switches, a dummy channel connected via a dummy switch is acquired as well, as a temporal reference signal. A digital multimeter (DMM, Agilent 34411A) has been employed for measuring the actual emulated sensor output; in that way, for each position of the cursor N, a more accurate indication of the actual measurand x is obtained.

A. Discussion on Uncertainties

The interface output $\langle x \rangle$ with respect to the reference x value is $\langle x \rangle = \gamma \cdot x$, with the ratio $\gamma = (V_{\text{ctrl}}/10[\text{V}]) \cdot (1/x)$ experimentally evaluated. The overall uncertainty $U(\langle x \rangle)$ has been estimated considering the uncertainty contribution from γ calculated as Type A (i.e., exploiting the standard deviation of the N_{OBS} realizations) and contribution from x calculated as Type B (i.e., exploiting the knowledge about uncertainty of the Agilent 34411A DMM). Statistical evaluation of γ leads to an uncertainty on the order of $U(\gamma) = 2.5 \times 10^{-3}$, when $N_{\text{OBS}} = 20$ observations are considered. On the other side, considering the relationship (3), the uncertainty on x can be evaluated as in the following equations:

$$U(x, C_1) = \frac{2C_2}{(C_1 + C_2)^2} U(C_1) \tag{13}$$

$$U(x, C_2) = -\frac{2C_1}{(C_1 + C_2)^2} U(C_2). \tag{14}$$

Consequently, the overall contribution is given by (15), where $k(= 2)$ is the covering factor

$$U(\langle x \rangle) = k\sqrt{U^2(\gamma) + U^2(x, C_1) + U^2(x, C_2)}. \tag{15}$$

The worst case is for $C_1 = C_2 = C_S/7 = 1$ nF/7 and leads to an overall uncertainty $U(\langle x \rangle) \approx 0.2$. It has to be noted that if averaging over N_{OBS} observations is tolerated, the uncertainty mainly depends on the DMM.

B. Resolution and Linearity Evaluation

Experimental tests of the circuit have been carried out using an automated test equipment exploiting National Instruments tools and a software purposely developed under the LabVIEW environment. The experimental setup is shown in Fig. 13. A National Instruments VirtualBench function generator has been employed for providing the excitation signal V_{sin}. Particularly, in agreement with the setup used in the simulations, the excitation signal has $|V_{\text{sin}}| = 10$ V peak-to-peak amplitude and $\omega_{\text{sin}} = 2\pi \times 10^3$ rad/s angular frequency (implicitly having null phase). The VirtualBench also drives the bank of switches, using a digital output port. Conversely, the interface output V_{ctrl} reading has been performed by a National Instruments NI6110 DAQ board. The choice is dictated by the simultaneous sampling capability, adopted for acquiring the analog signal of interest and digital driving signal of the reference dummy switch.

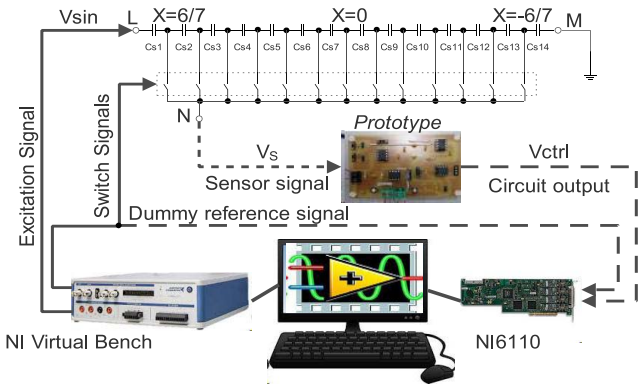

Fig. 13. Experimental setup.

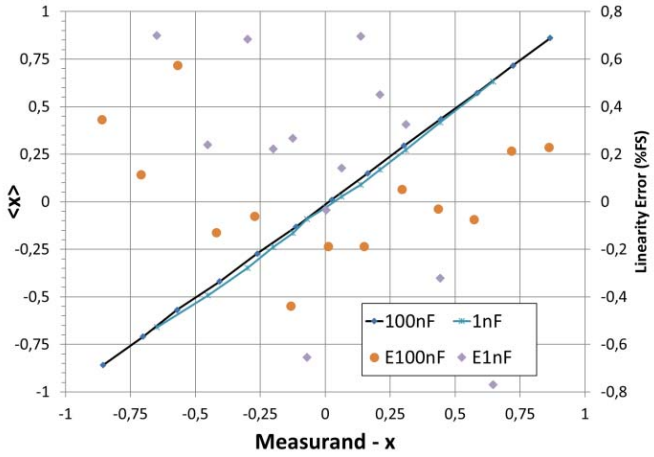

Fig. 14. Calibration curve and the linearity error for extreme values of the $C_S \in [1, 100]$ nF. Linearity errors for other C_S values are in between.

First, static performance is evaluated, considering different measurand x values and acquiring the circuit output V_{ctrl} once it has reached a steady value. For each measurand $x \in [-6/7, 6/7]$, $N_{\text{OBS}} = 20$ acquisitions of the V_{ctrl} output signal have been collected. In particular, each V_{ctrl} value is the average of $N_S = 125$ kSa acquired using a sampling frequency $f_S = 25$ kSa/s. From the average of the N_{OBS} available observations, each one lasting $T_{\text{OBS}} = 5$ s, an estimated value $\langle x \rangle$ of the measurand x has been obtained by means of (9), resulting in the calibration curve in Fig. 14; for this static characterization, we have chosen $C = 2$ nF and $R = 200$ kΩ. The maximum linearity error results in $e_{\text{LIN\_}\pm100\%,\text{MAX}} = [0.8, 0.7, 0.5, 0.6, 0.6]\%$ FS for $C_S \in [1, 2.2, 4.7, 10, 100]$ nF, respectively. If the useful range is limited to $x \in [-3/7, 3/7]$, the maximum linearity error decreases down to $e_{\text{LIN\_}\pm50\%,\text{MAX}} = [0.4, 0.4, 0.3, 0.1, 0.1]\%$ FS for $C_S \in [1, 2.2, 4.7, 10, 100]$ nF, respectively. As expected, when smaller values of C_S are considered and parasitics have larger effects, nonlinearity emerges. As previously highlighted, such a result is mainly imputable to parasitics in the discrete-component circuit implementation. Integrating the circuit in a single integrated circuit can greatly improve the performance.

In order to evaluate the resolution, N_{OBS} available observations for each reference measurand value x have been

TABLE I
EXPERIMENTAL EVALUATION OF CUTOFF ANGULAR FREQUENCY (rad/s) ($C = 2$ nF AND $R = 200$ kΩ)

x variations	-6/7 → 6/7	6/7 → -6/7	-1/7 → 1/7	1/7 → -1/7
C_0=100nF/7	78.13	78.13	81.30	81.97
C_0=10nF/7	78.13	78.74	80.65	81.30
C_0=4.7nF/7	79.37	78.74	79.37	81.97

TABLE II
EXPERIMENTAL EVALUATION OF CUTOFF ANGULAR FREQUENCY (rad/s) ($C = 2$ nF AND $R = 20$ kΩ)

x variations	-6/7 → 6/7	6/7 → -6/7	-1/7 → 1/7	1/7 → -1/7
C_0=100nF/7	657.89	781.25	751.88	810.11
C_0=10nF/7	709.22	787.40	746.27	803.82
C_0=4.7nF/7	645.16	781.25	729.93	805.79

TABLE III
COMPARISON TABLE

Reference	[10]	[15]	[17]	[27]	This work
C_0[F]	20 p	500 p	400 p	400 p	140p÷14n
Variation range [%]	±60	±50	±50	-30 +100	±100
Approach	C to V	C to V	C to Digital	C to V	C to V
Error [%]	<0.1	<0.03	<0.2	<0.45	0.5÷0.8

reckoned. As stated in Section V-A, the worst case standard deviation is 0.05 and can be considered an indication of the actual resolution.

C. Dynamic Response Characterization

In addition, dynamic performance has been evaluated. In this scenario, the same setups used for the simulations are replicated for the real-world prototype. For the sake of simplicity, only a subset of all the possible C_S and measurand x variations has been considered. Subsequently, supposing a first-order low-pass response, a fitting with an exponential function allows estimating the actual cutoff angular frequency, as resumed in Tables I and II. Frequencies similar to the simulated values are obtained. Differences are mainly imputable to tolerances on the nominal value of passive components. In addition, it has to be remembered that, at the integrator output, a residual ripple is observed. Main components are at $2 \cdot \omega_{\sin}$, due to the forward multiplier, and at $\omega_{\sin}$, due to any offset induced by devices and fed to the multiplier in the forward path. Clearly, the smaller the RC value, the less effecting the filtering action of the integrator. As a concluding remark, if faster circuit response is needed, a comparatively higher excitation frequency $\omega_{\sin}$ has to be adopted.

Finally, a comparison with other research work has been carried out, as shown in Table III. As stated in this paper, the proposed circuit suffers from parasitics, but the error is always smaller than 1% FS. Moreover, it has to be highlighted that such an error is evaluated across the full-range capacitive variation, differently from other works. The interface integration into a single-chip solution can mitigate parasitic effects. Additionally, an active compensation technique can be applied as well.

VI. CONCLUSION

A novel analog interface performing differential capacitance sensing has been designed. This work overcomes the main issue of a previous different solution, i.e., a nonlinear relation between the output response and the measurand, providing a direct simple relationship between capacitive variation and output voltage. Theoretical and simulated considerations have evaluated the goodness of the proposed approach. A discrete elements board solution has been tested, showing satisfactory results that confirm the circuit capability to follow the capacitive sensor variations in a full estimation range, having considered five different capacitive sensor baselines. An integrated implementation of the proposed interface is planned as future work.

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