Faculty of Science and Technology
Savitribai Phule Pune University
Maharashtra, India

http://unipune.ac.in

Curriculum
for
Second Year of Computer Engineering
(2019 Course)
(With effect from 2020-21)

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Savitribai Phule Pune University

Second Year of Computer Engineering (2019 Course)

(With effect from Academic Year 2020-21)

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Bachelor of Computer Engineering

Program Outcomes (POs)

Learners are expected to know and be able to–

PO1	**Engineering knowledge**	Apply the knowledge of mathematics, science, Engineering fundamentals, and an Engineering specialization to the solution of complex Engineering problems.
PO2	**Problem analysis**	Identify, formulate, review research literature and analyze complex Engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and Engineering sciences.
PO3	**Design / Development of Solutions**	Design solutions for complex Engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and Environmental considerations.
PO4	**Conduct Investigations of Complex Problems**	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern Tool Usage**	Create, select, and apply appropriate techniques, resources, and modern Engineering and IT tools including prediction and modeling to complex Engineering activities with an understanding of the limitations.
PO6	**The Engineer and Society**	Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practices.
PO7	**Environment and Sustainability**	Understand the impact of the professional Engineering solutions in societal and Environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics**	Apply ethical principles and commit to professional ethics and responsibilities and norms of Engineering practice.
PO9	**Individual and Team Work**	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication Skills**	Communicate effectively on complex Engineering activities with the Engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project Management and Finance**	Demonstrate knowledge and understanding of Engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary Environments.
PO12	**Life-long Learning**	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSO)

A graduate of the Computer Engineering Program will demonstrate-

PSO1	**Professional Skills**-The ability to understand, analyze and develop computer programs in the areas related to algorithms, system software, multimedia, web design, big data analytics, and networking for efficient design of computer-based systems of varying complexities.
PSO2	**Problem-Solving Skills**- The ability to apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success.
PSO3	**Successful Career and Entrepreneurship**- The ability to employ modern computer languages, environments and platforms in creating innovative career paths to be an entrepreneur and to have a zest for higher studies.

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Savitribai Phule Pune University

Second Year of Computer Engineering (2019 Course)

(With effect from Academic Year 2020-21)

Semester-III

Course Code	Course Name	Teaching Scheme (Hours/Week)			Examination Scheme and Marks						Credit Scheme			
		Lecture	Practical	Tutorial	Mid-Sem	End-Sem	Term work	Practical	Oral	Total	Lecture	Practical	Tutorial	Total
210241	Discrete Mathematics	03	-	-	30	70	-	-	-	100	03	--	-	03
210242	Fundamentals of Data Structures	03	-	-	30	70	-	-	-	100	03	-	-	03
210243	Object Oriented Programming (OOP)	03	-	-	30	70	-	-	-	100	03	-	-	03
210244	Computer Graphics	03	-	-	30	70	-	-	-	100	03	-	-	03
210245	Digital Electronics and Logic Design	03	-	-	30	70	-	-	-	100	03	-	-	03
210246	Data Structures Laboratory	-	04	-	-	-	25	50	-	75	-	02	-	02
210247	OOP and Computer Graphics Laboratory	-	04	-	-	-	25	25	-	50	-	02	-	02
210248	Digital Electronics Laboratory	-	02	-	-	-	25	-	-	25	-	01	-	01
210249	Business Communication Skills	-	02	-	-	-	25	-	-	25	-	01	-	01
210250	Humanity and Social Science	-	-	01	-	-	25	-	-	25	-	-	01	01
210251	Audit Course 3													
										Total Credit	15	06	01	22
	Total	**15**	**12**	**01**	**150**	**350**	**125**	**75**	**-**	**700**	-	-	-	-

Semester-IV

Course Code	Course Name	Teaching Scheme (Hours/Week)			Examination Scheme and Marks						Credit Scheme			
		Lecture	Practical	Tutorial	Mid-Sem	End-Sem	Term work	Practical	Oral	Total	Lecture	Practical	Tutorial	Total
207003	Engineering Mathematics III	03	-	01	30	70	25	-	-	125	03	--	01	04
210252	Data Structures and Algorithms	03	-	-	30	70	-	-	-	100	03	-	-	03
210253	Software Engineering	03	-	-	30	70	-	-	-	100	03	-	-	03
210254	Microprocessor	03	-	-	30	70	-	-	-	100	03	-	-	03
210255	Principles of Programming Languages	03	-	-	30	70	-	-	-	100	03	-	-	03
210256	Data Structures and Algorithms Laboratory	-	04	-	-	-	25	25	-	50	-	02	-	02
210257	Microprocessor Laboratory	-	02	-	-	-	25	-	25	50	-	01	-	01
210258	Project Based Learning II	-	04	-	-	-	50	-	-	50	-	02	-	02
210259	Code of Conduct	-	-	01	-	-	25	-	-	25	-	-	01	01
210260	Audit Course 4													
										Total Credit	15	05	02	22
	Total	**15**	**10**	**02**	**150**	**350**	**150**	**25**	**25**	**700**	-	-	-	-

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General Guidelines

1. Every undergraduate program has its own objectives and educational outcomes. These objectives and outcomes are furnished by considering various aspects and impacts of the curriculum. These **Program Outcomes (POs)** are categorically mentioned at the beginning of the curriculum (ref: NBA Manual). There should always be a rationale and a goal behind the inclusion of a course in the curriculum. Course Outcomes though highly rely on the contents of the course; many-a-times are generic and bundled. The **Course Objectives**, **Course Outcomes** and **CO-PO mappings matrix** justifies the motives, accomplishment and prospect behind learning the course. The Course Objectives, Course Outcomes and CO-PO Mapping Matrix are provided for reference and these are indicative only. The course instructor may modify them as per his or her perspective.

2. @:**CO and PO Mapping Matrix** (Course Outcomes and Program Outcomes)- The **expected** attainment mapping matrix at end of course contents, indicates the correlation levels of 3, 2, 1 and '-'. The notation of 3, 2 and 1 denotes substantially (high), moderately (medium) and slightly (low). The mark '-' indicates that there is no correlation between the respective CO and PO.

3. **#:Elaborated examples/Case Studies-** For each course, contents are divided into six units-I, II, III, IV, V and VI. Elaborated examples/Case Studies are included at the end of each unit to explore how the learned topics apply to real world situations and need to be explored so as to assist students to increase their competencies, inculcating the specific skills, building the knowledge to be applicable in any given situation along with an articulation. One or two sample exemplars or case studies are included for each unit; instructor may extend the same with more. **Exemplar/Case Studies** may be assigned as self-study by students and to be excluded from theory examinations.

4. *:For each unit contents, the desired content attainment mapping is indicated with Course Outcome(s). Instructor may revise the same as per their viewpoint.

5. For laboratory courses, set of suggested assignments is provided for reference. Laboratory Instructors may design suitable set of assignments for respective course at their level. Beyond curriculum assignments and mini-project may be included as a part of laboratory work. The Inclusion of few optional assignments that are intricate and/or beyond the scope of curriculum will surely be the value addition for the students and it will satisfy the intellectuals within the group of the learners and will add to the perspective of the learners.

6. For each laboratory assignment, it is essential for students to draw/write/generate flowchart, algorithm, test cases, mathematical model, Test data set and comparative/complexity analysis (as applicable). Batch size for practical and tutorial may be as per guidelines of authority.

7. For each course, irrespective of the examination head, the instructor should motivate students to read and publish articles, research papers related to recent development and invention in the field.

8. For laboratory, instructions have been included about the conduction and assessment of laboratory work. These guidelines are to be strictly followed. Use of open source software is appreciated.

9. **Term Work**[1]**–**Term work is continuous assessment that evaluates a student's progress throughout the semester[1]. Term work assessment criteria specify the standards that must be met and the evidence that will be gathered to demonstrate the achievement of course outcomes. Categorical assessment criteria for the term work should establish unambiguous

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standards of achievement for each course outcome. They should describe what the learner is expected to perform in the laboratories or on the fields to show that the course outcomes have been achieved. It is recommended to conduct internal monthly practical examination as part of continuous assessment.

Students' work will be evaluated typically based on the criteria like attentiveness, proficiency in execution of the task, regularity, punctuality, use of referencing, accuracy of language, use of supporting evidence in drawing conclusions, quality of critical thinking and similar performance measuring criteria.

10. **Laboratory Journal-** Program codes with sample output of all performed assignments are to be submitted as softcopy. Use of DVD or similar media containing students programs maintained by Laboratory In-charge is highly encouraged. For reference one or two journals may be maintained with program prints in the Laboratory. As a conscious effort and little contribution towards Green IT and environment awareness, attaching printed papers as part of write-ups and program listing to journal may be avoided. Submission of journal/ term work in the form of softcopy is desirable and appreciated.

11. **Tutorial**[1] - Tutorials can never be an individual course but an additional aid to the learners. Tutorials help the learners to inculcate the contents of the course with focused efforts on small group of the learners. Tutorial conduction should concentrate more on simplifying the intricacies converging to clear understanding and application. **Assessment of tutorial work is to be done in a manner similar to assessment of term-work; do follow same guidelines.**

12. **Audit Course**[1]: The student registered for audit course shall be awarded the grade AP/PP (Audit Course Pass) and the grade 'AP'/'PP' shall be included in the Semester grade report for that course, provided student has the minimum attendance as prescribed by the Savitribai Phule Pune University and satisfactory performance and secured a passing grade in that audit course. No grade points are associated with this 'AP'/'PP'' grade and performance in these courses is not accounted in the calculation of the performance indices SGPA and CGPA. Evaluation of audit course will be done at institute level itself.

13. **$**:For courses 210249: Business Communication Skills, 210250: Humanity and Social Science and 210260: Code of Conduct, one credit can be earned by student if student successfully completes the Swayam course as listed in curriculum of respective course in this document.

UGC has issued the UGC (Credit Framework for online learning courses through SWAYAM) Regulation 2016 advising the Universities to identify courses where credits can be transferred on to the academic record of the students for courses done on SWAYAM. AICTE has also put out gazette notification in 2016 and subsequently for adoption of these courses for credit transfer [2].

SWAYAM is a programme initiated by Government of India and designed to achieve the three cardinal principles of Education Policy viz., access, equity and quality. This is done through a platform that facilitates hosting of the courses to be accessed by anyone, anywhere at any time. Courses delivered through SWAYAM are interactive, prepared by the best teachers in the country and are available, free of cost to any learner. However, learners wanting a SWAYAM certificate should register for the final proctored exams that come at a fee and attend in-person at designated center on specified dates. Eligibility for the certificate is generally announced on the course page. Universities/colleges approving credit transfer for these courses can use the marks/certificate obtained in these courses for the same.[2]

Note: For Examination rules, pattern and assessment please refer [1]

[1]http://collegecirculars.unipune.ac.in/sites/documents/Syllabus%202019/Rules%20and%20Regulations%20F.E.%202019%20Patt_10.012020.pdf

[2] https://swayam.gov.in/about

Abbreviations		
TW: Term Work	**TH: Theory**	**PR: Practical**
OR: Oral	**TUT: Tutorial**	**Sem: Semester**

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Savitribai Phule Pune University
Second Year of Computer Engineering (2019 Course)
210245: Digital Electronics and Logic Design

Teaching Scheme	Credit Scheme	Examination Scheme and Marks
Lecture: 03 Hours/Week	03	Mid_Semester(TH): 30 Marks End_Semester(TH): 70 Marks

Prerequisite Courses : 104010: Basic Electronics Engineering

Companion Course : 210249: Digital Electronics Lab

Course Objectives:

The goal of this course is to impart the fundamentals of digital logic design; starting from learning the basic concepts of the different base number systems, to basic logic elements and deriving logical expressions to further optimize a circuit diagram. Objective is to see that learners are not only able to evaluate different combinational logic designs, but also design their own digital circuits given different parameters.

- To study number systems and develop skills for design and implementation of combinational logic circuits and sequential circuits
- To understand the functionalities, properties and applicability of Logic Families.
- To introduce programmable logic devices and ASM chart and synchronous state machines.
- To introduce students to basics of microprocessor.

Course Outcomes:

On completion of the course, learner will be able to–

CO1: Simplify Boolean Expressions using K Map.
CO2: Design and implement combinational circuits.
CO3: Design and implement sequential circuits.
CO4: Develop simple real-world application using ASM and PLD.
CO5: Differentiate and Choose appropriate logic families IC packages as per the given design specifications.
CO6: Explain organization and architecture of computer system

Course Contents

Unit I	Minimization Technique	(07 Hours)

Logic Design Minimization Technique: Minimization of Boolean function using K-map(up to 4 variables) and Quine Mc-Clusky Method, Representation of signed number- sign magnitude representation ,1's complement and 2's complement form (red marked can be removed), Sum of product and Product of sum form, Minimization of SOP and POS using K-map.

#Exemplar/Case Studies	Digital locks using logic gates
*Mapping of Course Outcomes for Unit I	CO1

Unit II	Combinational Logic Design	(07 Hours)

Code converter -: BCD, Excess-3, Gray code, Binary Code. Half- Adder, Full Adder, Half Subtractor, Full Subtractor, Binary Adder (IC 7483), BCD adder, Look ahead carry generator, Multiplexers (MUX): MUX (IC 74153, 74151), Cascading multiplexers, Demultiplexers (DEMUX)- Decoder (IC 74138, IC 74154), Implementation of SOP and POS using MUX, DMUX, Comparators (2 bit), Parity generators and Checker.

#Exemplar/Case Studies	Combinational Logic Design of BCD to 7-segment display Controller
*Mapping of Course Outcomes for Unit II	CO2

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Unit III	Sequential Logic Design	(07 Hours)
Flip-Flop: SR, JK,D,T, Preset and Clear, Master Slave JK Flip Flops, Truth Tables and Excitation tables, Conversion from one type to another type of Flop-Flop. Registers: SISO, SIPO, PISO, PIPO, Shift Registers, Bidirectional Shift Register, Ring Counter , Universal Shift Register Counters: Asynchronous Counter, Synchronous Counter, BCD Counter, Johnson Counter, Modulus of the counter (IC 7490),Synchronous Sequential Circuit Design :Models- Moore and Mealy, State diagram and State Table ,Design Procedure, Sequence Generator and detector.		
#Exemplar/Case Studies	Electronic Voting Machine (EVM)	
*Mapping of Course Outcomes for Unit III	CO3	
Unit IV	**Algorithmic State Machines and Programmable Logic Devices**	**(07 Hours)**
Algorithmic State Machines: Finite State Machines (FSM) and ASM, ASM charts, notations, construction of ASM chart and realization for sequential circuits. PLDS:PLD, ROM as PLD, Programmable Logic Array (PLA), Programmable Array Logic (PAL), Designing combinational circuits using PLDs.		
#Exemplar/Case Studies	Wave form generator using MUX controller method	
*Mapping of Course Outcomes for Unit IV	CO4	
Unit V	**Logic Families**	**(07 Hours)**
Classification of logic families: Unipolar and Bipolar Logic Families, Characteristics of Digital ICs: Fan-in, Fan-out, Current and voltage parameters, Noise immunity, Propagation Delay, Power Dissipation, Figure of Merits, Operating Temperature Range, power supply requirements. **Transistor**-Transistor Logic: Operation of TTL NAND Gate (Two input), TTL with active pull up, TTL with open collector output, Wired AND Connection, Tristate TTL Devices, TTL characteristics. CMOS: CMOS Inverter, CMOS characteristics, CMOS configurations- Wired Logic, Open drain outputs.		
#Exemplar/Case Studies	To study the various basic gate design using TTL/CMOS logic family	
*Mapping of Course Outcomes for Unit V	CO5	
Unit VI	**Introduction to Computer Architecture**	**(07 Hours)**
Introduction to Ideal Microprocessor – Data Bus, Address Bus, Control Bus. Microprocessor based Systems – Basic Operation, Microprocessor operation, Block Diagram of Microprocessor. Functional **Units of Microprocessor** – ALU using IC 74181, Basic Arithmetic operations using ALU IC 74181, 4-bit Multiplier circuit using ALU and shift registers. Memory Organization and Operations, digital circuit using decoder and registers for memory operations.		
#Exemplar/Case Studies	Microprocessor based system in Communication /Instrumentation Control	
*Mapping of Course Outcomes for Unit VI	CO6	

Learning Resources

Text Books:

1. R.P.Jain, " Modern Digital Electronics", Tata McGraw Hill 4th Edition, ISBN 978-0-07-06691-16
2. Moris Mano, "Digital Logic and Computer Design", Pearson , ISBN 978-93-325-4252-5
3. G. K. Kharate, "Digital Electronics", Oxford Press, ISBN-10: 0198061838

Reference Books:

1. John Yarbrough, "Digital Logic applications and Design", Cengage Learning, ISBN – 13: 978-81-315-0058-3

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2. D. Leach, Malvino, Saha, "Digital Principles and Applications"‖, Tata McGraw Hill, ISBN – 13:978-0-07-014170-4.
3. Anil Maini, "Digital Electronics: Principles and Integrated Circuits"‖, Wiley India Ltd, ISBN:978-81-265-1466-3.
4. Norman B and Bradley, "Digital Logic Design Principles", Wiley, ISBN:978-81-265-1258

eBooks:

- https://www.springer.com/gp/book/9783030361952
- https://www.mheducation.co.uk/ebook-fundamentals-of-digital-logic-9780077144227-emea

MOOC/ Video Lectures available at:

- Digital Circuits, by Prof. Santanu Chattopadhyay, https://swayam.gov.in/nd1_noc19_ee51/preview (Unit I, II, III, IV)
- Digital Circuits and Systems, Prof. S. Srinivasan https://nptel.ac.in/courses/117/106/117106086/ (Unit I, II, III, IV)
- Microprocessors and Interfacing By Prof. Shaik Rafi Ahamed | IIT Guwahati https://swayam.gov.in/nd1_noc20_ee11/preview (Unit VI)
- Switching Circuits And Logic Design By Prof. Indranil Sengupta w https://swayam.gov.in/nd1_noc20_cs67/preview (Unit V)

@The CO-PO Mapping Matrix

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	-	2	-	-	-	-	-	-	-	-	-
CO2	2	1	2	-	-	-	-	-	-	-	-	-
CO3	2	1	2	-	-	-	-	-	-	-	-	-
CO4	2	-	2	1	-	-	-	-	-	-	-	-
CO5	2	2	-	-	-	-	-	-	-	-	-	-
CO6	2	-	-	-	-	-	-	-	-	-	-	-

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Savitribai Phule Pune University
Second Year of Computer Engineering (2019 Course)
210248: Digital Electronics Laboratory

Teaching Scheme	Credit Scheme	Examination Scheme and Marks
Practical: 02 Hours/Week	01	Term Work: 25 Marks

Companion Course : 210245: Digital Electronics and Logic Design

Course Objectives:

To understand fundamentals and functionality of electronic circuits, design and implement combinational circuits like MUX, comparator, adder/subtractor, design and implement sequential circuits like flip-flop, registers, and counters using different integrated circuits.

Course Outcomes:

On completion of the course, learner will be able to–

CO1: **Understand** the working of digital electronic circuits.

CO2: **Apply** the knowledge to appropriate IC as per the design specifications.

CO3: **Design** and **implement** Sequential and Combinational digital circuits as per the specifications.

Guidelines for Instructor's Manual

The instructor‘s manual is to be developed as a hands-on resource and reference. The instructor's manual need to include prologue (about University/program/ institute/ department/foreword/ preface), curriculum of course, conduction and Assessment guidelines, topics under consideration-concept, objectives, outcomes, data sheets of various ICs.

Guidelines for Student's Laboratory Journal

The laboratory assignments are to be submitted by student in the form of journal. Journal consists of prologue, Certificate, table of contents, and **handwritten write-up** of each assignment (Title, Objectives, Problem Statement, Outcomes, software and Hardware requirements, Date of Completion, Assessment grade/marks and assessor's sign, Theory- Concept, circuit diagram, pin configuration, conclusion/analysis).

As a conscious effort and little contribution towards Green IT and environment awareness, attaching printed papers as part of write-ups and program listing to journal may be avoided.

Guidelines for Laboratory /Term Work Assessment

Continuous assessment of laboratory work is done based on overall performance and Laboratory performance of student. Each Laboratory assignment assessment should assign grade/marks based on parameters with appropriate weightage.

Suggested parameters for overall assessment as well as each Laboratory assignment assessment include- timely completion, performance, innovation, efficiency, punctuality and neatness.

Guidelines for Laboratory Conduction

The instructor is expected to frame the assignments by understanding the prerequisites, technological aspects, utility and recent trends related to the topic. The assignment framing policy need to address the average students and inclusive of an element to attract and promote the intelligent students.

The instructor may set multiple sets of assignments and distribute among batches of students. It is appreciated if the assignments are based on real world problems/applications. Student should perform at least 12 experiments with all experiments from group A and any 5 assignments from group Band one from group C assignments.

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Virtual Laboratory:

- http://vlabs.iitb.ac.in/vlabs-dev/labs/dldgates/index.html
- http://vlabs.iitb.ac.in/vlabs-dev/labs/dldesignlab/index.html

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Suggested List of Laboratory Experiments/Assignments	
Sr. No.	**Group A**
1	To Realize Full Adder/ Subtractor using a) Basic Gates and b) Universal Gates
2	Design and implement Code Converters-Binary to Gray and BCD to Excess-3
3	Design and Realization of BCD Adder using 4-bit Binary Adder (IC 7483).
4	Realization of Boolean Expression for suitable combination logic using MUX 74151 /74153, DMUX 74154/74138
5	To Verify the truth table of two bit comparators using logic gates.
6	Design and Implement Parity Generator and checker using EX-OR.
	Group B
7	Design and Realization: Flip Flop conversion
8	Design of 2 bit and 3 bit Ripple Counter using MS JK flip-flop.
9	Design of Synchronous 3 bit Up and Down Counter using MSJK Flip Flop / D Flip Flop
10	Realization of Mod -N counter using (Decade Counter IC 7490) .
11	Design and implement Sequence generator (for Prime Number/odd and even) using MS JK flip-flop.
12	Design and implement Sequence detector using MS JK flip-flop.
	Group C
13	Study of Shift Registers (SISO,SIPO, PISO, PIPO)
14	Design of ASM chart using MUX controller Method.

@The CO-PO Mapping Matrix

PO/CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2	-	-	-	-	-	-	-	-	-
CO2	3	2	3	-	-	-	-	-	-	-	-	-
CO3	3	2	2	1	-	-	-	-	-	-	-	-

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