JSPM's

Rajarshi Shahu College of Engineering, Pune

Department of Electronics & Telecommunication Engineering

Academic Year: 2024-25 (sem II)

INNOVATIONS IN TEACHING AND LEARNING

Subject: Cmos Design & Verification **Class:** TY BTech (B Div)

Topic: Lay out Design Rules in VLSI

NAME OF THE ACTIVITY:

I. **Concept:** Use of Microwind Simulation tool

II. **Objective(Goal):** Self learning , Exchange of knowledge ,

III. **Appropriateness (Relevance of Selected Method):** This method forces students to get in depth knowledge of Layout design rules.

IV. **Effective Presentation (Implementation Details):**
Student draw layout of given digital unit. Simulate the same using Microwind simulation tool, Obseeve the various performance parameters with variations in design in terms of L, W.

V. **Results (Impact):**
It helps students to visualize and simulate circuits, at the layout level. verify designs against technology constraints and explore different design techniques.

VI. **Reproducibility and Reusability by Other Scholars for Further Development**

Sr.No	Innovation Used by	Details of User	Purpose of Reproducibility and Re usability
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VII. PEER REVIEW AND CRITIQUE

Category: Internal/External/Interdepartmental

Score: (1:Least 2: Moderate 3:Highly)

Question 1. Is this Innovative Teaching and Learning Methodology useful during content delivery?

Question 2. Did this innovation increase student motivation or participation?

Question 3. Will it show improvement in student learning?

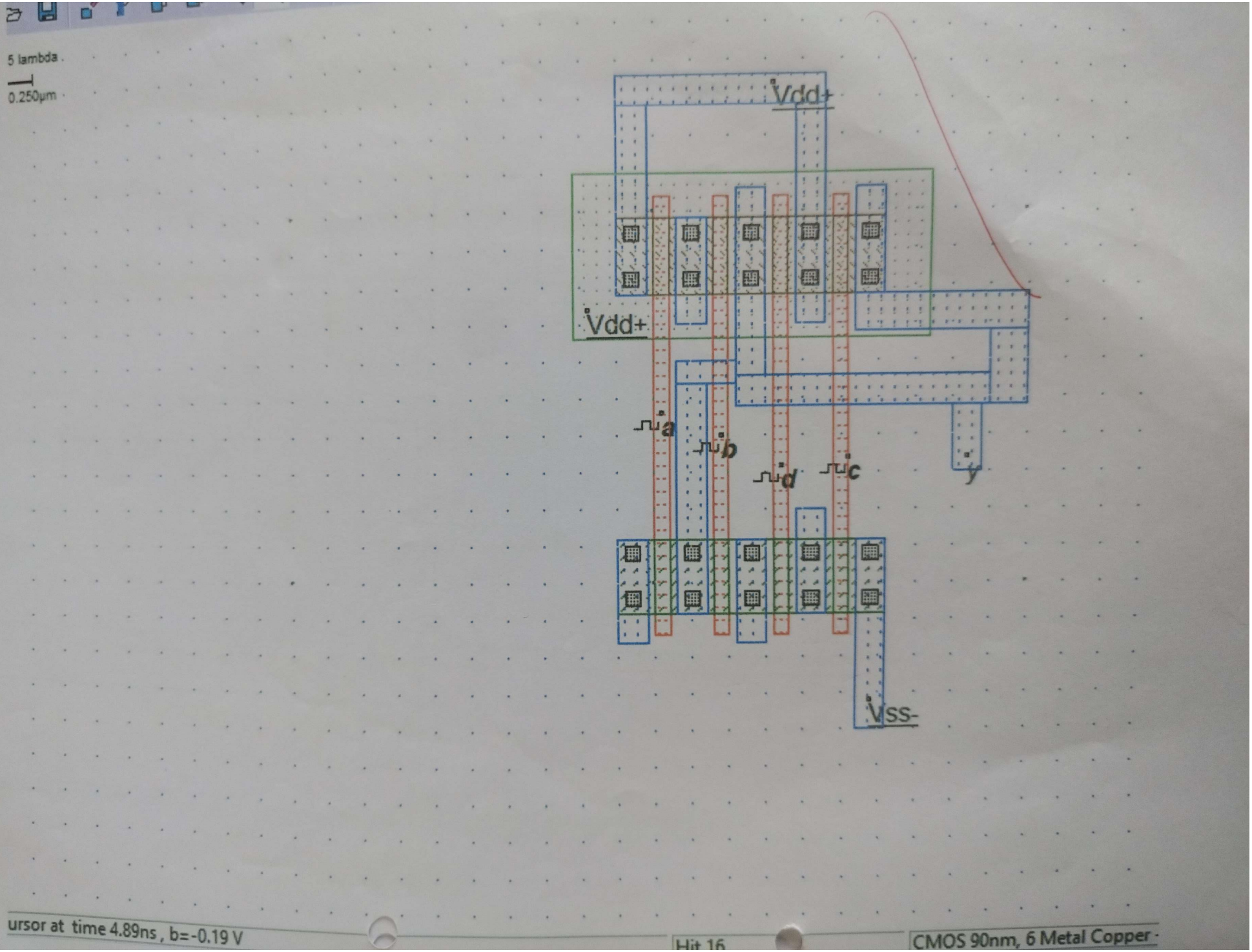
Question 4. Suggestions for improvement in future iterations.

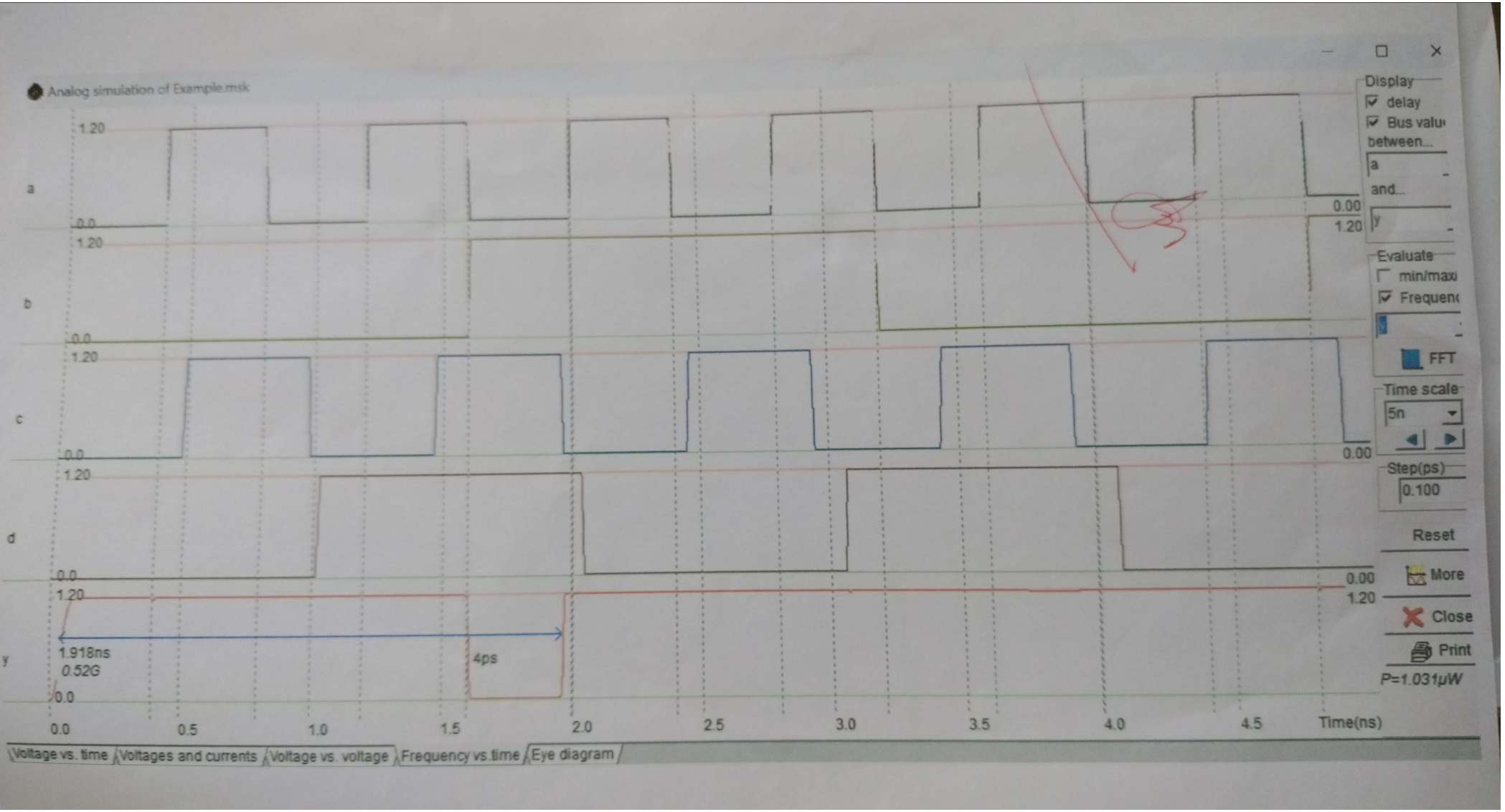
Category	Name of Peer	Organization	Q.1	Q.2	Q.3	Q. 4 Suggestion/Critique
Internal	Dr. S. C. Wagaj	RSCOE	3	2	3	Performance Parameter increase

Course Co-ordinator
Dr. Sakshi Paithane

Module Co-ordinator
Dr. Sakshi Paithane

HOD E&TC
Dr.S.C.Wagaj:


5 lambda
0.250µm
Vdd+
Vdd+
a
b
d
c
y
Vss-
ursor at time 4.89ns , b=-0.19 V
Hit 16
CMOS 90nm, 6 Metal Copper


Analog simulation of Example.msk
a
b
c
d
y
1.20
0.0
1.918ns
0.52G
4ps
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
Time(ns)
Display
delay
Bus valu
between...
a
and...
y
0.00
1.20
Evaluate
min/max
Frequen
FFT
Time scale
5n
Step(ps)
0.100
Reset
More
Close
Print
P=1.031μW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram