JSPM's

Rajarshi Shahu College of Engineering, Pune

Department of Electronics & Telecommunication Engineering

INNOVATIONS IN TEACHING AND LEARNING

Subject: CMOS Design Verification **Class:** T.Y. BTech E&TC

Topic: VHDL code program and CMOS circuit design

NAME OF THE ACTIVITY: VHDL code programming and CMOS design and layout

I. **Concept:** Simulation and synthesis using tools like Xilinx, ModelSim, Vivado Stick diagrams and layout drawing.

II. **Objective (Goal):** To design and simulate digital circuits using VHDL for real-world applications. To understand and implement CMOS logic gates and analyze their electrical behaviour.

III. **Appropriateness (Relevance of Selected Method):** Highly aligned with industry-standard tools and design practices. Prepares students for VLSI, ASIC, FPGA, and EDA tool-based careers. Enables application of MOSFET-level understanding in CMOS layouts and VHDL modelling.

IV. **Effective Presentation (Implementation Details):**

1) To write VHDL code, simulate with test bench, synthesis, implement on PLD 4 bit ALU for add, subtract, AND, NAND, XOR, XNOR, OR

YouTube Link: https://www.youtube.com/watch?v=ECR1Aj4LUgI

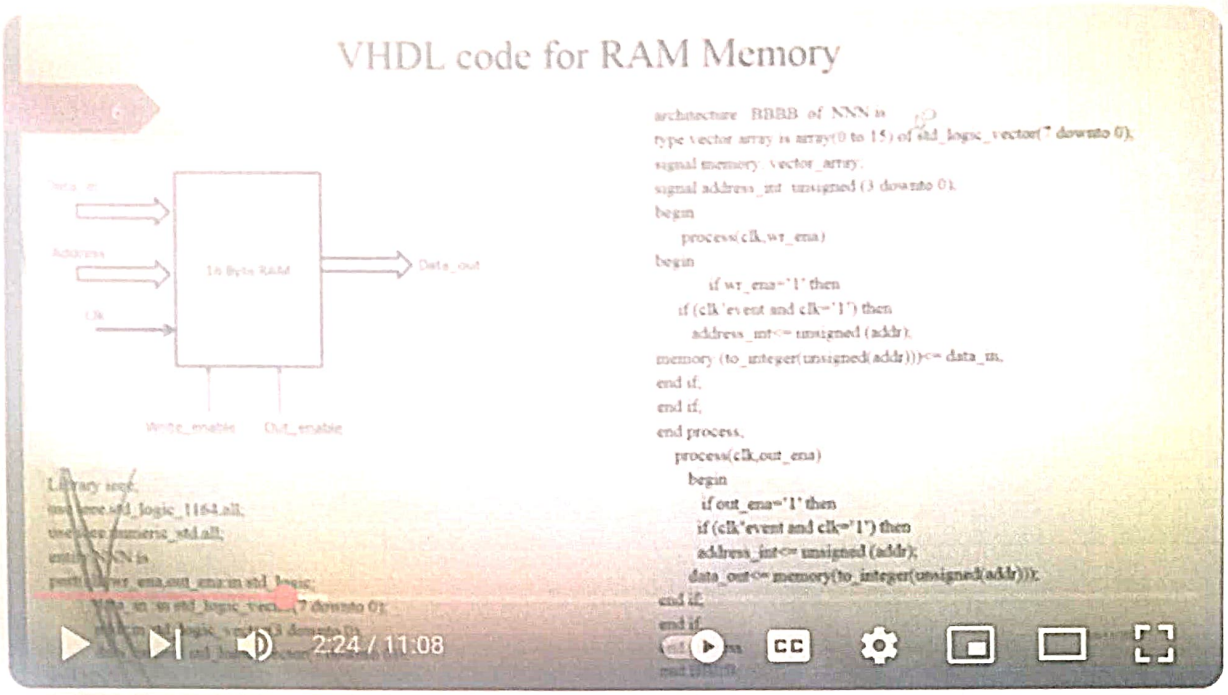
2) To write VHDL code and test bench, synthesis, simulate and download into PLD of 4 bit bidirectional shift register.

You Tube Link: https://www.youtube.com/watch?v=mm0ycI4rPGI

3) To design following logic, prepare layout in multimetal layers and simulate. Assume suitable technology, load capacitance free running frequency, switching timing etc. CMOS NAND, NOR

You Tube Link: https://www.youtube.com/watch?v=tC3F5it_T08

YouTube Search



CMOS NOT, NAND, NOR

@manavlimkar4543 2 years ago
No extra pictures, no extra drama, straight to the point !
1 Reply

@rohitkumarpatil5576 2 years ago
Nice video and helpful
Reply

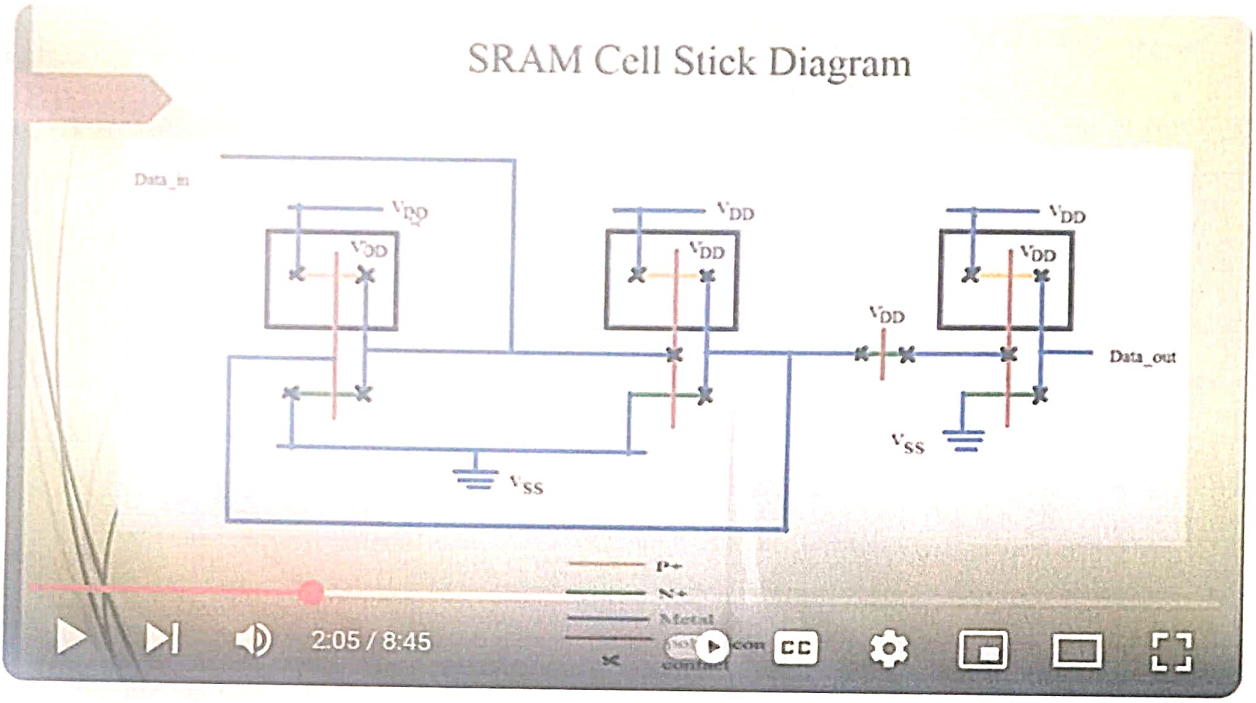
@suyashshinde5260 2 years ago
Reply

@mrunalmore7726 2 years ago
Well explained
Reply

Design a layout for Single Bit SRAM Cell using CMOS Technology.

You Tube Link: https://www.youtube.com/watch?v=t2MSO9YXgrY

YouTube Search



Experiment Title: Single Bit SRAM Cell.

@thenehajadhav 2 years ago
Really usefull.
Reply

@rohitkumarpatil5576 2 years ago
Nice explanation
Reply

@omkarwali49 2 years ago
Teaching method is very nice and rthymic!!!
Reply

@mrunalmore7726 2 years ago
Really helpful vdo !!
Reply

@suyashshinde5260 2 years ago
Clearly explained!
Reply

V. Results (Impact):

- **Improves problem-solving and design skills** by transitioning from logic gates to complex systems.
- **Boosts employability** in domains like VLSI, embedded systems, and digital design.
- Builds a strong base for **higher education or research** in microelectronics and embedded systems.

VI. Reproducibility and Reusability by Other Scholars for Further Development

Sr.No	Innovation Used by	Details of User	Purpose of Reproducibility and Reusability
1	B Tech students	students	A reproducible CMOS layout ensures that chip fabrication results will match simulation predictions.

VII. PEER REVIEW AND CRITIQUE

Category: Internal/External/Interdepartmental

Score: (1:Least 2: Moderate 3:Highly)

Question 1. Is this Innovative Teaching and Learning Methodology useful during content delivery?

Question 2. Did this innovation increase student motivation or participation?

Question 3. Will it show improvement in student learning?

Question 4. Suggestions for improvement in future iterations.

Category	Name of Peer	Organization	Q.1	Q.2	Q.3	Q. 4 Suggestion/Critique
Internal	S. A. Paithane	JSPM's RSCOE	3	2	3	Add Advance tool.
External	Subhas Patil	Marvel Semicondn	3	3	2	Use lateast Hardware discription lang.

Course Co-ordinator
Dr. S. C. Wagaj

Module Co-ordinator
Dr. S. A. Paithane

HOD E&TC
Dr.S.C.Wagaj:

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