E.ON Energy Research Center | RWTH AACHEN UNIVERSITY

A project report submitted to Institute for Automation of Complex Power Systems RWTH Aachen.

Simulation and Test of Micro-grid Dynamics

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1. Setup Description

1. Inverter Module:

The microgrid system was modelled as per the parameters provided in the Assignment. The two local energy sources were represented by constant DC voltages. A full-bridge module was used for the Inverter. IGBT modules were used and the gate signals were driven by PWM signals generated SVPWM (State-Vector PWM) module.

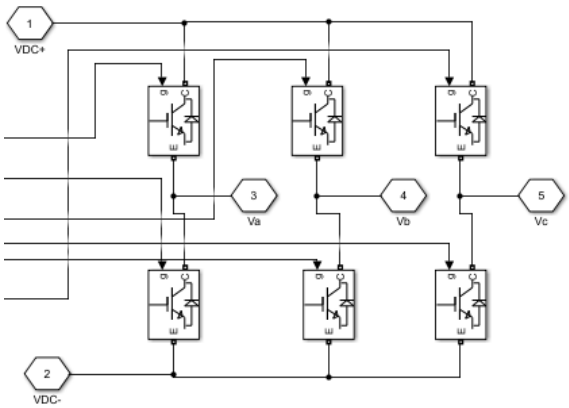

Fig: The Inverter Topology

2. LCL Filter:

The line currents were being measured at the output of the Inverter and the output voltage across the LCL filter Capacitor banks by using necessary current and voltage measurement units.

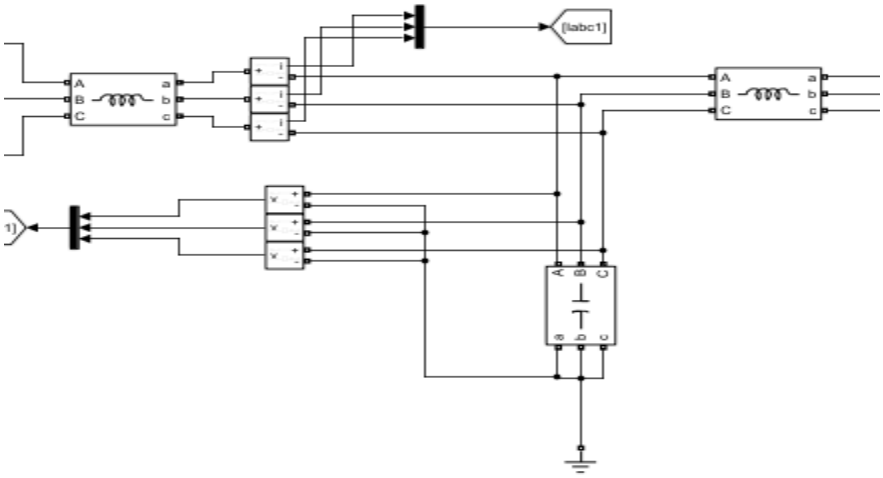

Fig: The LCL filter with current and voltage measurement

3. Controller Design:

The Local Controller is designed using the Nested Control Topology. The controller has two-levels of control – the current control loop and the voltage control loop.

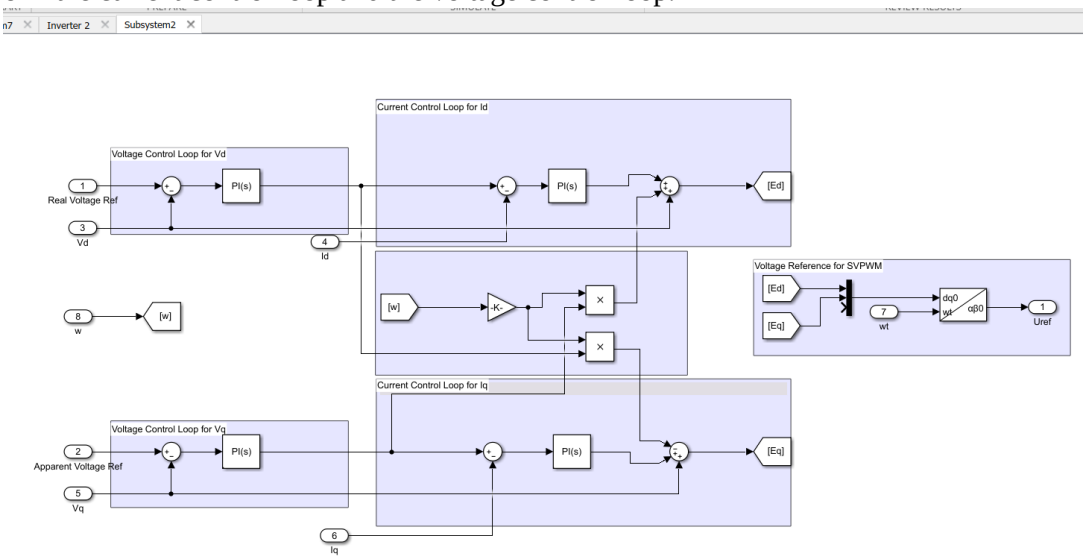

Fig: The Inner Current Control Loop and the Outer Voltage Control Loop

The current control loop is the Inner Control loop and is designed to be the fastest. It is designed by considering the pole cancellation of the load. The Load here is characterized by a Resistor. Moreover, we have Inductance and Resistance provided by the Line. So, we design our Controller such that the poles introduced by the Load and the Line is cancelled by the Current control loop.

$$K_P + \frac{K_I}{s} = R + sL$$

$$\frac{K_I + sK_P}{s} = R + sL$$

From the above equations, equating the numerators, the gains K_p and K_I can be computed for the PI controllers in the Current Control Loop. The Current Control Loop generates the necessary Voltage Reference for the SVPWM, which drives the inverter Gate Signal pulses.

The voltage control loop is the Outer Control loop and it generates the reference current inputs for the inner control loop. It is designed such the error between the measured and the reference voltages are reduced and the necessary reference current tracking point is provided to the Inner Control Loop.

The command ‘pidtunes’ was used in the matlab script to compute the PID gains of the controller. Since, the switching frequency is 10kHz, the bandwidth of the Current control loop was assumed to be 1kHz and the bandwidth for the Voltage control loop was assumed to be 100Hz for computing the Controller gains.

4. Inverter Module:

The nested control loops designed above is preceded by a Droop Logic unit. This unit makes sure that the necessary deviations introduced to the frequency and voltage of the system is taken care by the droop unit.

The droop unit takes measured power as input and compares it with the reference power values to generate reference voltage signals and phase angles. This reference value is then used to generate the reference sinusoidal voltage for the Nested Loop Controller designed previously. The gains needed for the Droop Unit is calculated using the below formula:

$$K_w = \frac{\Delta w}{\Delta P_{max}}$$

$$K_v = \frac{\Delta V}{\Delta Q_{max}}$$

5. Power Calculation Unit:

The droop unit is preceded by power calculation unit, which computes the power values from the voltages V_d, V_q, I_d, and I_q.

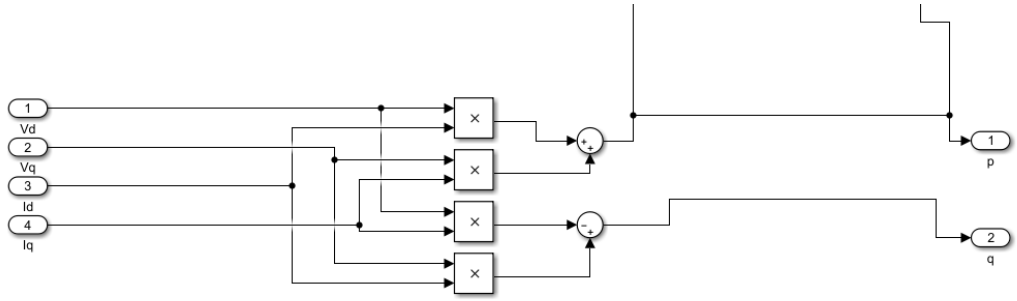

Fig: Power Calculation block

6. Frame conversion (abc-dq) unit:

And the first block in the whole control loop is the voltage conversion block which converts the measured 3-phase voltages and currents to d-q frame. The d-q frame is then further passed through a set of low pass filter to discard the disturbances.

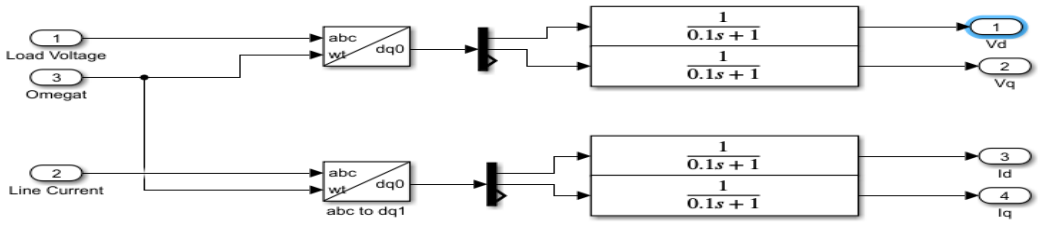

Fig: Voltage Conversion block

2. Simulation & Results

Run the Control Design Script to initialize the parameter values and the respective controller gains. Once the initialization is done, run the Simulink Model. The simulation runtime is set to 1sec and the step change in the load is introduce at 0.4s. This is achieved by adding a parallel resistance of 200Ω using a 3-phase circuit breaker.

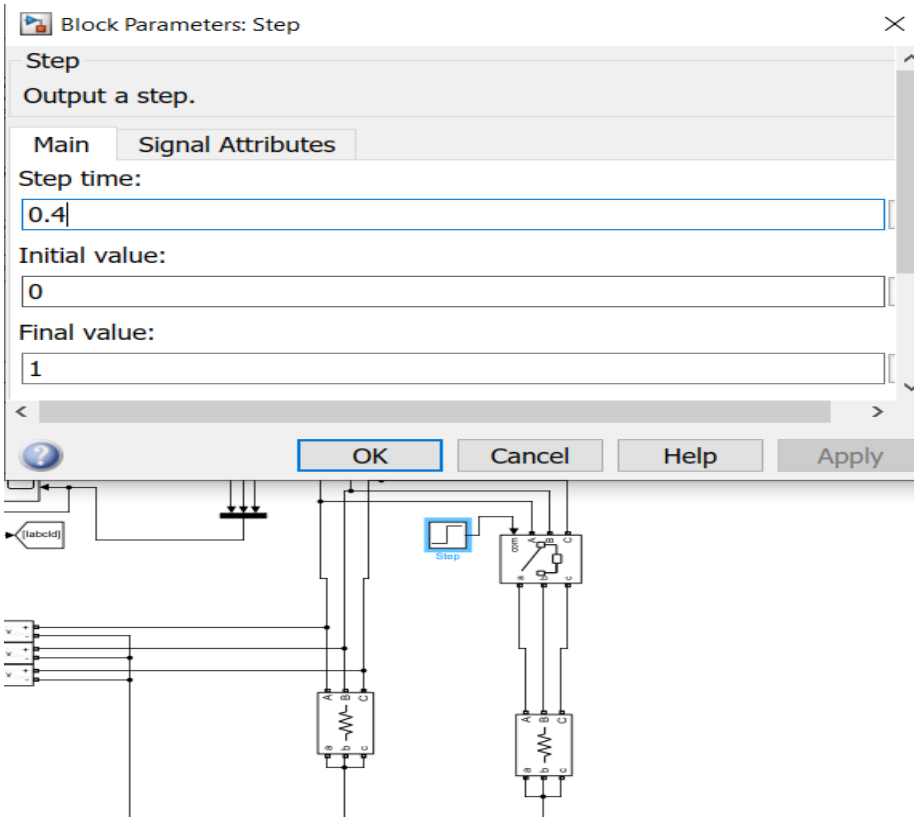

Fig: Step change of Load

Once the Simulation is run successfully, following results were obtained. The Inverters could drive the Phase voltage across the load to approximately 310V of peak values. The RMS voltage measured across the Load resulted to 202V.

After the introduction of the step disturbance, i.e., changing of the Load value from 50 Ω to 40 Ω, the voltage profile seems to be stable and the current profile across the load increases accordingly. The values can be seen below in the current output profile.

The whole system designed ends up having a THD of 6.2% approximately, which is allowable as per IEEE 519-2014 (for bus voltage below 1kV).

The system looks stable after the disturbance and the system frequency seems to be well with the allowed range. The voltage reaches up to 202V and the voltage profile seems to be stable there, instead of the step decrease in load at 400ms.

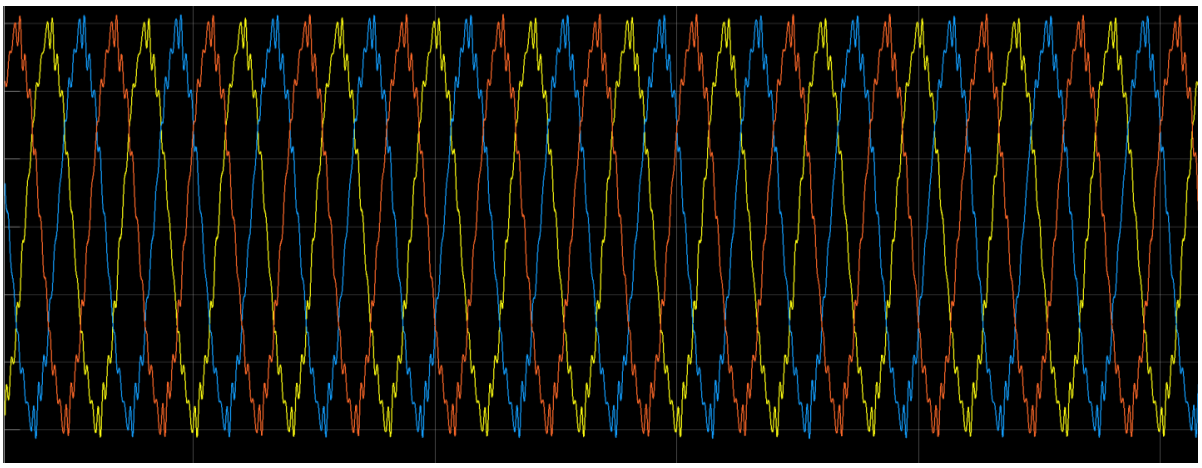

Fig: The 3-phase Voltage generated as output of Inverter-1 with THD-6.2%

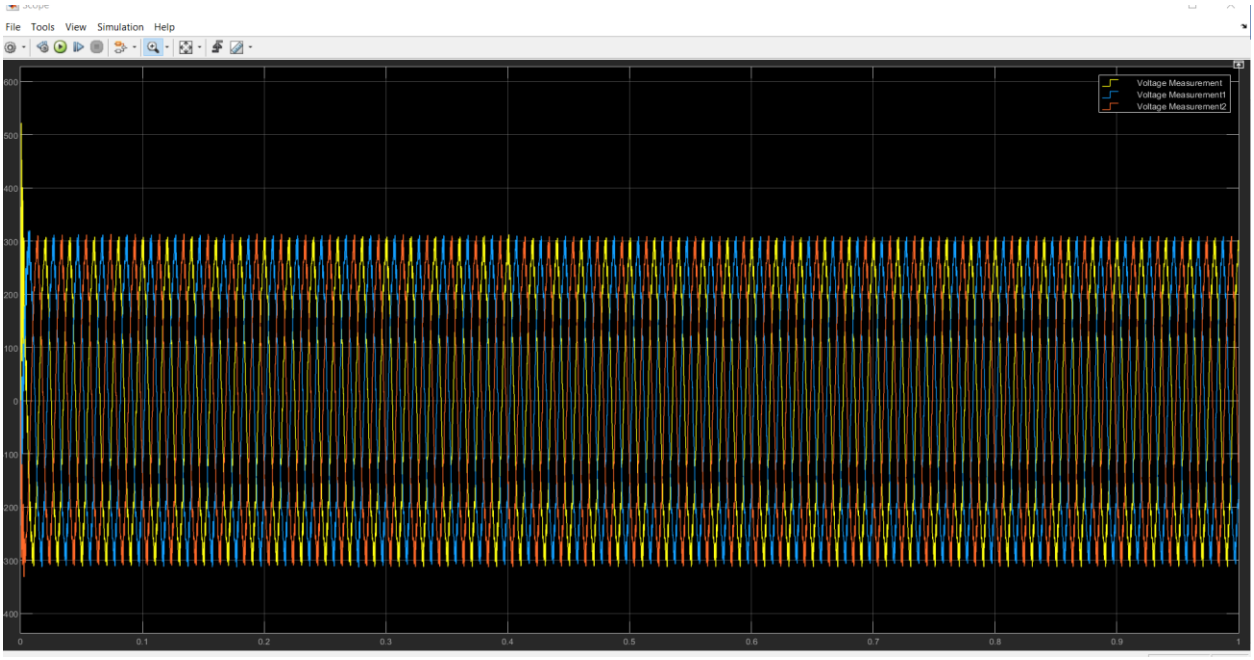

Fig: 3-phase Voltage out of Inverter-1 for whole cycle of simulation with THD-6.2%

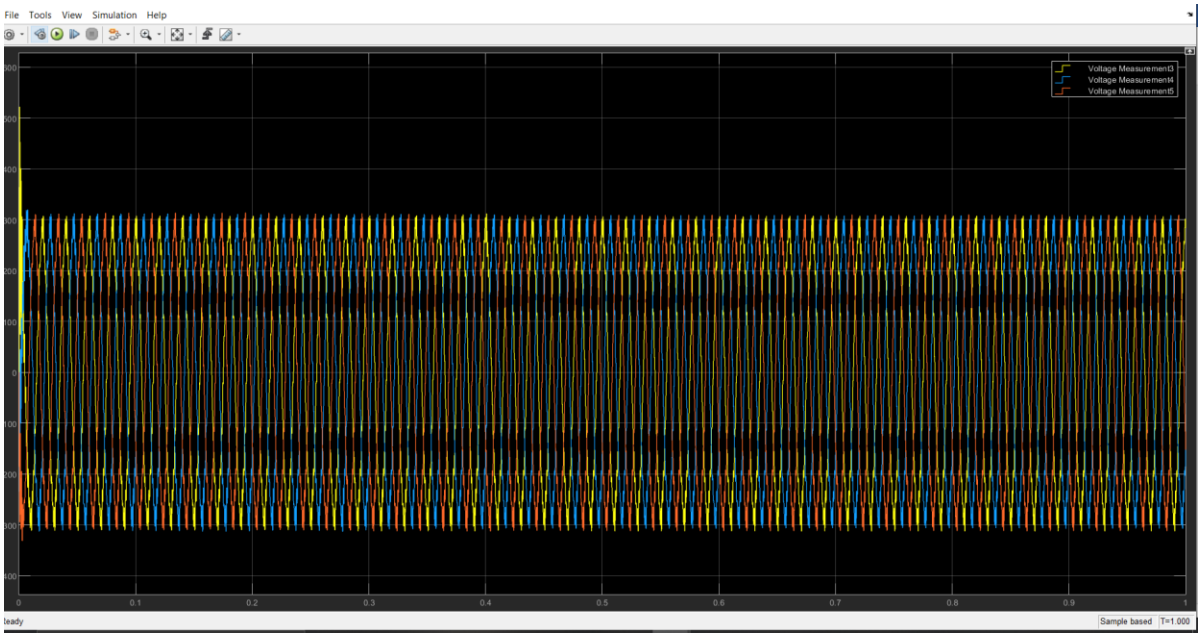

Fig: 3-phase Voltage out of Inverter-2 for whole cycle of simulation with THD-6.2%

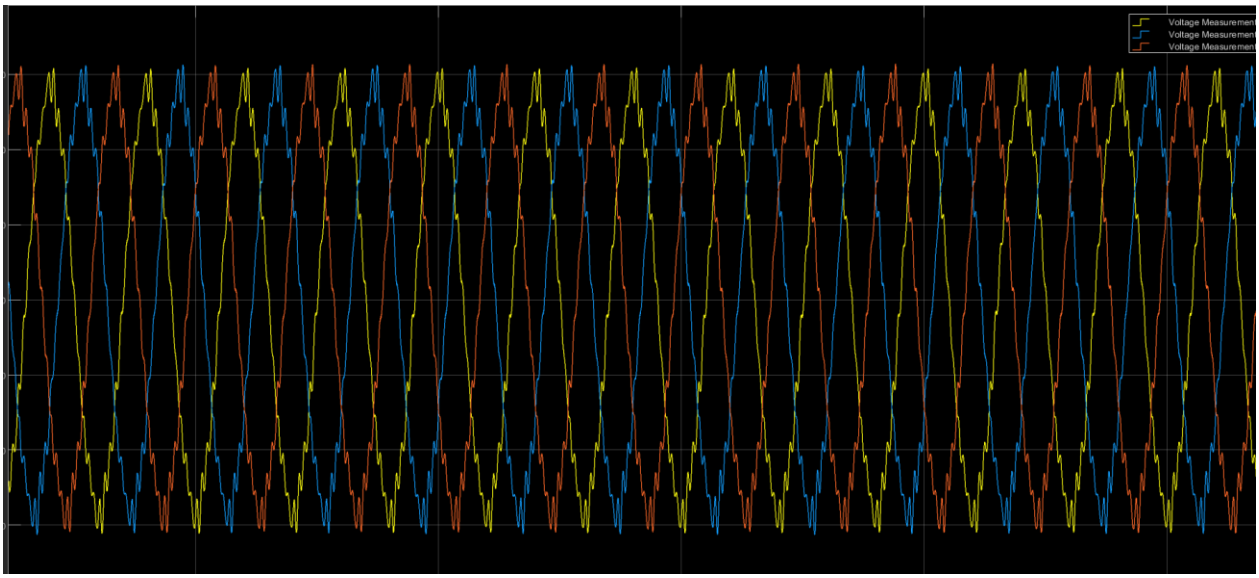

Fig: The 3-phase Voltage generated as output of Inverter-2 with THD-6.2%

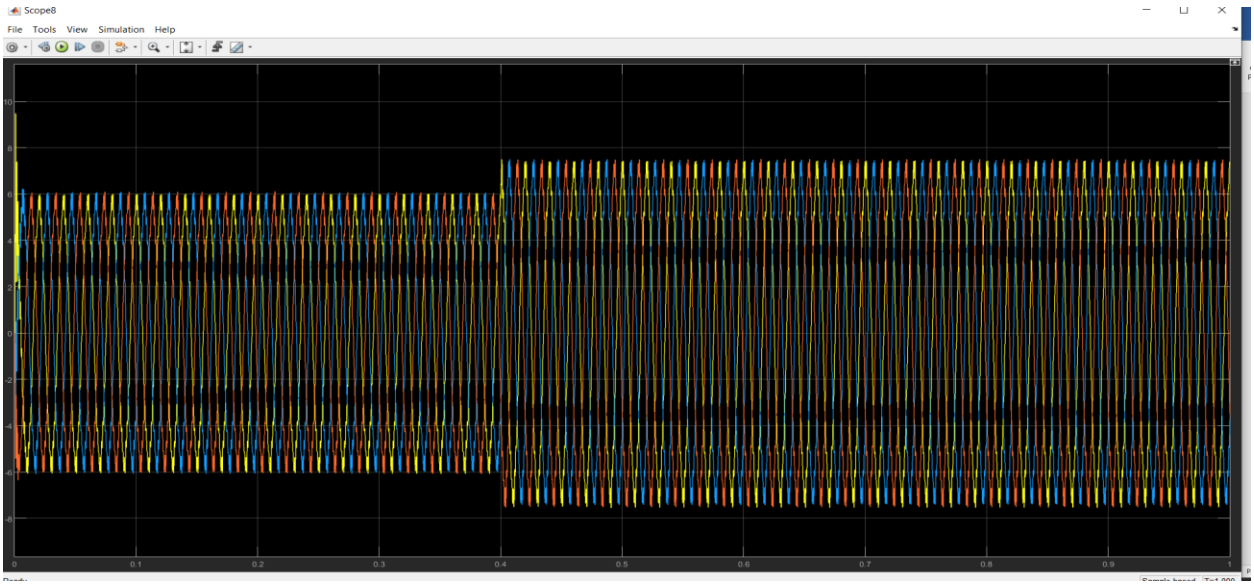

Fig: The 3-phase current through the load for the whole simulation cycle with THD-6.2%

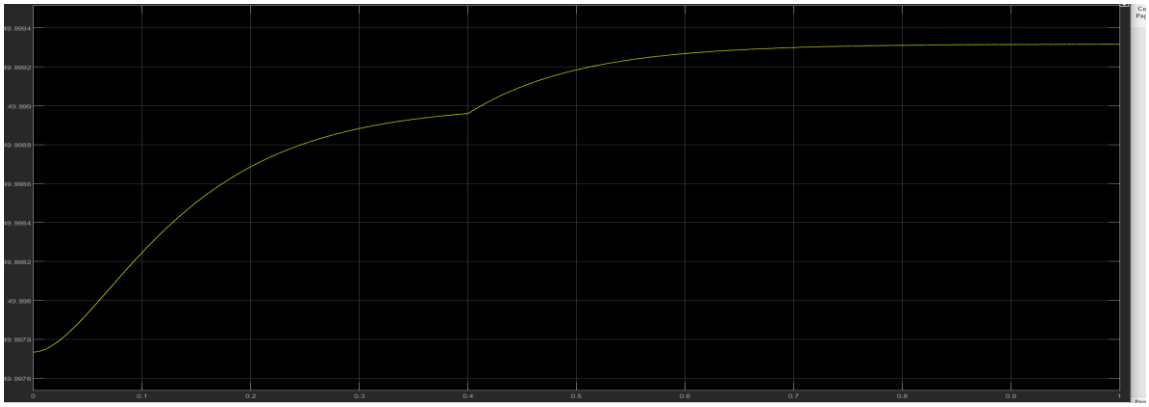

Fig: The frequency stabalization at the droop

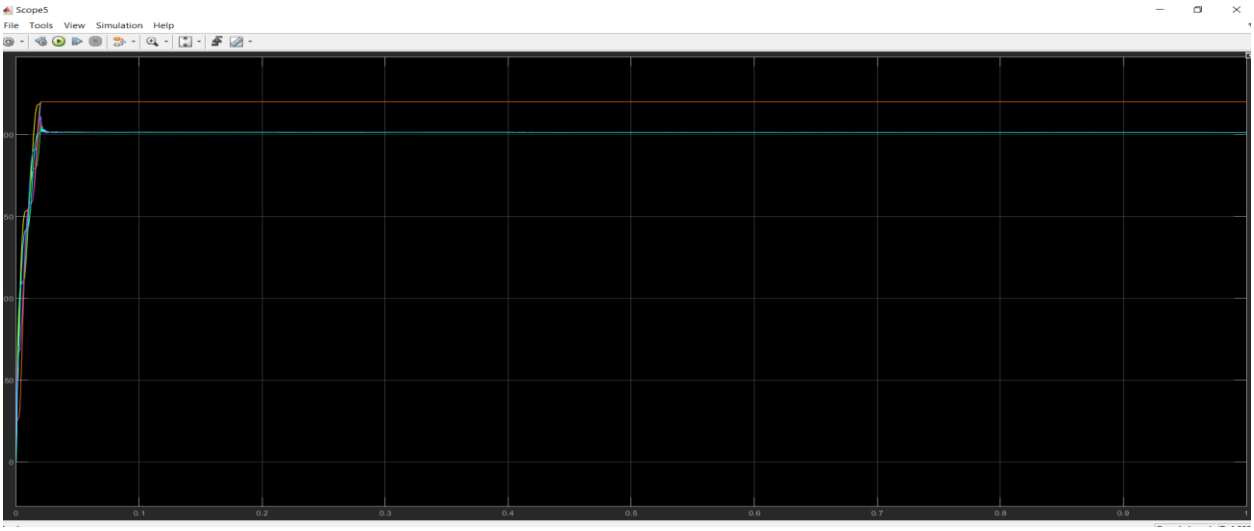

Fig: Voltage dynamics