Determining Golden Process Routes in Semiconductor Manufacturing Process for Yield Management

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Abstract - **Managing the yield of wafer is one of the most important tasks to the semiconductor manufacturers. A lot of efforts for enhancing the yield of wafer have been conducted in both industries and academia. Thanks to the advance of IoT and data analytics techniques, huge amount of process operational data, such as indices of process parameters, equipment condition data, or historical data of manufacturing process, is collected and analyzed in real-time. Though the amount and availability of process operational data have been increased, existing yield management approaches on semiconductor manufacturing process have only considered a single process or few processes among the overall processes. This study proposes a way to find process routes which maximize the yield of wafer (i.e., golden process routes) in view of multiple process steps. This work is expected to complement the existing efforts for managing the yield of wafer by adding results of process-oriented analysis.**

Keywords - **Yield management, Golden process route, Semiconductor manufacturing process**

I. INTRODUCTION

Semiconductor manufacturing is one of the most complex works that has hundreds of process steps, several kinds of wafers, machinery, re-entrant flow, and innumerable process parameters, so it takes few months for completing the whole processes accordingly [6, 12]. Also, since semiconductor manufacturing process is very sensitive on stream, yield management is one of the most important issues directly connected to survival of a company.

A lot of efforts have been carried out to manage the yield of semiconductor manufacturing process. Several researchers used experimental design methods (e.g., multi-response surface methodology or Taguchi method) for optimizing conditions of process parameters in order to improve the yield of wafer. On the one hand, data mining approaches, such as feature selection or classification algorithm, are widely used for predicting potential defect of wafer. In addition, recently, deep learning approaches, such as neural network or genetic algorithm, are used for enhancing prediction quality of the yield of wafer using process operational data.

Although such efforts have significantly contributed to improve overall quality of semiconductor manufacturing process, they could not analyze the whole manufacturing processes but focus on a single process step or a series of process steps. However, with the aid of advance of IoT and data analytics methods, availability of process operational data has been increased. According to such change, there can be an improvement point on existing yield management approaches in terms of utilizing process operational data from the overall semiconductor manufacturing processes. Thus, this study investigates a way to find process routes which maximize the yield of wafer. This analysis procedure is expected to complement the existing yield management approaches.

The paper is organized as follows. Existing approaches that manage the yield of wafer on semiconductor manufacturing process and their limitations are covered in the next section. After that, the authors suggests a conceptual framework of yield management in the view of overall manufacturing processes. The authors are going to discuss about strengths of our proposed concept which complements to the existing approaches. Finally, conclusions and future research directions are provided in the last section.

II. LITERATURE REVIEW

Since higher complexity and sensitive characteristics of semiconductor, yield management is one of critical issues on the overall manufacturing processes. Yield management of semiconductor manufacturing process can be divided into two major ways: 1) yield improvement through finding and adjusting optimal conditions of process parameters and 2) fault detection and yield prediction of wafer through analyzing process parameters.

A. Literature on yield improvement

Yield improvement through finding and adjusting optimal conditions of process parameters is a one of process optimization activities based on experimental design. Experimental design is used to examine the relationship between process input and output parameters (i.e., to study the effect of input parameters on the output parameters systematically). Since the complexity of semiconductor and its manufacturing processes continuously grow, several output parameters should be considered simultaneously. Multi-response surface methodology (MRSM) is one of typical experimental design methods used for this circumstance. MRSM is a systematic statistical method evaluating the influence of input parameters, searching optimal conditions of input

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parameters, and building prediction models for output parameters [2, 13].

A number of recent studies focused on finding optimal conditions of process parameters using MRSM. MRSM via harmony search algorithm is applied to wire bonding process optimization on semiconductor manufacturing process. Temperature, flow rate, and heater block temperature are three input process parameter which are influential to six output parameters. As a result, this approach showed efficient performance to find optimal conditions of input parameters compared to existing optimal search algorithms [1]. MSRS is also applied to to chemical and mechanical planarization (CMP) process in order to optimize three response variables that are critical to the final yield of semiconductor [9]. In this study, they adopted clustering method in order to find optimal solution, then they found optimal blend of the mixture slurry conditions. Another study investigated the optimization of the three components in polishing slurries for W barrier CMP process using MRSM [11]. As a result, they achieved better quality of wafers using the optimal conditions from MRSM.

Such studies have provided optimal conditions of process parameters on a certain process (e.g., CMP process) using experimental design. However, those works have limitations that they conducted experiment using limited sets of data. Since measuring and considering all combinations of process parameters is extremely costly in real environment, they selected part of influential input parameters. Thus, it may cause loss of information and requires additional test and prediction work using derived optimal conditions of parameters. In addition, they tried to optimize a single process, not several processes due to limited set of data. As a result, these approaches could not consider interactions among a series of processes came from finding optimal conditions of parameters on a certain process.

B. Literature on fault detection and yield prediction of wafer

As the availability of process operational data has been increased, fault detection and yield prediction research has been progressed continuously using data mining approach. Existing studies focused on extracting significant features to reduce the complexity of process operational data dimensions and increase the accuracy of fault detection of wafer. A feature extraction method based on spline regression model using sensor signals was proposed [10]. There is another study which combined feature selection method (i.e., principal component analysis) and classification method (i.e., support vector machine) in order to identify key parameters and detect fault on wafer [14]. Deep learning algorithm, (i.e., stacked denoising autoencoder (SdA)) is also applied to establish a fault detection model with minimizing loss of information from process operational data [7].

On the one hand, the prediction of final yield of wafer during semiconductor fab operations is also important for reducing cost and increasing productivity and profitability. The accurate prediction model of yield will play a role as a warning signal and help to make a decision of production plan [12]. A novel approach was suggested to improve wafer effectiveness and provide an IC feature design guideline associated with reducing cost [3]. A hybrid method which combines SVM and neural network model was designed to predict accuracy of yield and defective wafers in early [4]. Fuzzy neural network is also used for developing yield prediction model for improving prediction accuracy [12].

However, although those studies have contributed for detecting defective wafer or predicting the final yield of wafer using process operational data, they could not take the whole manufacturing processes into account. Existing studies only focused on a unit process step or connected process steps, not the whole manufacturing processes. As a result, as mentioned above, it is time to need an extended view which considers multiple process steps when managing the yield of wafer.

III. A CONCEPTUAL PROCEDURE OF DETERMINING GOLDEN PROCESS ROUTES FOR YIELD MANATEMENT

The conceptual procedure of determining golden process route for yield management consists of three steps: 1) Critical process steps identification, 2) Process route selection, and 3) Lot dispatching rule decision (see Fig. 1.).

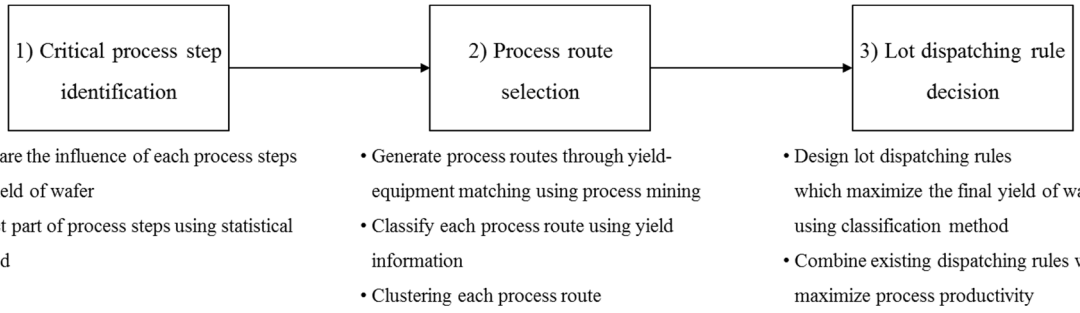

Fig. 1. A proposed conceptual procedure of determining golden route

Each step is explained in the following way.

1) *Critical process steps identification*: Semiconductor manufacturing process consists of hundreds of consecutive process steps and each process step consists of several process equipment in parallel generally. In addition, each equipment collects process operational data (e.g., process start/end time, process name (or code), information of input lot (and wafer), equipment code, or etc.) in real-time. Due to the above complexities, as the manufacturing process progressed, there are infinite number of process routes that can be selected by wafers. Process route means the historical record of each wafer during semiconductor manufacturing processes. Each process route consists of several types of information, such as aggregation of passed process steps and equipment of each wafer or operational conditions on each on-stream process step. Once we try to manage the yield of each wafer, considering a number of process routes is inefficient. Therefore, identifying critical steps which influence to the yield of wafer among the whole manufacturing processes is needed. Statistical method, such as ANOVA or regression analysis, can be a good way to identify the critical process steps. Indices of process steps capability (e.g., c_{pk} or p_{pk}) or condition parameters of equipment (e.g., temperature or pressure) can be used as influential factors when identifying the critical process steps.

2) *Process route selection*: Once critical process steps are identified, we can generate process routes of each wafers by analyzing lot information and process historical information collected from equipment on critical process steps. Process mining method will be suit for analyzing the information. Process mining analyzes process logs (i.e., lot history, process start/end time of equipment, or etc.) in order to generate process routes [8]. As generating the process routes, each yield of wafer is matched with processed history based on process logs (see Fig. 2). Once each yield and process route of wafer is matched, then we can classify each process route based on yield information into high yield process routes, namely golden process routes, and low yield process routes, namely worst routes. This route information will be valuable to decide lot dispatching routes during manufacturing processes. In addition, clustering analysis onto each classified route group (golden process routes and worst process routes) enables to extract characteristics of process routes, best/worst performance conditions of equipment, compatibility among equipment, or key performance equipment.

3) *Lot dispatching rule decision*: As completing step 2), we have information about process routes with high and low yield of wafer and results of clustering analysis. These result is now used for decision making problem on lot dispatching rule. Each lot has a predefined process schedule before going into the manufacturing processes. In this circumstance, whenever each lot arrives a critical step, information about process route of the wafer (high and low yield route) enables to advice a future processing route for the predefined schedule. In this sense, the process schedule of each lot can be customized by the information from step 2) in order to maximize the final yield of wafer. Existing classification algorithms, such as C4.5 or CART, will be useful to decide the process route.

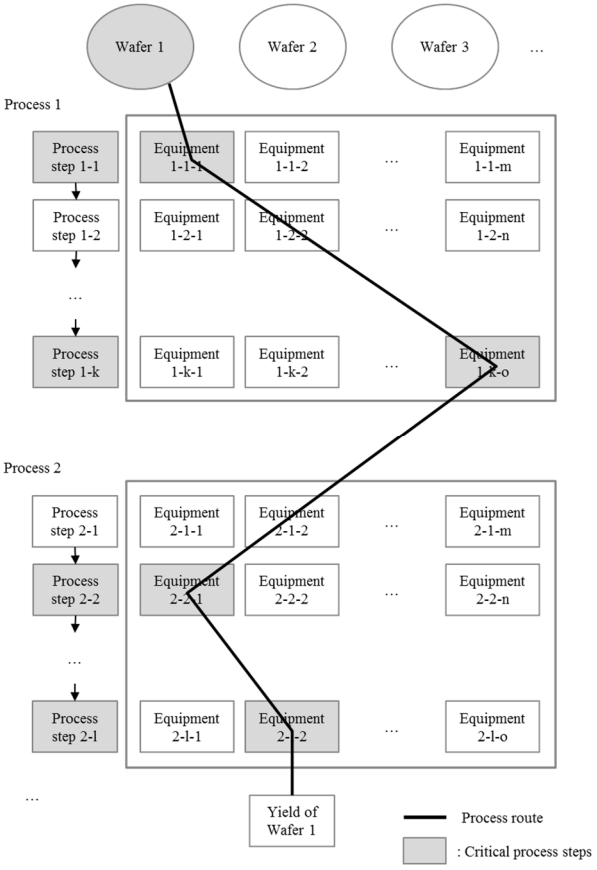

Fig. 2. Description of yield of wafer and process route matching

This process-oriented yield management framework has several advantages. First, it enables to understand the characteristics of each equipment more detail while operating. Since various process routes of wafers are classified, associated information of each equipment (e.g., processing time, change of temperature or pressure of equipment, or etc.), which affect to the yield of wafer, can be analyzed. In addition, operational data from equipment is relatively easy to collect and its amount is large in quantity compared to the inspection data of wafer. Because wafer inspection needs independent process steps and time, but operational data from equipment is collected through mounted sensors in real-time.

Second, it supports to more intuitive understanding of the whole semiconductor manufacturing processes to engineer and manager. Existing studies only consider some process steps, because collection of inspection and metrology data is not available on the whole processes [5]. However, on the other hand, equipment operational data is available on the whole processes, process route information based on the equipment operational data provides global viewpoint. In addition, classifying the yield of wafer based on its process route help to find exceptional cases (e.g., variations or re-entrant) during

manufacturing process which may effect to the yield of wafer. Furthermore, as process route information is cumulated, wafer dispatching rule can also be improved. It means that fine quality equipment can be matched with fine quality wafer in order to maximize the yield of wafer. Consequently, process route information plays a role as a dispatching guideline as well.

Third, it makes a connection with existing yield improvement, fault detection and yield prediction. The proposed procedure will contribute to find the 'golden process route (i.e., process route that shows the high yield of wafer)' by analyzing process route information associated with the yield of wafer. Then, existing yield management approaches can be applied to the golden process routes in several ways. In other words, the existing approaches help to discover optimal operational conditions of equipment on critical process step, predict the final yield based on the golden route, or potential root causes of defective wafers using the critical process step information. As a result, we can expect the synergy effect by integrating golden process route and the existing yield improvement approaches.

Additionally, although it aims to maximize the yield of wafer, productivity perspective should be considered as well. Practically, due to the large amount of production and limited number of process equipment, maximizing the yield of all wafers will hinder the productivity of semiconductor manufacturing process. Therefore, future lot dispatching rule should consider both yield and productivity simultaneously. As a result, investigation about integrating a designed new dispatching rule based on golden process route and existing dispatching rule is required. In addition, this study is a conceptual investigation and preemptive attempt, more specific methodology should be investigated further.

IV. CONCLUSION

This paper aims to propose a procedure of finding golden process routes for yield management. The proposed approach is expected to complement the existing yield management approaches on the semiconductor manufacturing process. The proposed procedure combines process mining approach, existing statistical methods and data mining approaches to cover multiple processes during manufacturing. The golden process routes and associated information add a process-oriented view to the existing yield management approaches for enhancing the yield of wafer. The existing limitation, hard to handle the overall process caused by the complexity of semiconductor manufacturing process, will be relieved by utilizing process operational data from equipment. However, since this study is a conceptual attempt, follow-up studies which utilize actual process operational data are required to verification.

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