RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
14:332:473 Introduction to VLSI Design
Assignment VI
Assigned: November 22, 2004
Due November 29, 2004

Reading Assignment: Chapter 6 of Weste and Harris.

No collaboration is permitted on this assignment. Your work must be your own. You must turn in theses specific items for each question to receive credit:

- Schematic Composer logic schematic (Problem 1).
- Schematic Composer transistor schematic (Problem 2).
- Virtuoso layout produced manually (Problem 2).

Problems:

1. **Register File Cell Schematic.** Design a register file cell using ordinary CMOS logic that can be laid out by abutment so that data can move freely from right to left in all rows of a cell matrix, which we call a *register file*. The more cells you put on the chip, the bigger and wider your register file becomes. Cells are arranged in a matrix whose dimensions are the number of bits in a word $\times$ the number of words in a register file. The cell must be able to shift data words left or right by 1 bit in the register file. However, it does not have to operate in both modes SIMULTANEOUSLY. Use these control signals: *SHL* (shift left within a word), *COMPLEMENT* (complement a word), and *PHI* (the clock signal – the cell should load the master when *PHI* is high). Generate a logic schematic for this cell using the Cadence tools.

2. n-p **Dynamic CMOS Layout with Abutment Constraints.** Draw a layout for the two-dimensional shifter cell that you designed using the **Virtuoso** layout editor. The cell must have a regular geometric form so that it can be replicated horizontally and vertically to form a regular array of cells. Use CMOS domino logic with alternating n and p logic blocks and two-phase clocking. Also, use **Schematic Composer** to produce a switch-level schematic. Design the cell so that that all input control signals are stable during $\phi = 1$ (the evaluation phase for the n blocks). $\phi = 0$ is the precharging phase for the n blocks. $\overline{\phi} = 1$ is the precharing phase for the p blocks, and $\overline{\phi} = 0$ is the evaluation phase for the p blocks. You are to create a two-stage design with the first stage realized by an n block and the second by a p block. You must also use a C-switch on the output of the p block to hold the latch contents when both the p and n stages are precharging. Otherwise, your cell will forget the current memory contents. The cell must have a regular geometric form so that it can be replicated horizontally and vertically to form a regular array of cells. Wiring must be by abutment. The way to do this is to find those strongly-connected transistors in the cell using your transistor level schematic, and then draw the sticks so that strongly-connected transistors are placed next to each other. You need draw only one copy of the sticks diagram cell. It must be possible to wire an arbitrarily large, two-dimensional array of cells by abutment. Please note that the layout area is determined by the interconnections of

this design, so please lay out the interconnections FIRST and then place transistors AFTERWARDS where you need them.