RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
16:332:574 Computer-Aided Digital VLSI Design
Assignment IV
Assigned: November 9, 2005
Due November 16, 2005

Reading Assignment: Chapters 4, 5, and Section 6.2 of Weste and Harris.
No collaboration is permitted on this assignment. Your work must be your own.

1. (**Circuit Extraction of Equivalent Resistances and Capacitances.**) Consider the following layout for a bus driver, the long interconnect, and the two p-channel transistors that represent the load on the bus in Figure 1. Use Table 4.7 in the text to calculate these values. You need $t_{ox} = 40 Angstroms$ for the TSMC 0.18 μm process in order to use these tables. Assume that each contact resistance is 20.0Ω for metal1-poly, 20.0Ω for metal1- p-diffusion, and 20.0Ω for metal1- n-diffusion and use Table 1 and Table 4.9 in Weste and Harris to calculate your wire resistances and drain capacitances. Approximate fringing capacitance by simply doubling the wiring capacitance (however, note that this approximation is increasingly incorrect as we scale down). Based on the formulae given in lecture and in Weste and Eshraghian, calculate the following values for this circuit net (assuming $\lambda = 0.09\mu m$):

Table 1: Typical Sheet Resistances for Conductors in 0.18 μm Process

Material	R_s (Ω/Square)
Metal1	0.08
Polysilicon	10.0
Diffusion (n+)	10.0
Diffusion (p+)	10.0

   (a) C_L, the load capacitance (view the gates of the driven inverters as capacitors). Calculate exact geometric areas for all wiring components of C_L and use the appropriate coefficients below to find all component capacitances. You need not apply all of the rules in the book for unusual shapes. Just break the layout into rectangles and calculate load capacitance based on rectangles.

   (b) The output rise time t_r for the bus driver.

   (c) The output fall time t_f for the bus driver.

   (d) The maximum propagation delay through the interconnect wiring from the driver to the load furthest away.

(e) Adjust this propagation delay to account for capacitive fringing field effects.

(f) The τ_{av} average gate delay for the bus driver.

(g) The total propagation delay (gate delay + propagation delay through the wire).

Show all calculations in detail in order to receive the maximum partial credit. Also, please note that you must allow for the different possibilities of transistors being on in the driving logic gate. In order to receive maximum credit for this problem, you must show all of your work. Use a ruler to measure the layout or edit the layout for cell *homework4assignment04* in Cadence library */caip/u3/bushnell/tryme* using *layoutPlus* and use electronic rulers to measure this layout. The people who get high grades on this assignment are the ones who are fairly careful about modeling parasitics in the layout.

2. (**Reduction of CMOS Propagation Delay in Long Buses.**) Consider again the prior problem. Answer the following questions about the circuit:

   (a) Will it speed up the circuit to break the wire into two lengths and use a buffer (consisting of two cascaded inverters) in between the two lengths? In order to determine the answer, you must assume minimal wiring distance between the two static inverters making up the buffer. Also, you must recalculate all wiring delays for the first wire segment and the second wire segment. If it pays to break the wire into two lengths, how much shorter will the new propagation delay be? Do not forget to include the effect of the new buffer.

   (b) Would it be even better to break the wire into three lengths?

3. (**Static CMOS Decoder Design.**) Design a logic schematic, a transistor schematic, a sticks diagram, and a circuit layout (using the rules established in Assignment III) for a three-input, eight-output decoder. Use only CMOS transmission gates, pass transistors, and inverters. Important hint: Use a regular gate matrix layout style for this design. Use p-channel MOSFET's to realize the conditions for decoding each output (pulling it to logic 1) when it is selected. Use a weak n-channel MOSFET transistor on each output to pull it down to logic 0 when it is not being decoded. Turn in the following items: a logic schematic (generated by **Cadence**), logic simulation results for all possible input combinations (generated by **Cadence**), a transistor schematic (generated by **Cadence**), switch level simulation results for all possible input combinations (generated by **Spectre**), a layout (generated by **Cadence**), and analog simulation results for the layout (generated by **Spectre**). Submission of the sticks diagram is optional but the sticks are very helpful for this problem.

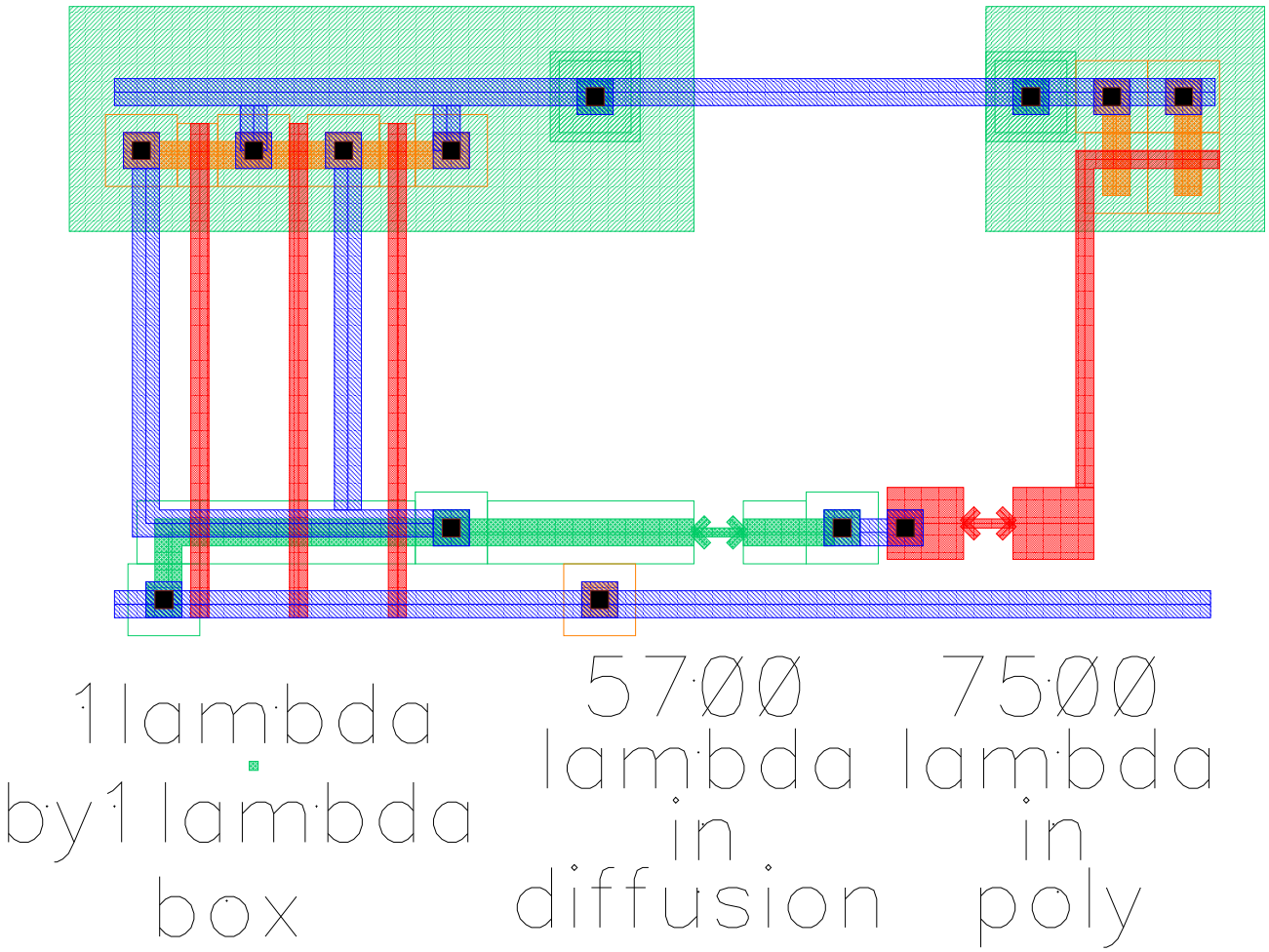

Figure 1: Layout for Circuit Extraction