Elective II: VLSI Design

Code: CISM 402

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Courtsey for slides: Debasis Mitra, NIT Durgapur

Exam Schedule

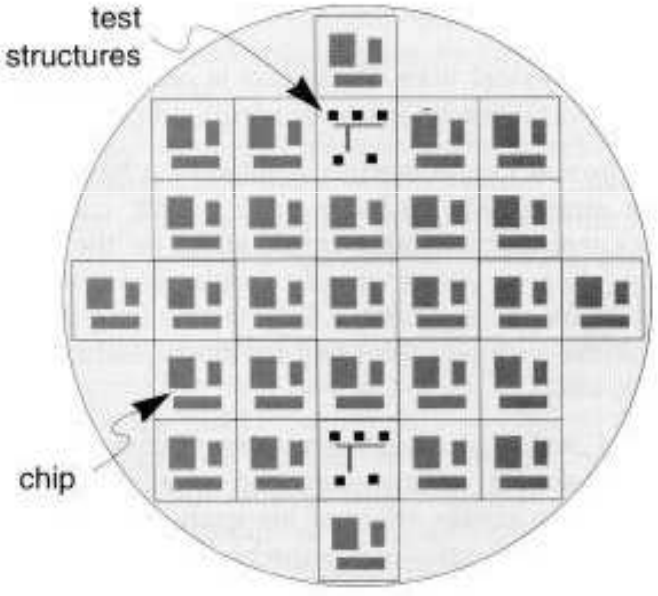
- **Mid-Sem Exam: 30 marks**
  - Tentative schedule:
    - 25/04/2011 - 30/04/2011
  - Syllabus:
    - Topics covered 1 week before the date of exam
- **Class assignments : 30 marks**
  - All assignments for a week should be submitted on the last working day of the next week

Resources

- Books:
  - Naveed A. Sherwani, *Algorithms for VLSI Physical Design Automation*, Kluwer Academic Publishers
  - M. Sarafzadeh and C. K. Wong, *An introduction to VLSI Physical Design*, The McGraw Hill Companies, Inc.
  - S. M. Sait and H. Youssef, *VLSI Physical Design Automation: Theory and Practice*, World Scientific
  - S. K. Lim, *Practical Problems in VLSI Physical Design Automation*, Springer
  - Neil H.E. Weste and Kamran Eshraghian, *Principles of CMOS VLSI DESIGN – A Systems Perspective*, Second edition, Addison Wesley, Chapter 1.

Introduction

- Study of theory and methodologies for designing a chip



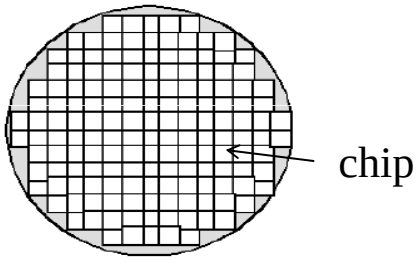
Introduction

- Study of theory and methodologies for designing a chip
- Objective: packing more and more logic devices into smaller and smaller areas
- VLSI : Very Large Scale Integration *of transistors in an IC (Integrated circuit)*
- VLSI CAD (*Computer Aided Design)*: study of algorithms and tools for aiding VLSI design
- ASIC : Application Specific IC

Terminologies

- IC : combination of inter connected circuit element within a substrate
- Substrate: semiconductor material on which chip is fabricated
- Wafer: 10 cm (diameter)

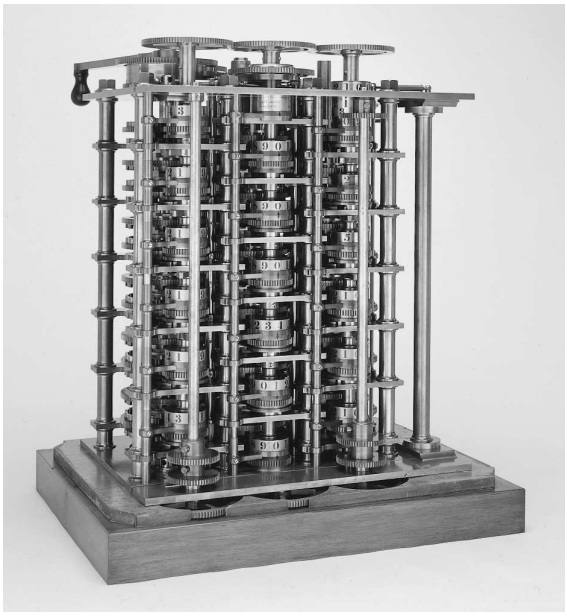
  12 to 30 chips



- Feature size: minimum gate length of a transistor : 0.18µ
- Fabrication process : 0.18µ process, 200mm wafer

Evolution of Computer

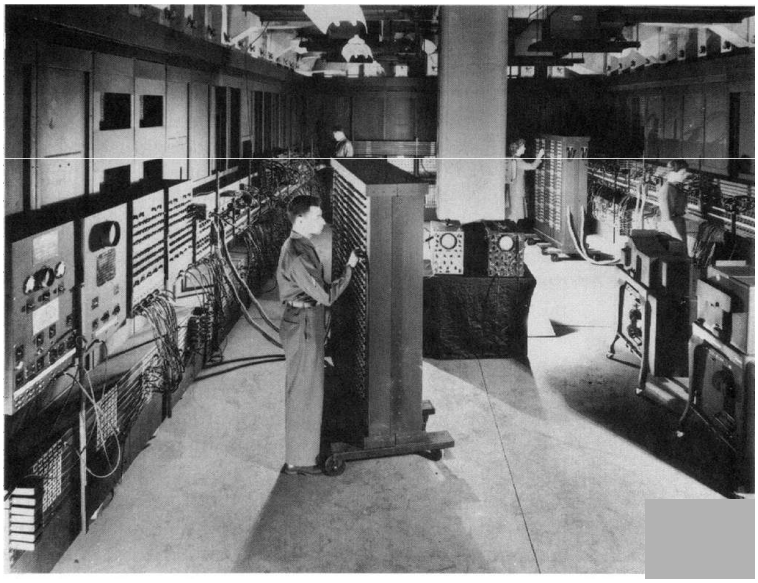
Babbage Difference Engine : First Computer (1832)



25000 parts

Evolution of Computer

ENIAC : The First Electronic Computer (1943-1946)



Length = 80 ft

Height =8.5 ft

Floor area = 1500 sq ft

Weight = 30 tons

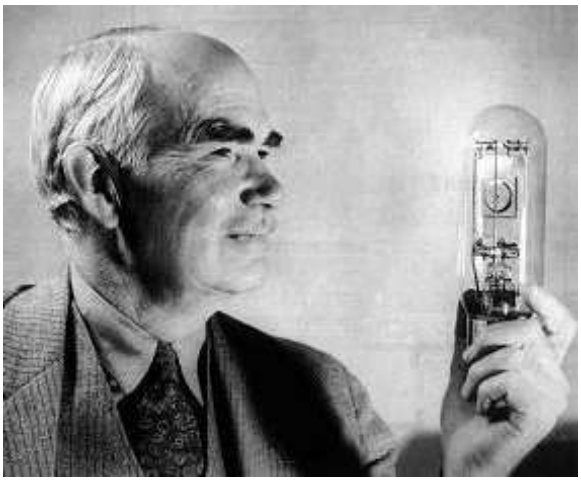
18000 vacuum tubes

70,000 resistors

140 kw of power

Evolution of Computer

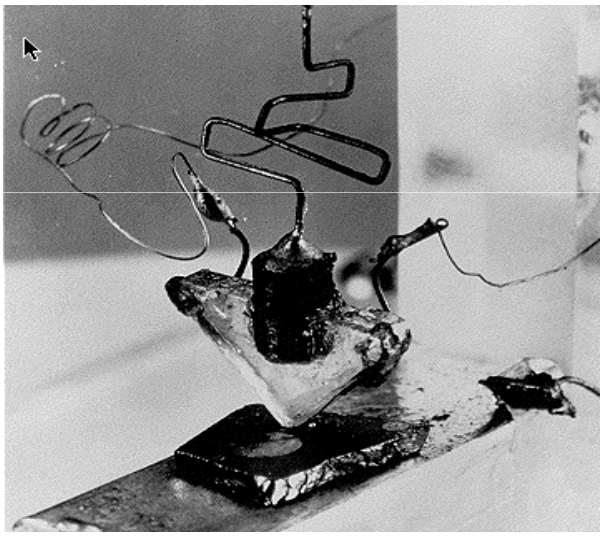
ENIAC : The First Electronic Computer (1943-1946)



Audion (Triode), 1906, Lee De Forest

Foundation of IC Industry

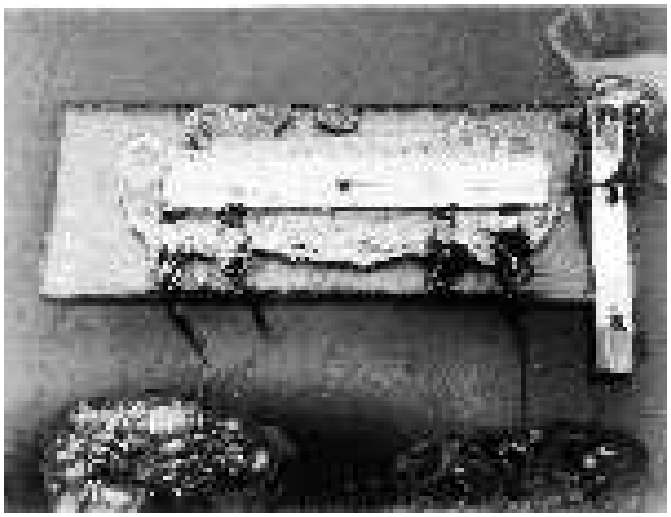
First transistor (germanium), 1947



John Bardeen and Walter Brattain, Bell Laboratories

Foundation of IC Industry

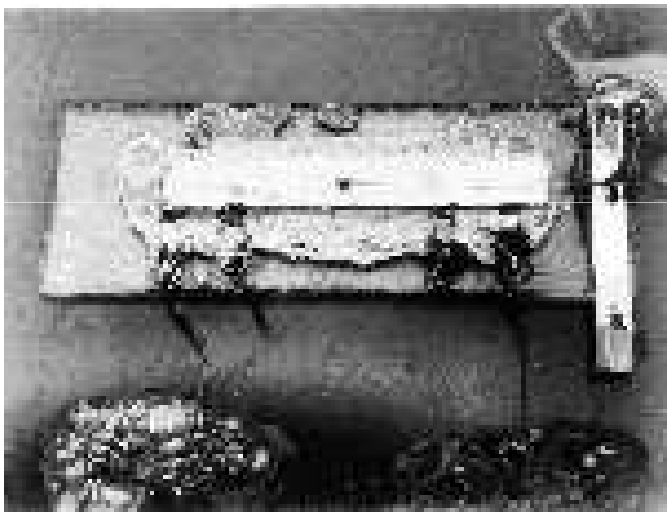
First integrated circuit (germanium), 1958



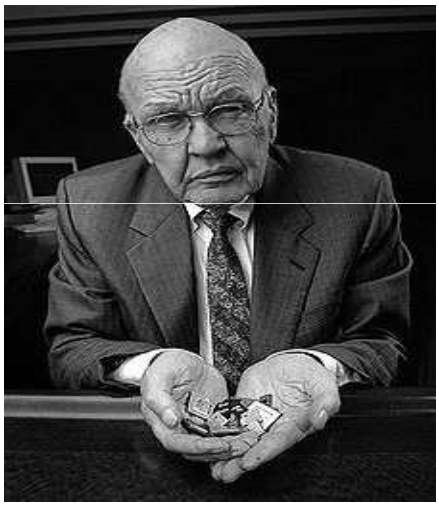
Jack S. Kilby, Texas Instruments

Foundation of IC Industry

First integrated circuit (germanium), 1958



Jack S. Kilby, Texas Instruments

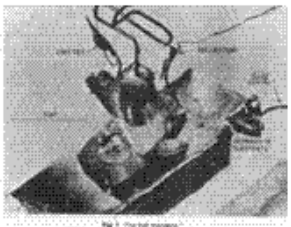


Jack S. Kilby (1923 - 2005)

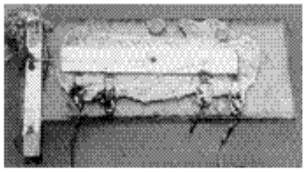
Better late than never : Awarded Nobel prize in Physics in 2000

Milestones of IC Industry

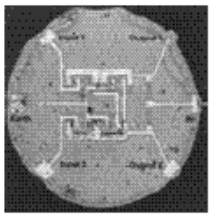
- **1947:** Bardeen, Brattain & Shockly invented the transistor, foundation of the IC industry.
- **1952:** SONY introduced the first transistor-based radio.
- **1958:** Kilby invented integrated circuits (ICs).
- **1965:** Moore's law.
- **1968:** Noyce and Moore founded Intel.
- **1970:** Intel introduced 1 K DRAM.



First transistor



First IC by Kilby

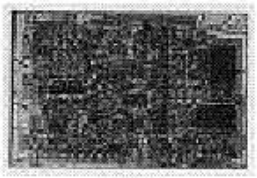


First IC by Noyce

Milestones of IC Industry

- **1971:** Intel announced 4-bit 4004 microprocessors (2250 transistors).
- **1976/81:** Apple II/IBM PC.
- **1985:** Intel began focusing on microprocessor products.
- **1987:** TSMC was founded (fabless IC design).
- **1991:** ARM introduced its first embeddable RISC IP core (chipless IC design).

Intel founders



4004

IBM PC

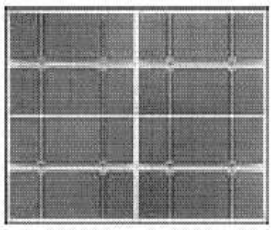
tsmc

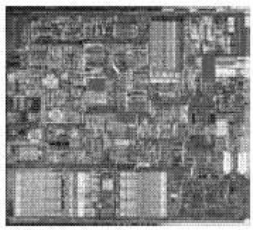
ARM

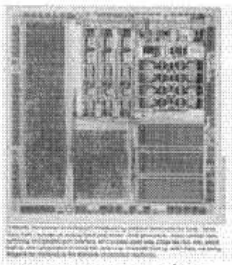
Advanced RISC Machines

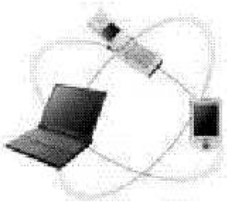
Milestones of IC Industry

- **1996:** Samsung introduced IG DRAM.
- **1998:** IBM announces1GHz experimental microprocessor.
- **1999/earlier: System-on-Chip (SOC)** methodology applications.
- An Intel P4 processor contains 42 million transistors (1 billion by 2005)
- Today, we produce > 30 million transistors per person (1 billion/person by 2008).
- **Semiconductor/IC:** #1 key field for advancing into 2000 (*Business Week*, Jan. 1995).


4GB DRAM (2001)


Pentium 4

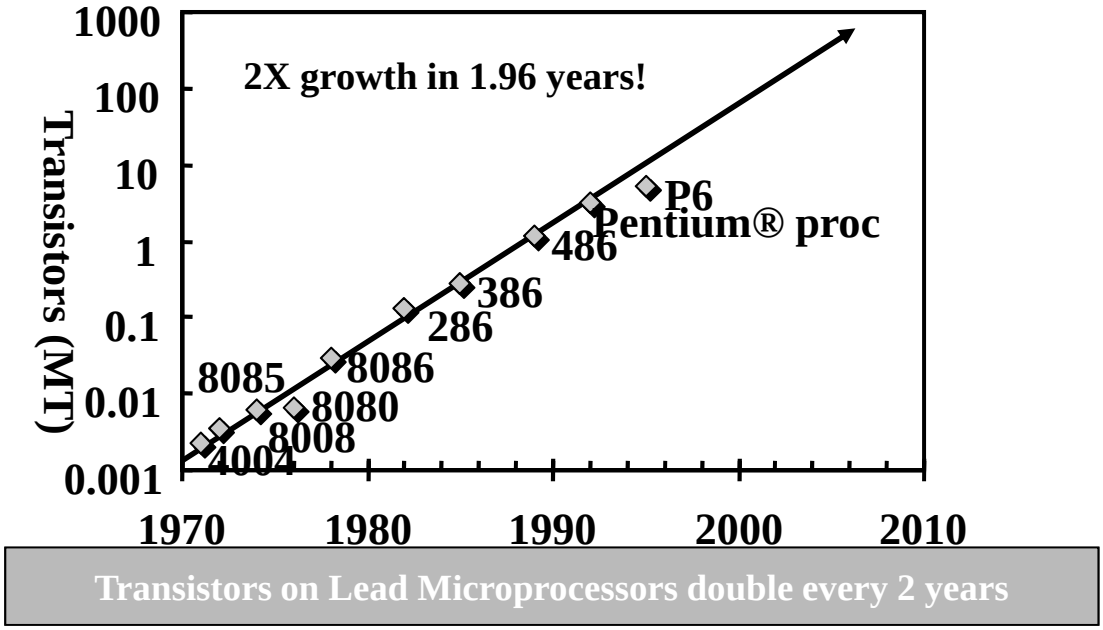

Scanner-on-chip


Blue tooth technology

Gordon Moore: 1965

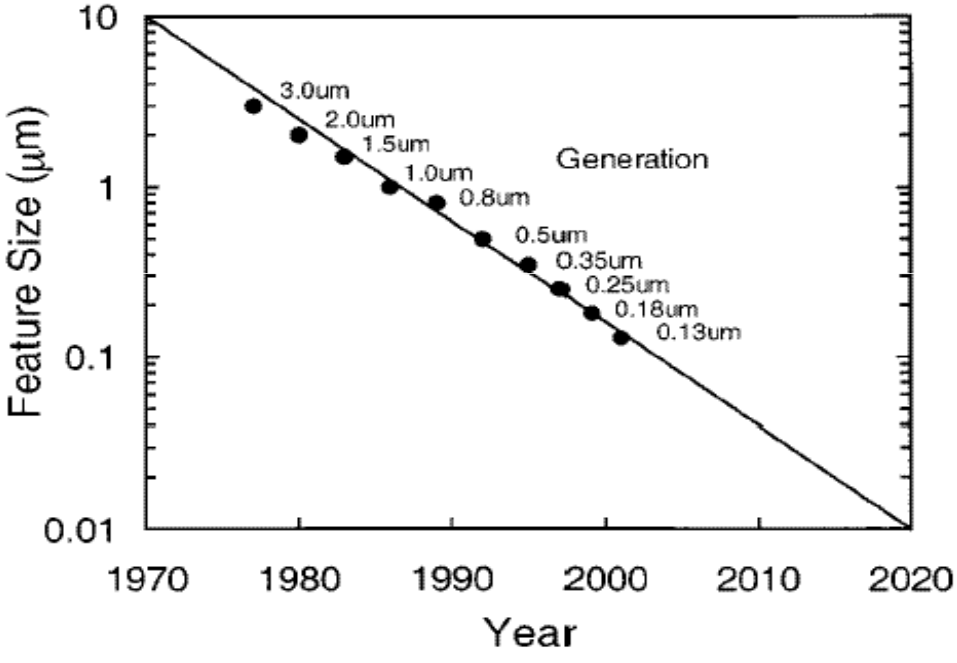
- Predicted that the number of transistors integrated on a die would grow exponentially (doubling every 12 to 18 months)
- Million transistors/chip barrier crossed in the 1980s
  - 42 Million, 2 GHz clock, 0.18 m m CMOS technology (Intel P4) - 2001
  - 140 Million transistor (HP PA-8500)

Moore's law in Microprocessors



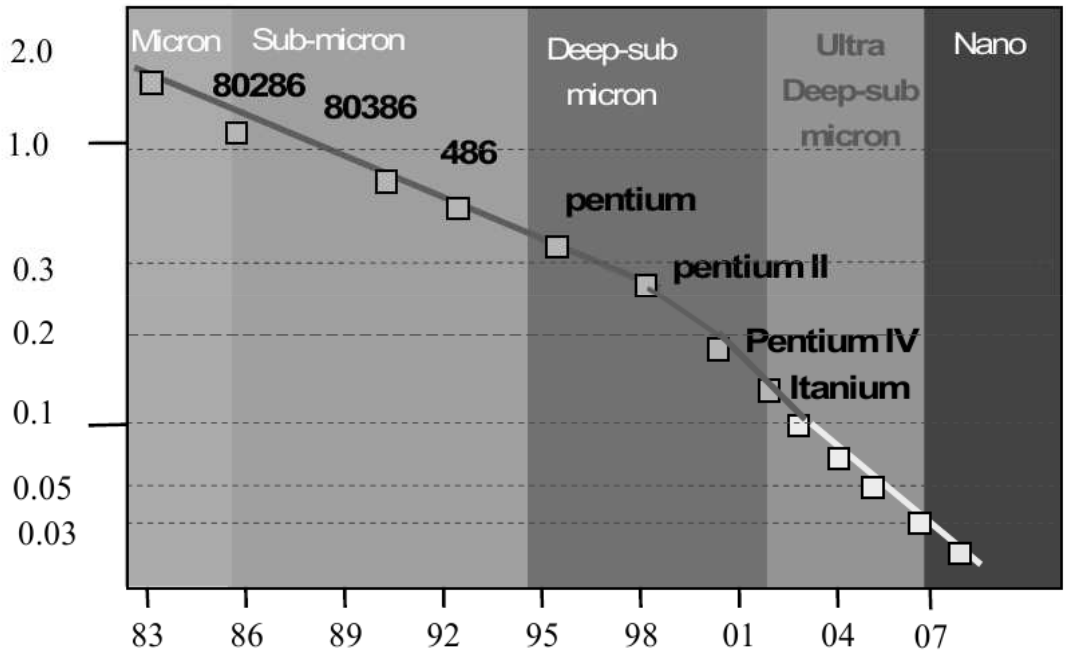
Courtesy, Intel

Semiconductor Technology Minimum Feature Size



Courtesy: Intel

How small are transistors

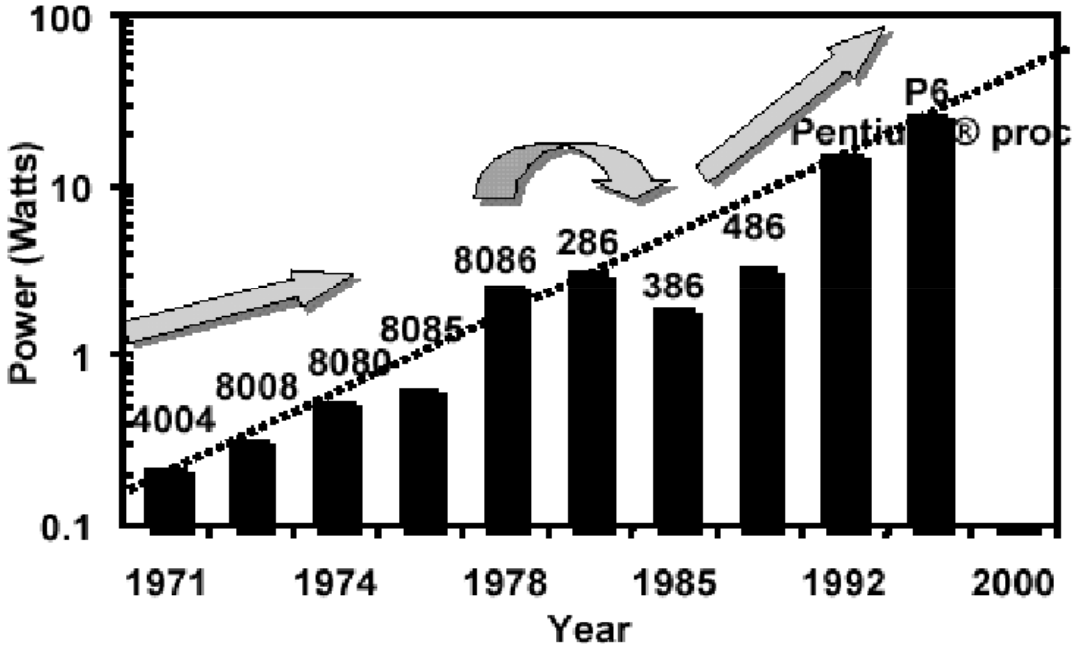


Courtesy: Intel

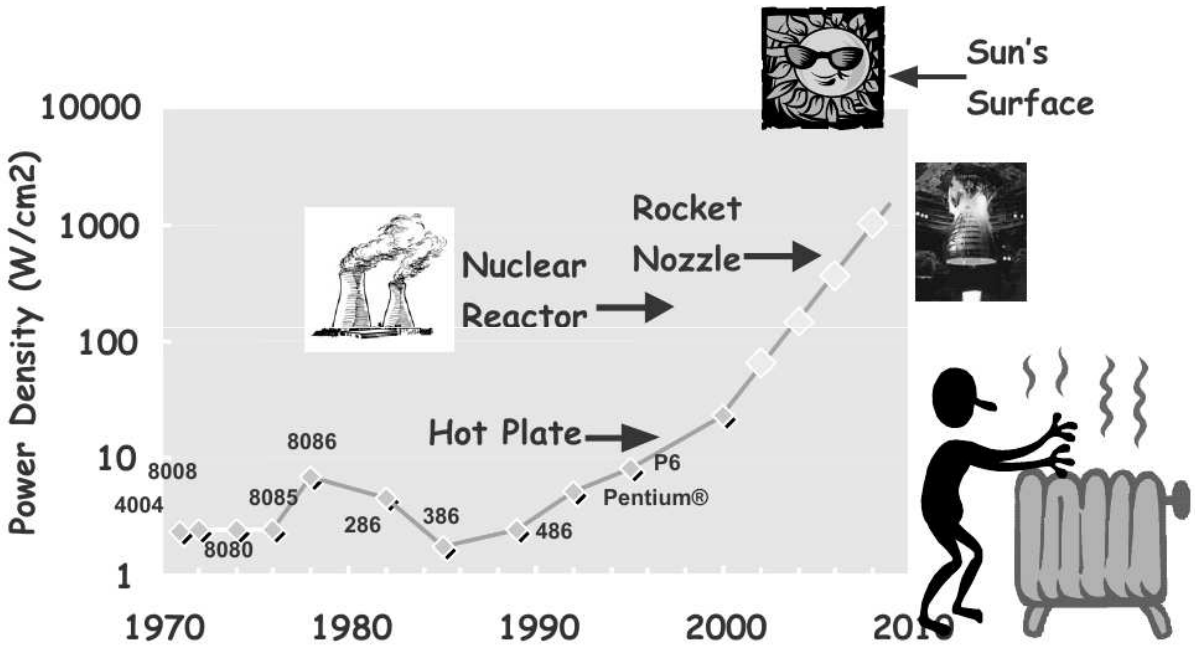
History of IC (Integrated Chip)

Year	Technology	# of transistors	Products
1947	Invention of transistor	1	-
1950	discrete components	1	Junction transistor, Diode
1961	SSI	10	logic gate, flip-flops
1966	MSI	10^2- 10^3	counters, mux, adders
1971	LSI	10^3- 20×10^3	8088, RAM, ROM
1980	VLSI	20×10^3 - 10^6	16/32 μprocessor, DRAM
1990	ULSI	10^6 - 6×10^6	ASIC
2000	GSI	$10 - 20 \times 10^6$	DSP
2010	nano meter	$5 - 10 \times 10^9$	System-on chip

Processor Power trends



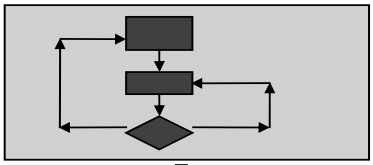
Processor Power density increase



VLSI Design Cycle

System specifications

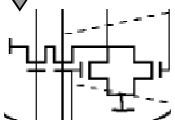
Functional design (o/p:timing diagram , relationship between blocks/subblocks)



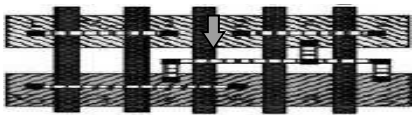
Logic design/RTL(o/p : RTL and boolean expn)

F = (AB + C) *(D+E(X+Y)),
G = XY + AD

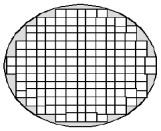
Circuit design (o/p: CMOS transistor, R, C)



Physical design
(deals with geometric structures)



Design Verifivation
(deals with DRC and Circuit Extraction)



DIP (Dual Inline Package)
PGA (Pin Grid Array)

Fabrication ,Packaging, Testing, Debugging
(die/ chip on wafer)

ATPG

VLSI Design Cycle

System specifications

Functional design (High level language)

High level Synthesis

Logic design / RTL (Hardware Description Language VHDL/Verilog)

Logic Synthesis

Circuit design

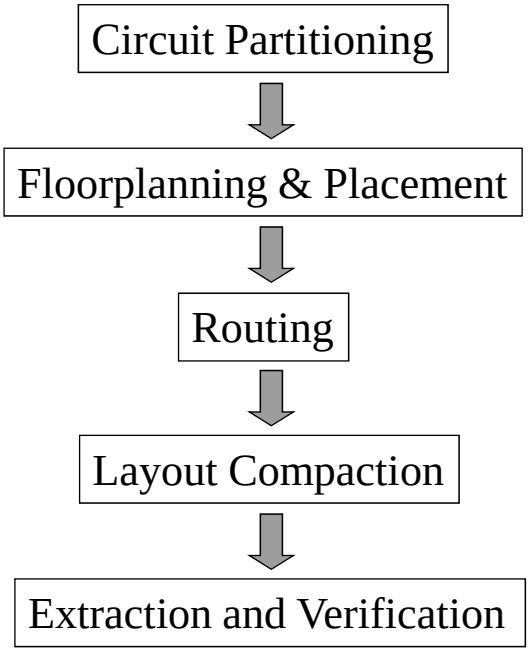
Physical design (netlist of components)

Physical Synthesis (Floorplaning , Place and Route)

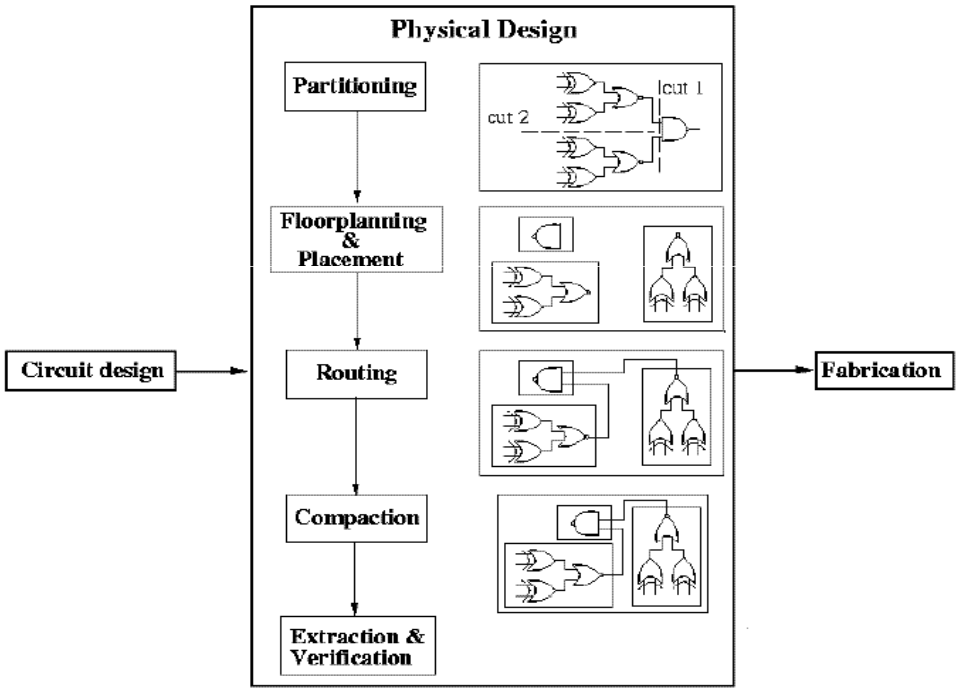
Fabrication and Packaging

Testing

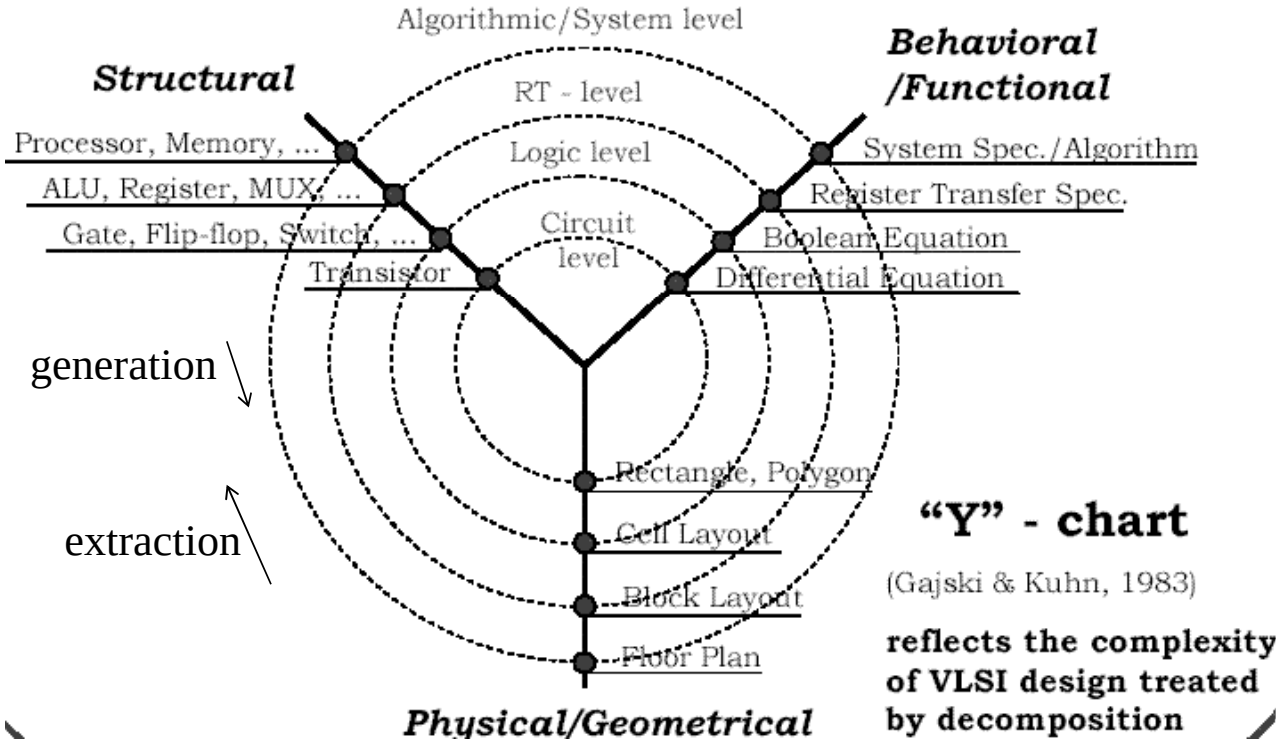
Physical Design Flow



Physical Design Flow



Different Design Views

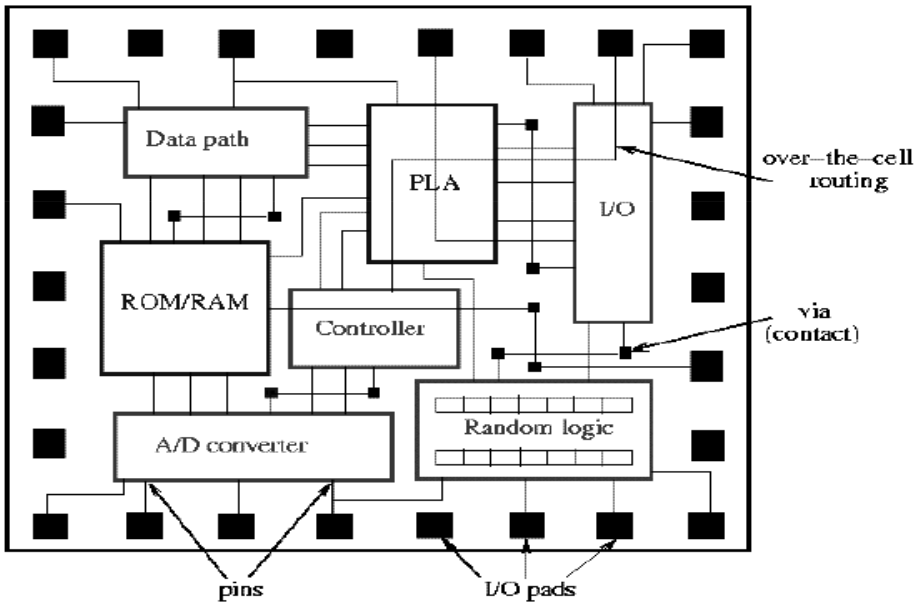


Design Styles

- Full-Custom Design
- Standard Cell
- Gate Array
- FPGA
- System-on-Chip (SOC)

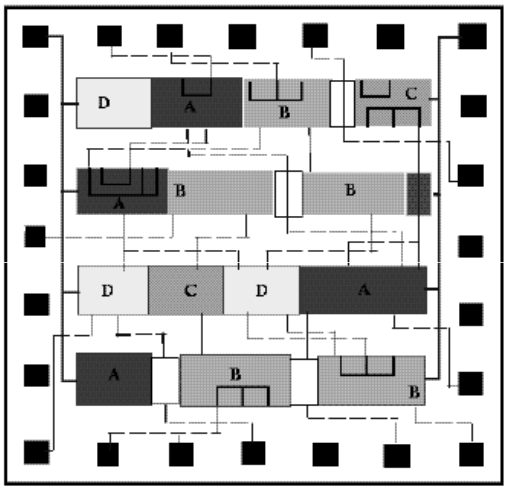
Full Custom Design Style

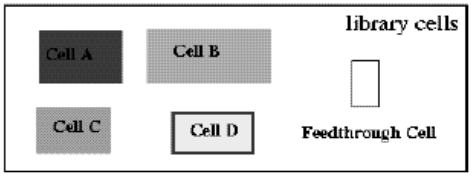
- Designers can control the shape of all mask patterns.
- Designers can specify the design up to the level of individual transistors.



Standard Cell Design Style

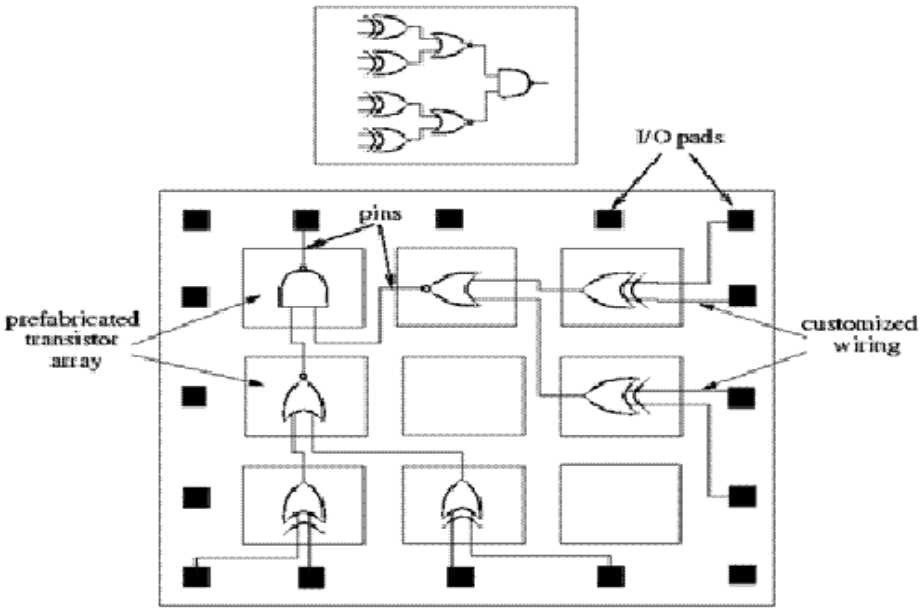
- Selects pre-designed cells (of same height) to implement logic





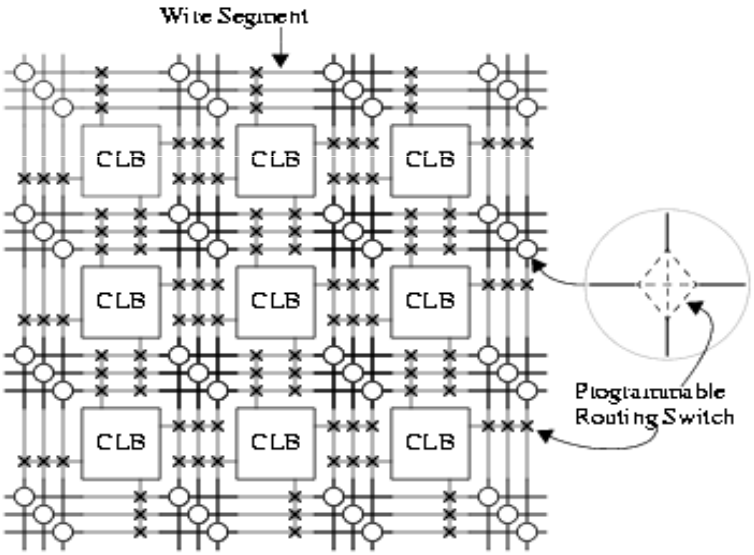
Gate Array Design Style

- Prefabricates a transistor array
- Needs wiring customization to implement logic

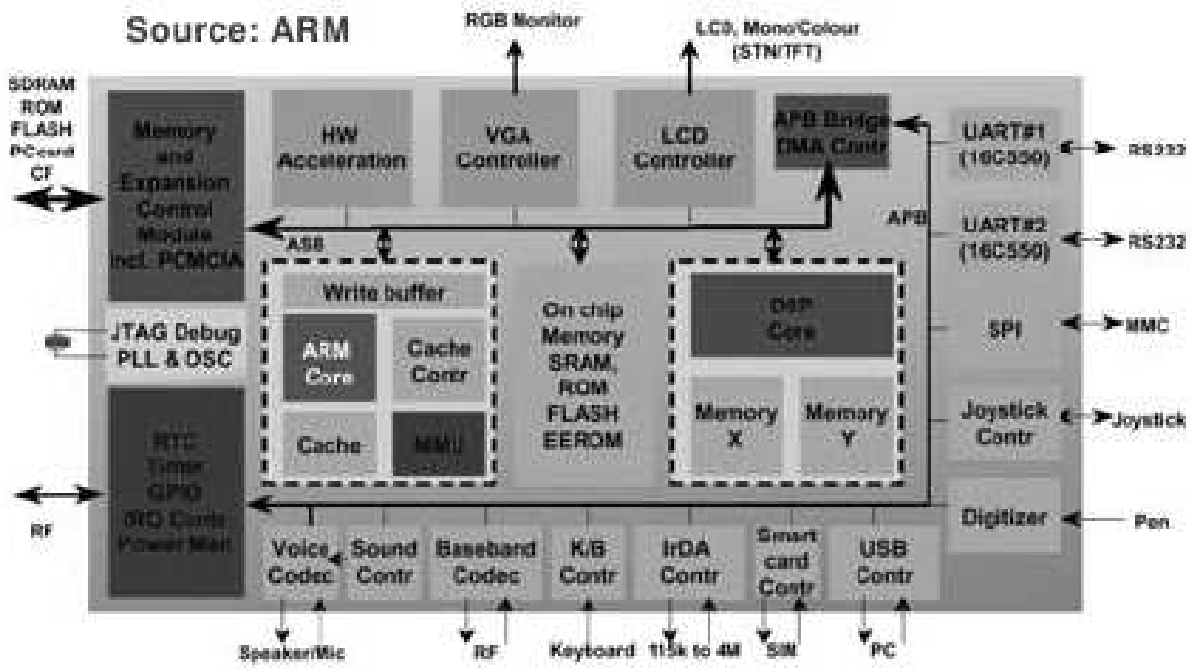


FPGA Design Style

Logic and interconnects both prefabricated



System on chip



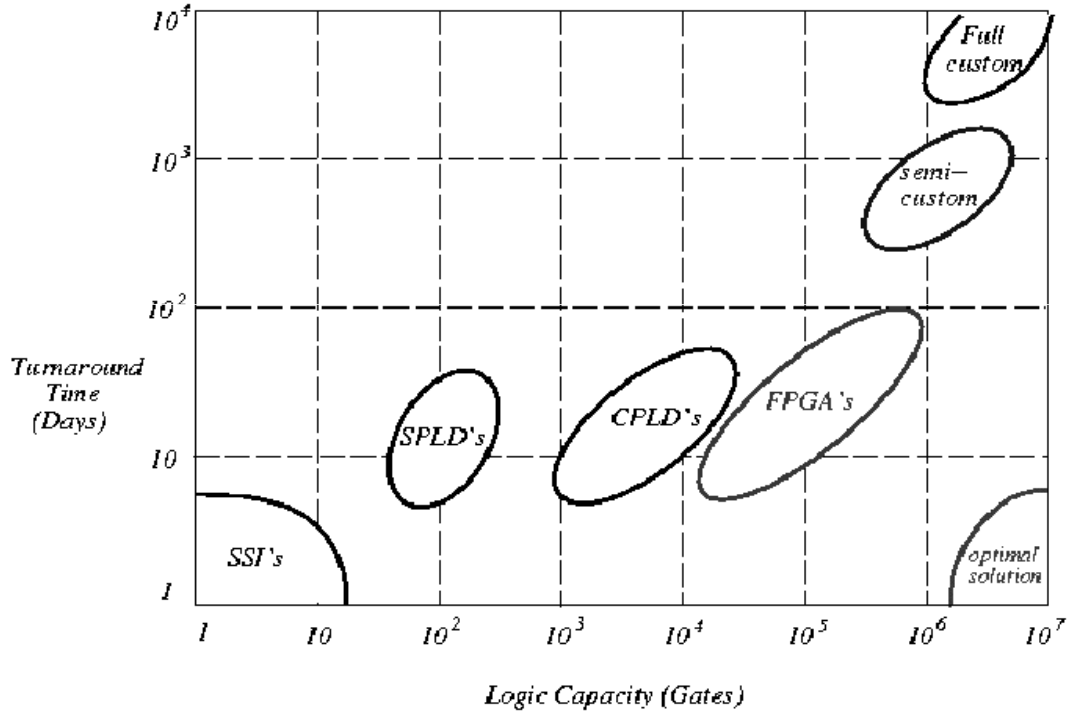
Comparison of Design Styles

	Full-Custom	Standard Cell	Gate Array	FPGA
Cell size	variable	fixed height	fixed	fixed
Cell type	variable	variable	fixed	program-mable
Cell placement	variable	in row	fixed	fixed
Inter-connections	variable	variable	variable	program-mable
Fabrication layers	all layers	all layers	routing layers only	no layer
Area	compact	compact to moderate	moderate	large

Comparison of Design Styles

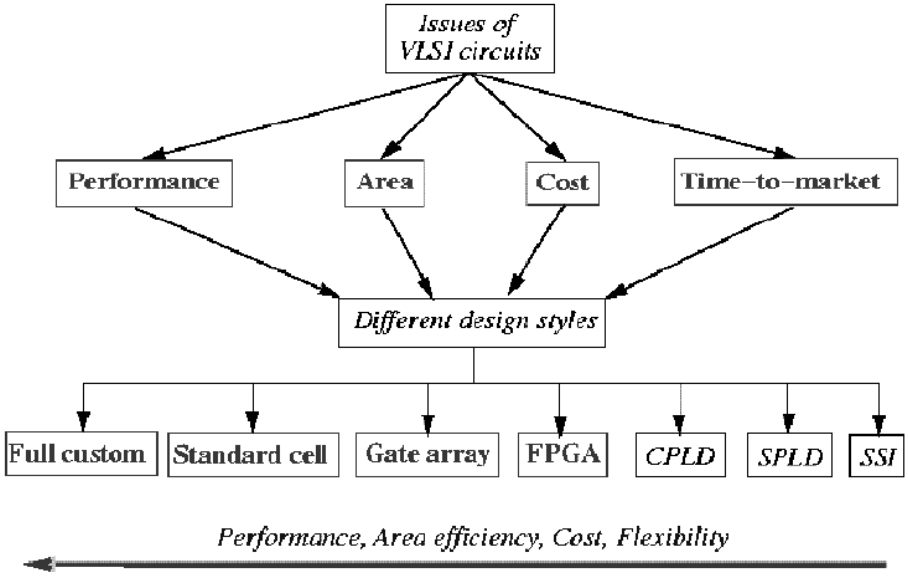
	Full-Custom	Standard Cell	Gate Array	FPGA
Performance	high	high to moderate	moderate	low
Design cost	high	medium	medium	low
Time-to-market	long	medium	medium	short

Design Style Trade-offs



Comparison of Design Styles

- Specific design styles shall require specific CAD tools



VLSI Physical Design Automation

Objective:

- study of algorithms and data structures related to physical design process
- Optimal arrangement of devices on plane & Efficient interconnection scheme
  - Performance of chip
  - Size of chip
  - Power
- Develop time efficient CAD tool

How to solve ?

Type of objects: geometric objects- line, rectangles

Algorithms: graph theoretic, combinatorial optimization,

- Constraints are problem dependent (electrical requirement)

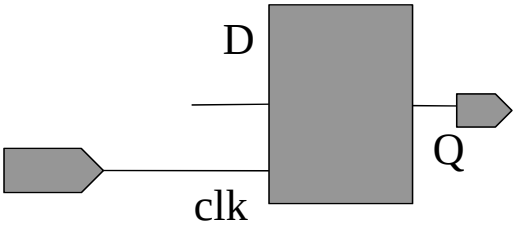
Design Entry for IC design

- **Register transfer level** (**RTL**) is a level of abstraction to describe operation of a synchronous digital circuit.
  - flow of signals (or transfer of data) between hardware registers,
  - logical operations performed on those signals.
- Hardware Description Languages (HDLs) : Verilog and VHDL
  - create high-level representations of a circuit,
  - lower-level representations and ultimately actual wiring can be derived.

VHDL

Very High Speed Integrated Circuit H/W Description Language

```
entity ff is
   Port ( D : in  STD_LOGIC;
          Q : out STD_LOGIC;
            clk : in STD_LOGIC);
end ff;
```




```
architecture Behavioral of ff is
Begin
process(clk)
begin
    if clk'event and clk ='1' then
     Q <= D;
    end if;
end process;
end Behavioral;
```