RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
16:332:574 CAD Digital VLSI Design
Assignment VII
Assigned: December 5, 2005
Due December 12, 2005

Reading Assignment: Read the Cadence tools operation manual for Silicon Ensemble and attend the Silicon Ensemble tutorial.

No collaboration is permitted on this assignment. Your work must be your own.

1. (**Standard Cell Place-and-Route for an ALU.**) Design a layout implementing an 8-bit ALU with ripple carries using standard Cell place-and-route. The ALU has two control bits, $SEL[0:1]$, and pattern 00 causes it to ADD the A bus to the B bus, producing an 16-bit result on the C bus. Pattern 01 instead computes $C \leftarrow A - B$, pattern 10 computes $C \leftarrow A \times B$, and pattern 11 is a NOP, which leaves C in the high impedance state. The ALU is combinational hardware, and produces a 1 on the C_OUT bit if an operation is done and produces a carry or borrow out. If $C == 0$ when an operation is done, the ALU produces $ZERO \leftarrow 1$, otherwise $ZERO \leftarrow 0$. The ALU takes a C_IN bit as an input carry or borrow into the least significant bit position. The A and B busses are 8 bits, but the C bus is 16 bits to allow full representation of the product from a multiplication.

   Describe this circuit using the *Verilog* hardware description language, do a logic simulation of the description using *Verilog-XL*, automatically create a layout for the module using Cadence *Silicon Ensemble*, extract the equivalent circuit from the layout, and produce a *Spectre* analog simulation of the layout. This homework assignment will teach you how to quickly and automatically generate a chip layout from Verilog. Use the TSMC 0.25 μm process for this assignment, because that is the process that has the standard cell place-and-route library available.