RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
16:332:574 CAD Digital VLSI Design
Assignment VII
Assigned: December 1, 2004
Due December 8, 2004

Reading Assignment: Read the Cadence tools operation manual for Silicon Ensemble.
No collaboration is permitted on this assignment. Your work must be your own.

1. (**Standard Cell Place and Route for Parallel Multiplier.**) Design a layout implementing a 4-bit by 4-bit parallel multipler using ripple caries. Describe this circuit using the *Verilog* hardware description language, do a logic simulation of the description using *Verilog-XL*, automatically create a layout for the module using Cadence *Silicon Ensemble*, extract the equivalent circuit from the layout, and produce a *Spectre* analog simulation of the layout. I am organizing a tutorial on Silicon Ensemble for Friday night. This homework assignment will teach you how to quickly and automatically generate a chip layout from Verilog. Use the TSMC 0.25 μm process for this assignment, because that is the process that has the standard cell place-and-route library available.