RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
332:473 Introduction to VLSI Design
Projects
Jan. 21, 2004

As you are all aware, there is both a short project and a final project for this course. The short project should be sub-component of the final project. Hopefully, Assignments I through VII and the midterm will adequately prepare you to do these projects. The purpose of this handout is to describe what I expect from you and your project, and to give some ideas about what the project might be.

Your first job is to create a small project. This should have, **AT MOST**, 15 to 30 transistors and should represent a well-defined sub-unit of your large project integrated circuit. The short project is due shortly after the midterm. You are to design the schematic using CMOS logic gates and transistors, and lay out the device with Cadence. You must also analyze the timing requirements of all long wires and all gates that drive more than one fanout using Cadence. You must remove redundant logic and generate test-patterns using the **EST** and **SEST** CAD tools. The short project is due on April 12, 2004.

The course requires a long project, which is a major component of your course grade. Your first job is to concoct a project idea. You may work alone or with, at most, one other person. However, if you submit a multi-person project, you must clearly identify which part of the project is your contribution, and you will be evaluated solely on the quality of YOUR contribution. Groups of more than two people are strongly discouraged. On February 18th, you should turn in a one-page description of your project idea. Be precise and concise. Please include a rough estimate of the size (in λ^2) and number of package pins required for your chip. The undergraduate student IC fabrication process is a 0.5 μm AMI process, and you are allowed a maximum chip area of 1.5 $mm \times 1.5$ mm. A typical chip pad frame has 40 pins, and six are reserved for V_{DD} and GND. This leaves 34 pins for inputs, outputs, and test points. However, additional pins may be allowed for undergraduate projects. If your design needs to use more pins than that, then you must see Dr. Bushnell for approval. However, your area and dimensions must remain below the maximum limit. The design should contain between two and five thousand transistors. The actual size will be difficult to estimate. The complexity of the design is more important than the number of transistors. If you want to do a really complex design, such as an ALU, first design a four-bit ALU and extend the design to more bits if time and space permit. I will require a single directory containing your design at the end of the semester. I will review your proposal to make sure you are not attempting too ambitious or too small a project. Feel free to include any diagrams you think will help explain your idea. Also, feel free to discuss your ideas with me. Graduate students are expected to do an ambitious and first-rate large project, meaning that all synthesis and analysis aspects of the chip must be performed, and the work must be correct. Undergraduates need not create a really ambitious project to get an **A** in this course – you only need to do a good job on a moderate-sized design. If you really want to create a larger chip, that is also possible, but then you must do the project with a partner. However, you will then have to explain to me how you expect to get the design finished in the time allowed.

Design Activity	Due Date	Penalty
Project Conceived and One Page Description Handed In	2/11/04	– 1/2 Letter Grade on Project
One-Two Page Status Report	2/16/04	– 1/2 Letter Grade on Project
VHDL Descriptions of Logic (if Synopsys synthesized logic) where appropriate	2/23/04	– 1/2 Letter Grade on Project
Logic Schematics from Cadence and Logic Simulation Results	3/8/04	– 1/2 Letter Grade on Project
SEST and EST Redundant Logic Removal Commentary where appropriate	3/15/04	NONE
Transistor Schematics from Cadence and Switch-Level Simulation Results (where appropriate)	3/22/04	– 1/2 Letter Grade on Project
Hand Drawn Chip Floor Plan	3/22/04	– 1/2 Letter Grade on Project
Short Project Due	4/12/04	– 1/2 Letter Grade on Project
All Leaf Cell Layouts (laser printer plots o.k.) and Spectre timing simulations	4/14/04	– 1/2 Letter Grade on Project
Final Chip Floor Planning, Global Routing, and Detailed Routing	4/21/04	– 1/2 Letter Grade on Project
Chip Interconnect Critical Path Timing Analysis and Maximum Clock Frequency Derivation	4/26/04	NONE
Final Chip Project Presentations	5/3/04	
Final Test-Patterns Generated Automatically by EST and SEST	5/3/04	NONE
Final electronic layout for Pattern Generation Tape with Overglassing and all Notches Filled	5/14/04	NONE
Final Project Report Due	5/14/04	NONE

With your one or two page status report for your full project on 2/16/04, include with it logic or VHDL cell descriptions or logic schematics of circuits you have already designed. Statements like, “We designed a static register cell, but then discovered that it was not static ... redesigning it.” are just fine, and are encouraged. Also, on 5/3/04, you should be prepared to give a fifteen minute oral presentation of your chip, complete with viewgraphs.

You must turn in a final report on or before 5/14/04. The final report MUST include:

- An overall description of the project, its organization, and how it works.
- A floor plan of the chip, with pads clearly labeled as to function (signal name).
- A check plot of the project, with as much annotation as necessary to understand it. The best scheme would be plots of the individual cells together with descriptions of how they work; then, include plots of larger assemblies, etc.

- Engineering calculations that estimate the performance of your chip. In addition, you should simulate all pieces of your design that are critical to its performance. You are not expected to simulate the entire chip. I expect to see Cadence logic simulations of all parts of the design and analog mode simulations for all critical paths in the chip.

- A complete plan for testing your chip, spelled out in detail, including test patterns. Also, you can use built-in self-testing hardware, as designed for you by the Rutgers **delaybist** CAD tool.

- A description of where the layout, GDS II, and test-pattern files reside on the Suns.

- A one or two page data book style description. The intent is that you would give this sheet of paper to someone who wants to use your chip. Look at the Texas Instruments MOS parts catalogue for an example data book description.

- A description of at most one quarter page in length explaining each unique cell that you created for your project. Each cell description must include a logic schematic, **EST** or **SEST** information indicating that no redundant logic exists, and logic simulation results from Cadence. Furthermore, you must include a layout and analog timing results from Cadence or from **SPICE**.

- A description of how useful *Cadence*, *Synopsys*, **EST**, and the other Rutgers CAD tools were to you.

- Bonding pads must be attached to the layout.

- You must calculate the current density, J, for all power and ground wires in the chip.

- You must estimate the power consumption of your chip and its clock rate.

Your design must be sent to be fabricated in order for you to receive credit for this course. Be aware that the U.S. Government has established restrictions on the area and number of pins for a design that they will fabricate, and I will explain these restrictions shortly. Chips will probably be returned by Sept. 1st, 2004.

You should use the following design tools: Cadence tools, **Spice** circuit simulator, **EST** (a combinational logic test-pattern generator), and **SEST** (a sequential logic test-pattern generator). Other Rutgers CAD tools may also be used.

Your final projects will be graded on the following criteria:

- Logical correctness (shift registers that don't shift will cost you points).

- Physical correctness (design rule violations will cost you points).

- Electrical correctness (chips that cannot achieve your specified clock rate will cost you points).

- Correct use of electrical circuit simulation tools.

- Quality of the chip documentation (if it is a mess, you will lose points).

- Completeness. If the cell layouts and global chip wiring layouts are incomplete, you will lose lots of points.

Verify logical and physical correctness as you progress in the design phase, not after the whole thing is laid out.

1 Project Ideas

Below are some project ideas. You need not choose a project from this list. It is not necessary that your project be a brand new innovation. However, I strongly encourage you to be creative. I will not accept any digital alarm clock, parallel multiplier, or analog circuit designs this year. If you want to do analog layout, there is a graduate course in spring 2005 for that. This course presents an exciting design opportunity!

I hope that your project will reflect some of the things I have been stressing in this course, such as regularity, reducing global wiring, using pass transistors, electrical correctness, etc. If you find yourself trying to translate a TTL design into MOS, you are probably on the wrong track. You should spend most of your time on creating an elegant design for your project and on verifying correct electrical operation of your chip. You should discover that elegant designs are easier to create, and have good performance as well. Here are some project ideas:

1. Design a Field-Programmable Gate Array.

2. Design some counter logic for optical encoders mounted in quadrature. This will form part of an "optical mouse" that keeps track of signals from a pair of optical sensors moving in any direction over a regular pattern of black and white stripes. The simplest design keeps track of the position down to a quarter of a cycle. A more involved design obtains velocity information by differencing.

3. Devise a way to design a Programmable Logic Array so that there is a "done" signal that indicates when signals have had sufficient time to propagate through the PLA and set the outputs properly. This requires developing a way to have a "timing model" of the PLA – as the PLA slows down or speeds up, so will the timing model. The timing model must always be conservative (i.e., always be slower than the slowest signal in the PLA).

4. Design a processing element of a Single-Instruction-Multiple-Datapath computer. Show how arithmetic will be done on such an element.

5. Design a simple bus-oriented arithmetic engine.

6. Design a memory error detector/corrector using Hamming codes.

7. Design part of a floating-point adder/multiplier. It should be able to do the appropriate pre-scaling, and probably should produce normalized results.

8. Design part of a barrel-shifter for a BitBlt (RasterOp) processor.

9. Design a systolic sorter.

10. Design a systolic pattern-matcher.

11. Design a programmable I/O controller.

12. Design an associative memory chip (either fully associative or set associative).

13. Design a FIFO chip.

14. Design a digital neural network chip with programmable weights and thresholds.

15. Design part of a data path suitable for a Digital Signal Processor.

16. Design a chip to implement part of a Discrete Cosine Transform.
17. Design part of a home automation system.
18. Design part of a trip routing system for an automobile.
19. Design part of a knock-out switch for an Asynchronous Transfer Mode (ATM) internet switch.
20. Design port of a low-power portable wireless device.

These are only suggestions, but represent some of the better VLSI designs that have been done at Carnegie Mellon, Duke, and Rutgers.