

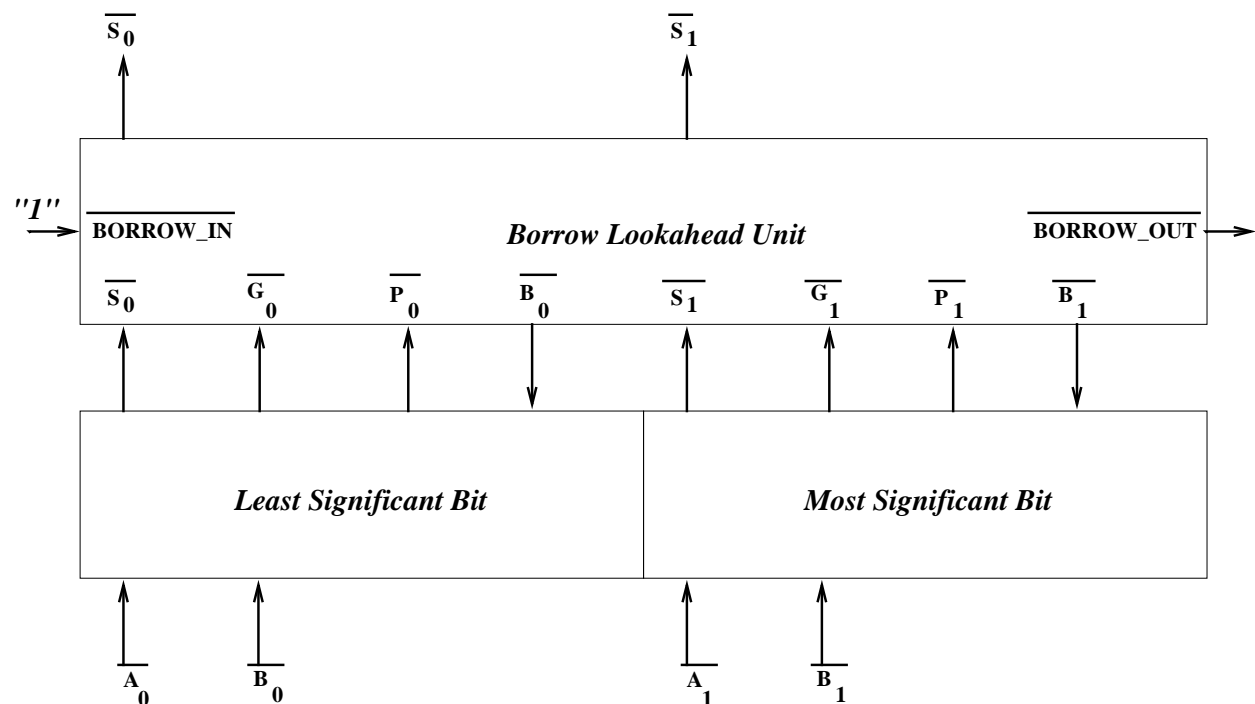
RUTGERS UNIVERSITY  
 Department of Electrical and Computer Engineering  
 16:332:574 CAD Digital VLSI Design  
 Assignment II  
 Assigned: October 5, 2005  
 Due October 12, 2005

**Reading Assignment:** Chapters 1 and 2 and Section 8.2.1.2 of Weste and Eshraghian.

No collaboration is permitted on this assignment. Your work must be your own.

Some signals in this assignment are active low (negative logic) and some are active high (positive logic).

1. (**CMOS Arithmetic Circuit Wiring by Abutment.**) You are to design a borrow-lookahead subtracter module that subtracts two input  $n$ -bit unsigned binary numbers  $\overline{A}$  and  $\overline{B}$  and a  $\overline{BORROW\_IN}$  signal and produces an output  $n$ -bit sum  $\overline{S}$ , and  $n$ -bit  $\overline{GENERATE}$  and  $\overline{PROPAGATE}$  signals.  $\overline{S} = \overline{A} - \overline{B}$ . You are to design a one-bit subtracter, and then you should replicate an array of these one-bit subtracters to realize an  $n$ -bit subtracter. Thus, we only need to do a sticks layout for one cell, as follows. Each cell has three inputs (correspond-



ing bits of  $\overline{A}$ ,  $\overline{B}$  and  $\overline{BORROW\_IN}$ ) and three outputs (a  $\overline{SUM}$  bit ( $\overline{S}$ ),  $\overline{GENERATE}$ , and  $\overline{PROPAGATE}$  signals). The cells are designed to be rectangular and designed to fit conveniently next to one another. We wire the cells by making sure that the outputs of one cell touch the inputs of the next cell, and are routed on the same wiring layer. This allows us to build a subtracter of arbitrary size (any  $n$ ) by simply juxtaposing a sufficient number of cells. You only have to design a single bit of the subtracter cell. The signals  $\overline{A}$  and  $\overline{B}$  should be on the bottom of the cell, and the output signals  $\overline{S}$ ,  $\overline{GENERATE}$ , and  $\overline{PROPAGATE}$  should be on the top of the cell. Also, the input  $\overline{BORROW\_IN}$  signal should be on the top of the cell.  $\overline{S}$  should be directly across from input  $\overline{A}$ . Turn in a logic schematic, a transistor schematic, and a sticks diagram for a single cell. Concentrate on making the cell rectangular and very compact. Don't forget to minimize your cell logic, using Karnaugh maps. For extra credit, explain what simple additions are needed to turn this subtracter circuit into a subtracter circuit.

2. (**CMOS Arithmetic Circuit Borrow Lookahead Unit.**) For the subtracter cell that you designed in Problem 1, design a 4-bit borrow lookahead unit. The unit should wire by abutment on top of four of the cells from Problem 1, so that the *Borrow Lookahead* (BLA) Unit routes the four  $\overline{S}$  (sum) signals directly through to its outputs. The Borrow Lookahead Unit should take the input signals  $\overline{B0}$  (least significant borrow input),  $\overline{G0}$ ,  $\overline{P0}$ ,  $\overline{G1}$ ,  $\overline{P1}$ ,  $\overline{G2}$ ,  $\overline{P2}$ ,  $\overline{G3}$ , and  $\overline{P3}$  from its bottom side and produce all borrows  $\overline{B1}$ ,  $\overline{B2}$ ,  $\overline{B3}$ , and  $\overline{B4}$ . The  $\overline{S}$  bits should appear on the top of the BLA unit, and the  $\overline{B}$  bits should all appear on the bottom of the BLA unit. Note that you must design the BLA unit so that the  $\overline{B}$  bits line up with the  $\overline{BORROW\_IN}$  bits of the four subtracter cells, and so that the  $\overline{Gi}$  and  $\overline{Pi}$  bits line up with the  $\overline{GENERATE}$  and  $\overline{PROPAGATE}$  bits of the four subtracter cells. Please turn in a logic schematic, and transistor schematic, and a sticks diagram for the BLA Unit cell.

Save both of your designs, as you will be extending them in a later homework assignment.