RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
16:332:574 CAD Digital VLSI Design
Assignment VI
Assigned: November 22, 2005
Due December 5, 2005

Reading Assignment: Chapter 6 of Weste and Harris.

No collaboration is permitted on this assignment. Your work must be your own. You must turn in theses specific items for each question to receive credit:

- Schematic Composer logic schematic (Problem 1).
- Schematic Composer transistor schematic (Problem 2).
- Virtuoso layout produced manually (Problem 2).

Problems:

1. **Register File Cell Schematic.** Design a stack cell using ordinary CMOS logic that can be laid out by abutment so that data is read from or written to all four sides of the cell. The more cells you put on the chip, the deeper your stack becomes. Cells are arranged in a matrix whose dimensions are the number of bits in a word $\times$ the number of words in a stack. The cell must be able to shift data in two dimensions (i.e., into the stack, right shift, left shift, or complement cell contents). However, it does not have to shift SIMULTANEOUSLY in two dimensions. Use these control signals: *COMPLEMENT* (complement bits within a word), *SHR* (shift right within a word), *PUSH* (push a new word onto the stack), $\overline{SHL}$ (shift left within a word), *PHI* (clock to load the master latch of the cell on the rising edge), $\overline{PHI}$ (clock to load the slave latch of the cell from the master). If the cell is not pushing, shifting, or complementing, then it must remember its current contents. Generate a logic schematic for this cell using the Cadence schematic composer tool.

2. $n-p$ **Dynamic CMOS Layout with Abutment Constraints.** Draw a layout for the two-dimensional shifter cell that you designed using the **Virtuoso** layout editor. The cell must have a regular geometric form so that it can be replicated horizontally and vertically to form a regular array of cells. Use CMOS dynamic $n-p$ logic with alternating n and p logic blocks and two-phase clocking. Also, use **Schematic Composer** to produce a switch-level schematic. Design the cell so that that all input control signals are stable during $\phi = 1$ (the evaluation phase for the n blocks). $\phi = 0$ is the precharging phase for the n blocks. For the p blocks, $\overline{\phi} = 1$ is the precharging phase and $\overline{\phi} = 0$ is the evaluation phase. You are to create a two-stage design with the first stage realized by an n block and the second by a p block. You must also use a C-switch on the output of the p block to hold the latch contents when both the p and n stages are precharging. Otherwise, your cell will forget the current memory contents. Wiring must be by abutment. The way to do this is to find those strongly-connected transistors in the cell using your transistor level schematic, and then draw the sticks so that strongly-connected transistors are placed next to each other. You need draw only one copy of the sticks diagram cell. It must be possible to wire an arbitrarily large, two-dimensional array of cells by

abutment. Please note that the layout area is determined by the interconnections of this design, so please lay out the interconnections FIRST and then place transistors AFTERWARDS where you need them, rather than the other way around.