RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
332:574 CAD Digital VLSI Design
Projects
Sept. 1, 2006

As you are all aware, there is both a short project and a final project for this course. The short project should be sub-component of the final project. Hopefully, the assignments and the midterm will adequately prepare you to do these projects. The purpose of this handout is to describe what I expect from you and your project, and to explain what the project will be.

Your first job is to create a small project. This should have, **AT MOST**, 15 to 30 transistors and should represent a well-defined sub-unit of your large project integrated circuit. The short project is due shortly after Homework VII is due. You are to design the schematic using CMOS logic gates and transistors, and lay out the device with **Cadence** tools. You must also analyze the timing requirements of all long wires and all gates that drive more than one fanout using **Cadence**. You must remove redundant logic and generate test-patterns using the **EST** and **spectralATPG** CAD tools. The short project is due on Nov. 8, 2006.

The course requires a long project, which is a major component of your course grade. I wish to follow past practice, and have each group class project created as a *System-on-a-Chip* (SoC). My reasons for doing this are:

1. System-on-a-Chip design is the future of all hardware systems. You will benefit enormously from doing this project.

2. IBM and Lucent Technologies have suggested that we start creating benchmark System-on-a-Chip designs for academic research. The companies will not let us have access to their designs, so the Universities must create their own.

3. If we plan this project correctly, it will be less onerous than the previous individual projects have been.

The drawbacks of doing this are:

1. If a few people in the class do not complete their part of the SoC, then the entire project is ruined. This nearly happened three years ago with both SoC projects.

2. Students will be forced to work together. However, this is also very excellent experience for your future careers in VLSI design.

We have made a major change to the large project: the work now spans two terms, and two courses (332:574 and 332:578). In the subsequent course, you will do all layout, analog timing verification,

and interconnect work. In this course, you will design the SoC only down to the logic level. Also, credit will not be given for 332:574 until you also complete 332:578.

These SoC projects are suggested, but you can also create your own project idea:

1. A 7-man cellular telephone and memorandum book project. This will have these components:

   (a) Two DSP processors for managing phone conversations.

   (b) Simple microprocessor to handle the memorandum and address book.

   (c) Static non-volatile memory for permanent contents of address book.

   (d) Bus module for communications on the chip.

   You will not be asked to design the RF stage, the power amplifier, or the heterodyning analog multiplier circuit. It is still not feasible to integrate these components with the rest of the hardware, because the RF stage requires large, precision inductors, which we cannot yet make on a chip; an integrated CMOS power amplifier has severe noise pickup problems from the rest of the chip; and the multiplier also has severe noise pickup problems.

2. A 2-man wireless EZ-Pass toll collection chip and base station toll booth transmission chip project. This will have these components:

   (a) Encryption/decryption unit for encrypting all transmissions having to do with account deductions to pay tolls.

   (b) Simple microprocessor controller to operate the wireless chip and the base station.

   (c) Static non-volatile memory for permanent contents.

   (d) Simplistic DSP unit for wireless transmission.

3. A Global Positioning Service chip design project for 4 people.

   (a) DSP baseband processor.

   (b) Simple microprocessor.

   (c) Static non-volatile memory.

   (d) Bus module.

4. An 802.11 receiver/transmitter project for 5 people.

   (a) DSP baseband processor.

   (b) Simple microprocessor.

   (c) Static non-volatile memory.

   (d) Bus module.

5. A low power Bluetooth project for 4 people.

   (a) DSP baseband processor.

   (b) Simple microprocessor.

   (c) Static non-volatile memory.

   (d) Bus module.

The projects will be fabricated in the TSMC 0.18 μm technology.

We will rely on outside advice from Bell Laboratories, Agere Systems, Lucent Technologies, and Motorola as we design the telecommunications circuits for these devices. In order to avoid having an entire project ruined if someone does not do their part of the work, I will be the manager of all these projects. I will break up the entire design effort into various little projects, some of which will duplicate the work from last year. My hope is to get graduate SoC chips fabricated around June, 2007 and submit them to the Mentor Graphics United States Chip Design Contest. Several years ago, a design from this class was judged the Best Design in the USA in the Novice Design Category.

By Oct. 4, we must finalize the project description and specifications, and determine who is doing what parts of the chips. I will work extensively with you on this proposal to make sure that the SoC projects are doable. Please note that in the past, each graduate student has personally designed projects varying in size from 20,000 transistors to 60,000 transistors. In last year's SoC projects, the most that any single person did was 10,000 transistors. Therefore, the focus here is on doing less, but attaining a higher quality level in the design than before. Since we have prior designs and experience to look at, this should be possible.

Each graduate student is expected to do a somewhat ambitious and first-rate piece of the SoC, meaning that all synthesis and analysis aspects of the chip must be performed, and the work must be correct.

Required Design Activity	Grade	Due Date	Penalty
Project Conceived and One Page Description Handed In	A–	9/25/06	– 1/2 Letter Grade on Project
System Block Diagram	B+	9/27/06	– 1/2 Letter Grade on Project
Team Work Assignment	B	10/2/06	– 1/2 Letter Grade on Project
Revised System Block Diagram & Specs.	B–	10/4/06	– 1/2 Letter Grade on Project
Revised Work assignment	C+	10/4/06	– 1/2 Letter Grade on Project
Final System Specs	C	10/11/06	– 1/2 Letter Grade on Project
Verilog Descriptions of Logic (if Synopsys synthesized logic) where appropriate	C-	11/1/06	– 1/2 Letter Grade on Project
Short Project Due	D+	11/8/06	– 1/2 Letter Grade on Project
Logic Schematics from Cadence and Logic Simulation Results	D	11/29/06	– 1/2 Letter Grade on Project
SpectralATPG Redundant Logic Removal Commentary where appropriate	D-	12/6/06	– 1/2 Letter Grade on Project
Interim Chip Project Presentations (Evening)	F+	12/11/06	– 1/2 Letter Grade on Project
Interim Project Report	F	12/13/06	– 1/2 Letter Grade on Project

There is a one-page group status report due on each of these deadlines. Include with it logic or Verilog cell descriptions or logic schematics of circuits you have already designed as appropriate. Statements like "We designed a static register cell, but then discovered that it was not static ... redesigning it." are just fine, and are encouraged. Also, on Dec. 13, 2006, you should be prepared to give a thirty minute group oral presentation of your chip, complete with viewgraphs. I am sorry, but these deadlines will be brutally enforced, since prior experience shows that students are not responsible enough to get their work done unless there is a serious penalty.

You must turn in a final report on or before Dec. 13th, 2006. The final report MUST include:

- An overall description of the sub-project, its organization, and how it works.
- A block diagram of the chip, with pads clearly labeled as to function (signal name).
- A check plot of the project, with as much annotation as necessary to understand it. The best scheme would be logic schematics of the individual cells together with descriptions of how they work; then, include schematics of larger assemblies, etc.
- Engineering calculations that estimate the performance of your chip. In addition, you should simulate all pieces of your design that are critical to its performance. You are expected to simulate the entire chip with the **Cadence** logic simulator.
- A complete plan for testing your chip, spelled out in detail, including test patterns. Also, you can use built-in self-testing hardware. You must add the necessary design-for-testability hardware to the chip.
- A description of where the Cadence logic library and test-pattern files reside on the Sun computers.
- A one or two page data book style description. The intent is that you would give this sheet of paper to someone who wants to use your chip. Look at the Texas Instruments MOS parts catalog for an example data book description.
- A description of at most one quarter page in length explaining each unique cell that you created for your project. Each cell description must include a logic schematic, **EST** or **spectralATPG** information indicating that no redundant logic exists, and logic simulation results from **Cadence**.
- A description of how useful **Cadence**, **Synopsys**, **EST**, and the other Rutgers CAD tools were to you.
- You must estimate the power consumption of your chip.

You must take the second graduate course in order for you to receive credit for this course.

You should use the following design tools: **Cadence** schematic capture, layout capture, logic simulation, and analog simulation. **EST** (a combinational logic test-pattern generator), and **spectralATPG** (a sequential logic test-pattern generator). Other Rutgers CAD tools may also be used.

Your final projects will be graded on the following criteria:

- Logical correctness as determined by logic simulation (shift registers that don't shift will cost you points).
- Low power design.
- Quality of the chip documentation (if it is a mess, you will lose points).
- Completeness.

Verify logical correctness as you progress in the design phase, not after the whole thing is designed.