# Graduate Course for Spring 2001
# TESTING OF
# ULTRA LARGE SCALE INTEGRATED CIRCUITS
# 16:332:576
# Section 01 Index Number 46426

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This course covers the problems of testing of *Ultra Large Scale Integrated Circuits* (*ULSI*), the design of circuits for testability, the design of built-in self-testing circuits, and the use of the IEEE Boundary Scan Standards. IBM's ULSI circuits contained 50 million transistors in 2000. *Testing* determines whether a manufactured ULSI circuit contains any broken wires or transistors. *Design for Testability* is necessary, since testing has become so difficult that we must explicitly synthesize circuits to be testable and testing must be considered during all design phases. Testing of circuits is currently one of the most critical obstacles to designing microprocessors and *Application Specific Integrated Circuits* (*ASIC's*). Chip designers, who want to learn about design for testability in order to design better chips, and researchers, who wish to develop algorithms and patents for testing, should take this course. Currently, verification testing and production testing represent 50 to 60 % of the cost of making VLSI chips, and is now the biggest cost of this technology. The course will be presented as a series of lectures, and each student will have to give a half hour in-depth lecture on a topic that he/she has researched in the literature. In addition, each student will have to turn in a *well-researched* and *well-written* paper on his topic. The level of this course is appropriate for a college senior or a first year graduate student with experience in Digital Electronics Design. The seminar will meet once a week, for three hours. Agrawal and Bushnell have finished a new testing book based on this course, which will be used this year.

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| **PROFESSORS**: | Michael L. Bushnell | Room 624, CORE Bldg. |
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| Bushnell's Telephone: | (732)445-4854 | |
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| Agrawal's Email Addresses: | va@research.bell-labs.com or va@agere.com | |
| Bushnell's Office Hours: | Tuesday, Wednesday 3:00-6:00 | |
| Meeting Room: | Room 216, SEC Building | |
| Meeting Time: | Friday, 9:20-12:30 a.m. | |
| First Meeting: | Friday, Jan. 19, 2001 | |
| Course Completion Date: | May 11, 2001 | |

**TEXT:**

- *Essentials of Electronic Testing: Digital, Analog, and Mixed-Signal*, Bushnell and Agrawal, Kluwer Academic Press, Boston, 2000, ISBN # 0-7923-799-1-8.

**REFERENCE BOOKS:**

- See Appendix C of the Bushnell & Agrawal textbook.

**ASSUMED BACKGROUND:**

Boolean Algebra
Sequential Circuit Logic Design
C and C++ Language Programming
Combinational Circuit Logic Design
College Sophomore Electrical Network Theory
RISC Computer Architecture

**WORK EXPECTED OF STUDENTS.** The course will meet once a week, for three hours, for 13 weeks. There are a series of lectures that each student is expected to attend. Each student will have to complete all of these items:

1. A twenty minute in-depth presentation on a testing topic that he/she has researched in the literature. The student talk must SUPPLEMENT, not REITERATE, material presented by the main lecturer(s). Please prepare viewgraph transparencies so that your talk goes faster.

2. An individual programming or design project, in which he/she writes part of a Computer-Aided Design program for circuit testing in C++, or develops a testing circuit. The programming project must be demonstrated to the rest of the class at the term end.

3. Thirteen homework assignments on the various test-pattern generation algorithms and on the structure of scan-design and built-in self-testing circuits.

4. A *well-researched* and *well-written* paper (of at most 6 pages) describing his/her topic, with proper literature citations. Badly written papers will be returned to you for rewriting. For examples on how to correctly write technical papers, look at the papers cited in Bushnell and Agrawal.

5. A final examination.

**TENTATIVE SCHEDULE OF TOPICS:**

| Topic | Reading Chapter | Lecturer | Date | Home-work |
|---|---|---|---|---|
| Part I – Introduction to Testing | | | | |
| Test Introduction & Test Equipment | 1-2 | Agrawal/Bushnell | 1/19/01 | 1 |
| Test Economics, Product Quality, & Fault Modeling | 3-4 | Agrawal | 1/26/01 | 2 |
| Part II – Test Methods | | | | |
| Logic & Fault Simulation | 5 | Agrawal | 2/2/01 | 3 |
| Testability Measures and Combinational Automatic Test-Pattern Generation (ATPG) | 6, 7 | Bushnell | 2/9/01 | 4 |
| Combinational ATPG (Continued) | 7 | Bushnell | 2/16/01 | 5 |
| Sequential Automatic Test-Pattern Generation | 8 | Agrawal | 2/23/01 | 6 |
| Memory Testing | 9 | Bushnell | 3/2/01 | 7 |
| Analog Testing | 10 | Bushnell | 3/9/01 | 8 |
| Delay Fault and IDDQ Testing | 12 & 13 | Agrawal/Bushnell | 3/23/01 | 9 |
| Part III – Design for Testability | | | | |
| Design for Testability | 14 | Agrawal | 3/30/01 | 10 |
| Built-In Self-Testing I | 15 | Bushnell | 4/6/01 | 11 |
| Built-In Self-Testing II | 15 | Bushnell | 4/13/01 | - |
| Boundary Scan & Mixed-Signal Test Bus | 16 & 17 | Bushnell | 4/20/01 | 12 |
| System Test & CORE-Based Design | 18 | Agrawal | 4/27/01 | 13 |

**GRADING:**

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|---|---|
| Homeworks 1-13 (Only 10 best are included) | 25 % |
| 20 Min. In-Class Presentation | 10 % |
| Final Paper | 15 % |
| Course Project | 30 % |
| Final Examination | 20 % |
| Total | 100 % |

Note that if you do not interact with the rest of the class during the term, then your In-Class Presentation grade will be reduced.

**HOMEWORK AND FINAL EXAM TOPICS:**

1. *Homework 1:* Test Introduction and ATE
2. *Homework 2:* Test Economics and Fault Modeling
3. *Homework 3:* Logic and Fault Simulation
4. *Homework 4:* Testability Measures
5. *Homework 5:* Combinational ATPG
6. *Homework 6:* Sequential ATPG

7. *Homework 7:* Memory Testing
8. *Homework 8:* Analog Testing
9. *Homework 9:* Delay Fault Testing & IDDQ Testing
10. *Homework 10:* Design for Testability
11. *Homework 11:* Built-In Self-Testing
12. *Homework 12:* Boundary Scan and Analog Test Bus
13. *Homework 13:* System Test and CORE-Based Design
14. *Final Exam:* All Topics