RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
14:332:479 Concepts in VLSI Design
Assignment III
Assigned: September 27, 2006
Due October 9, 2006

Reading Assignment: In Chapter 3: Sections 3.1, 3.2, and 3.3; all of Chapter 4. Concentrate on Section 3.3 – Lambda-based n-well rules.

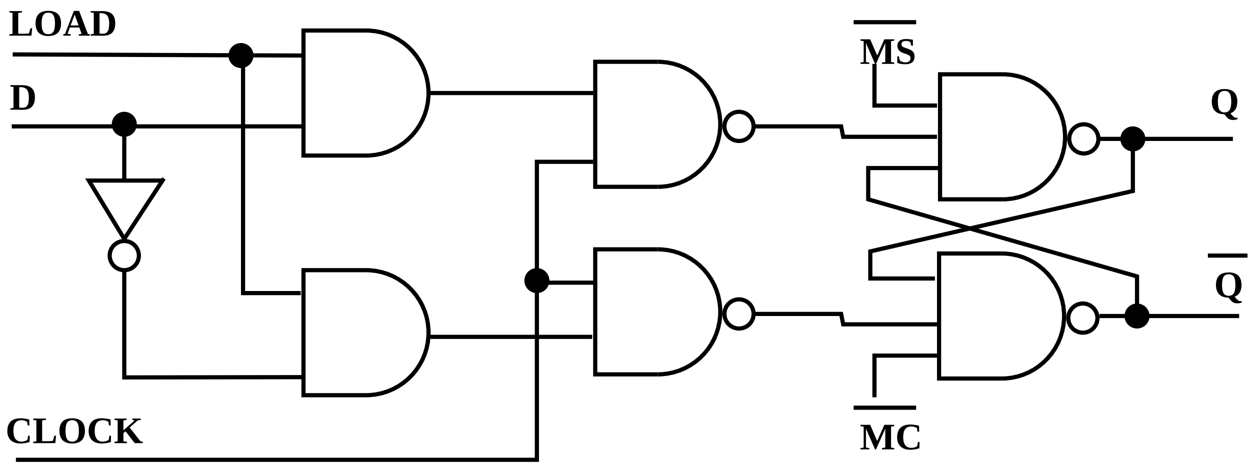
If you do not know how to design NOR and NAND latches, please read *Digital Design Principles and Practices*, by John F. Wakerly, Publisher Prentice-Hall, 1990, pages 349-360 and 363-364. If you are unfamiliar with nMOS design, please review the VLSI Course lecture notes. nMOS design material can also be found in the obsolete book *Introduction to VLSI Systems*, by C. Mead and L. Conway, Publisher Addison-Wesley, 1980, pages 5-6 and 15-17.

NO COLLABORATION IS PERMITTED ON THIS ASSIGNMENT. YOUR WORK MUST BE YOUR OWN. YOU WILL BE SEVERELY PENALIZED FOR LOGIC CIRCUIT ERRORS. POINTS WILL BE DEDUCTED FOR EACH LAYOUT OR STICKS DESIGN RULE VIOLATION. NON-RECTANGULAR LAYOUTS AND LAYOUTS THAT WASTE AREA WILL LOSE ADDITIONAL POINTS.

Read the sections of the manual describing the Cadence layout editor and simulator tutorials. Log into a Sun work station in one of the CAD labs and do both tutorials. Then, read the rest of the material on the Cadence layout tool.

Problems to be handed in:

1. (**CMOS NAND Latch Logic Schematic Entry.**) Consider the following latch:



Draw a CMOS logic circuit diagram (using the Cadence schematic editor tool) for the Static CMOS NAND D Latch.

2. (**CMOS Latch Logic Simulation.**) Simulate the NAND latch logic schematic at the logic level with the Spectre analog simulator. Perform exhaustive logic simulation for all values of the inputs $LOAD$, D, $\overline{MS}$, $\overline{MC}$, and $CLOCK$ using the simulator and turn in logic timing diagrams for the NAND latch produced by the logic simulator. If your latch does not simulate correctly, redesign it to fix it.

3. (**CMOS Latch Transistor Schematic Entry.**) Draw a CMOS transistor circuit diagram (using the Cadence schematic editor) for the Static CMOS NAND D Latch (use the transistor realizations of ordinary CMOS gates). Assume that each p transistor can have a W/L ratio of 6 λ to 2 λ. Assume that each n transistor can have a W/L ratio of 3 λ to 2 λ. Provide inverters if you need the opposite polarity of any circuit signal. Perform any logic optimization on the latch logic that you deem advisable before creating the transistor-level latch schematic.

4. (**CMOS Latch Transistor Simulation.**) Simulate the NAND latch logic schematic at the transistor level with the Cadence simulator. Perform exhaustive logic simulation for all values of the inputs $LOAD$, D, $\overline{MC}$, $\overline{MS}$, and $CLOCK$ using the simulator and turn in logic and switch level timing diagrams for the NOR latch produced by the simulator. If your latch does not simulate correctly, redesign it to fix it.

5. (**CMOS NOR Latch Transistor Schematic Entry.**) Draw a CMOS logic gate diagram on paper for the NOR form of latch (use the same assumptions as above). In this form, the two output NAND gates in the above schematic are replaced with NOR gates. Pay attention to the polarity level of logic signals (some of them change from the NOR version of the latch, in particular $LOAD$, MC, and MS) and make sure that you label signal polarities correctly. Then, draw the CMOS transistor circuit diagram for the NOR latch (using the Cadence schematic editor).

6. (**CMOS NOR Latch Transistor Simulation**.) Simulate the NOR latch logic schematic at the transistor level with the logic simulator. Perform exhaustive logic simulation for all values of the inputs $LOAD$, D, MC, MS, and $CLOCK$ using the logic simulator and turn in the switch level timing diagram for the NOR latch produced by the simulator. If your latch does not simulate correctly, redesign it to fix it.

7. (**CMOS Static Inverter Loop Latch.**) Redesign the above latching circuit to use a static inverter loop with appropriate CMOS transmission gates. Enter the transistor switch-level schematic for the latch into the Cadence schematic editor, using the same conventions as before, assuming that the $LOAD$ signal is available in dual-rail logic (both $LOAD$ and $/LOAD$ are available). This will allow you to use CMOS transmission gates. However, only $CLOCK$ is available, so if you need $/CLOCK$, you must include the inverter to generate it. Implement only the $/MS$ function to asynchronously set the latch, and not the $/MC$ function. The slash in front of a signal means that it is active low. Strive for the absolute minimum-area layout. Turn in the transistor schematic from the Cadence schematic editor and the transistor level timing diagram from the logic simulator.

8. (**Inverter Loop Latch Sticks Diagram.**) Draw a minimal area sticks diagram of the Static Inverter Loop Latch. Implement only the $/MS$ function, and not the $/MC$ function.

9. (**Static CMOS Layout Using Layout Editor.**) Draw a full n-well CMOS layout (yes, the actual IC layout) for the static inverter loop version of the latch using the λ design rules appearing in the back fly-leaf of Weste and Harris using the Cadence layout editor and the NC State 180 nm CMOS process. The λ design rules are fully described in Section 3.3 of the book. We are using the TSMC $0.18 \mu m$ feature size process, which has 6 metal layers. Use these color conventions (which should be enforced by the Cadence layout editor):

n+ Region: Green crosshatched	p+ Region: Yellow crosshatched
n-well: Green hatched	Polysilicon: Red crosshatched
n select: Green outlined	p select: yellow outlined
Metal1: Blue hatched	Metal2: Purple crosshatched
Metal3: Light Blue hatched	Metal4: White dotted
Metal5: Light Blue dotted	Contact cut: Brown dotted
Metal6: Gold hatched	via: Purple crosshatched
via2: Light Blue crosshatched	via3: White crosshatched
via4: Dark Blue crosshatched	via5: Gold crosshatched
overglassing: Grey lined	

Assume that contacts can be made to the Metal2 layer only from the Metal1 layer, and that these contacts cannot lie on top of any other contact. The Metal2 layer must be 3λ units wide and spaced from other Metal2 geometry by 4λ, whereas the Metal1 layer must be 3λ units wide and spaced from other Metal1 geometry by 3λ. The Metal2-Metal1 contact has a $2\lambda \times 2\lambda$ contact cut, with both Metal1 and Metal2 overlapping the cut by 1λ. Similarly, assume that contacts can be made to the Metal3 layer only from the Metal2 layer, and that these contacts cannot lie on top of any other contact. The Metal3 layer must be 3λ units wide and spaced from other Metal3 geometry by 3λ. The Metal3-Metal2 contact has a $2\lambda \times 2\lambda$ contact cut, with both Metal1 and Metal2 overlapping the cut by 2λ. A 1λ space must be provided between any Metal2-Metal1 contact and any other contact or between any Metal3-Metal2 contact and any other contact. Leave out overglassing. You will be marked off for each design rule violation. Strive for the absolute minimum-area layout. Do not forget to include substrate V_{SS} contacts, and n-well V_{DD} connections using the correct contact structures shown in the book. The Cadence layout editor should correctly insert n-wells, n+ and p+ regions for you into the layout, but you must supply substrate and V_{SS} contacts and you must ensure that every n-well is anchored at V_{DD}. The Cadence layout editor provides a color layout printing facility. Plot your final, CORRECT layout on the color laser printer known as c633gn. However, please only do this for the very final layout. No credit will be given for hand-plotted layouts. Save the schematic, switch-level schematic, and layout files in your directories. Perform analog circuit simulation on the analog circuit extracted from your Cadence layout using the analog simulator. Route signals D, Q, $\overline{Q}$, $CLOCK$, $LOAD$, V_{SS}, $/MS$, and V_{DD} to the edge of the cell, or credit will be taken off. Also, the D and Q signals should be at the same position and layer, but D is on the left side of the cell and Q is on the right side. The $LOAD$, $CLOCK$, V_{SS}, and V_{DD} signals must route straight through the cell on a single wire. Turn in a color layout plotted by the layout editor and an analog circuit simulation timing diagram from the analog simulator.

10. (**Static nMOS Transistor Latch.**) Redesign the CMOS latching circuit to be an nMOS latching circuit. Include only the $/MS$ signal. Draw a transistor circuit diagram (not a

layout) by hand, and assume that the circuit will behave correctly if you make the K_n ratio for the pulldown transistor n-block is 4 times greater than the K_n ratio for a pullup transistor depletion n-block. Do this by lengthening the pullup transistor, NOT by widening the pulldown transistor. Don't forget that in the n-tree, two transistors in series produce half as strong an n-tree, and two transistors in parallel produce twice as strong an n-tree, so you must adjust the pullup device accordingly. Label all transistor sizes in the diagram, and show the correct gate connections for the pullup transistors. Do not bother to simulate this design.