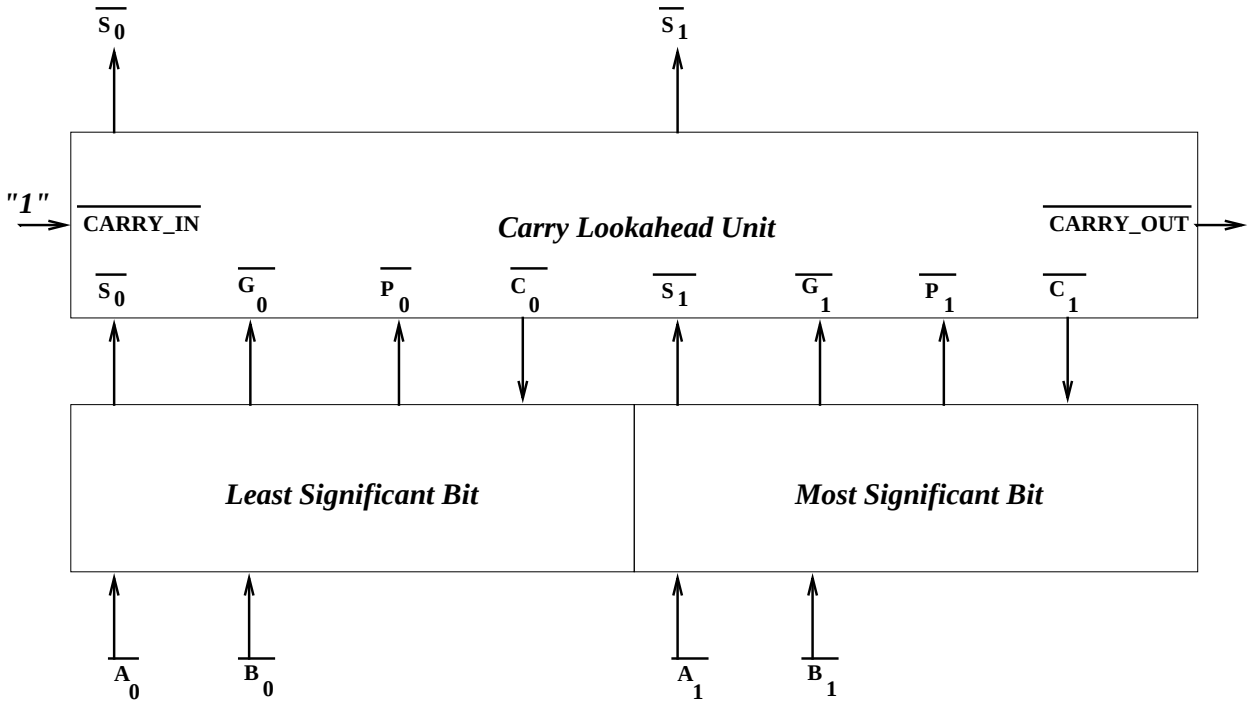
RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
16:332:574 CAD Digital VLSI Design
Assignment II
Assigned: September 29, 2004
Due October 6, 2004

Reading Assignment: Chapters 1 and 2 and Section 8.2.1.2 of Weste and Eshraghian.

No collaboration is permitted on this assignment. Your work must be your own.

Some signals in this assignment are active low (negative logic) and some are active high (positive logic).

1. (**CMOS Arithmetic Circuit Wiring by Abutment.**) You are to design a carry-lookahead adder module that adds two input n-bit unsigned binary numbers $\overline{A}$ and $\overline{B}$ and a $\overline{CARRY\_IN}$ signal and produces an output n-bit sum $\overline{S}$, and n-bit $\overline{GENERATE}$ and $\overline{PROPAGATE}$ signals. You are to design a one-bit adder, and then you should replicate an array of these one-bit adders to realize an n-bit adder. Thus, we only need to do a sticks layout for one cell, as follows. Each cell has three inputs (corresponding bits of $\overline{A}$, $\overline{B}$ and $\overline{CARRY\_IN}$)



and three outputs (a $\overline{SUM}$ bit ($\overline{S}$), $\overline{GENERATE}$, and $\overline{PROPAGATE}$ signals). The cells are designed to be rectangular and designed to fit conveniently next to one another. We wire the cells by making sure that the outputs of one cell touch the inputs of the next cell, and are routed on the same wiring layer. This allows us to build an adder of arbitrary size (any n) by simply juxtaposing a sufficient number of cells. You only have to design a single bit of the adder cell. The signals $\overline{A}$ and $\overline{B}$ should be on the bottom of the cell, and the output signals $\overline{S}$, $\overline{GENERATE}$, and $\overline{PROPAGATE}$ should be on the top of the cell, Also, the input $\overline{CARRY\_IN}$ signal should be on the top of the cell. $\overline{S}$ should be directly across from input $\overline{A}$. Turn in a logic schematic, a transistor schematic, and a sticks diagram for a single cell. Concentrate on making the cell rectangular and very compact. Don't forget to minimize your cell logic, using Karnaugh maps. For extra credit, explain what simple additions are needed to turn this adder circuit into a subtracter circuit.

2. (**CMOS Arithmetic Circuit Carry Lookahead Unit.**) For the adder cell that you designed in Problem 1, design a 4-bit carry lookahead unit. The unit should wire by abutment on top of four of the cells from Problem 1, so that the *Carry Lookahead* (CLA) Unit routes the four $\overline{S}$ (sum) signals directly through to its outputs. The Carry Lookahead Unit should take the input signals $\overline{C0}$ (least significant carry input), $\overline{G0}$, $\overline{P0}$, $\overline{G1}$, $\overline{P1}$, $\overline{G2}$, $\overline{P2}$, $\overline{G3}$, and $\overline{P3}$ from its bottom side and produce all carries $\overline{C1}$, $\overline{C2}$, $\overline{C3}$, and $\overline{C4}$. The $\overline{S}$ bits should appear on the top of the CLA unit, and the $\overline{C}$ bits should all appear on the bottom of the CLA unit. Note that you must design the CLA unit so that the $\overline{C}$ bits line up with the $\overline{CARRY\_IN}$ bits of the four adder cells, and so that the $\overline{Gi}$ and $\overline{Pi}$ bits line up with the $\overline{GENERATE}$ and $\overline{PROPAGATE}$ bits of the four adder cells. Please turn in a logic schematic, and transistor schematic, and a sticks diagram for the CLA Unit cell.

Save both of your designs, as you will be extending them in a later homework assignment.