14:332:479 Concepts in VLSI Design
Fall 2006
Electrical and Computer Engineering Department
School of Engineering
Rutgers University

August 31, 2006

PHILOSOPHY:

This course presents a systematic approach to the design of Full-Custom, Ultra Large Scale Integrated Circuits (55 million transistors in the Intel Pentium 4 running at 3.6 GHz, one billion transistors on the latest 1 Gbit DRAM). At present, industry is looking forward to 1 billion transistor designs. The course is intended for those who wish to know how to design an IBM Power PC, an AMD Athlon microprocessor, or a twenty million transistor custom *Application-Specific Integrated Circuit* (ASIC). Today, this design process is accomplished on engineering work stations and PCs, using complex *Computer-Aided Design* (CAD) programs. We will design and make individual chip designs in this course using commercial VLSI Design software donated by Cadence and Synopsys Corporations. You will be taught how to effectively use this software, which is used world-wide in the electronics industry. At this moment, the industry is scaling to 45 nm chip technology. Since lithography, power, and testing problems will doom the present VLSI technology by the time it scales below 20 nanometer feature sizes, we are introducing nanotechnology into this course, which is the future of all chip design. A highlight for students from previous years was the fabrication line tour of Micron Technology's $50nm$ fab. line in Manassas, Virginia, in August, 2006.

COURSE DESCRIPTION:

Introductory Digital VLSI Chip Design, CMOS Technology & Design Rules, Clocked Logic & Registers, CMOS Technology & Design Rules, Static and Dynamic CMOS logic, Electrical On-chip Timing Considerations, CAD Tools (Layout Editors, Logic Simulators, Automatic Test-Pattern Generators, Design Rule Checkers, and Wire Routers), Analog MOSFET Timing Analysis, Elementary Circuit Testing. Cell Library construction and Chip Assembly.

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Course Web Site:	http://www.caip.rutgers.edu/∼ bushnell/rutgers.html
Lecture Times:	Monday, Wednesday 5:00 p.m. - 6:20 p.m.
Classroom:	Room 538, CORE Bldg.
Course Laboratory:	Rooms CORE 629 and CORE 533
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PREREQUISITES:

- 332:231 Digital Logic Design
- 332:252 Programming Methodology I
- 332:361 Electronic Devices
- 332:366 Digital Electronics
- 332:368 Digital Electronics Lab.

COREQUISITES:

- 332:331 Computer Architecture and Assembly Language
- 332:333 Computer Architecture Laboratory

VERY HELPFUL COURSES:

- 332:361 Electronic Devices
- 332:362 Analog Electronics
- 332:465 Physical Electronics

TEXTS:

- Neil Weste and David Harris, *CMOS VLSI Design: A Systems Perspective*, third edition. Reading, MA: Addison-Wesley, 2005, ISBN # 0-321-14901-7.
- Michael L. Bushnell and Vishwani D. Agrawal, *Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits*, third printing. Boston: Kluwer Academic Publishers, 2000 (optional), ISBN #0-7923-7991-8.

Some material will be covered only in lecture. The textbooks are available now at the Rutgers University Bookstore.

LABORATORY:

- You should obtain Cartesian graph paper and a set of colored pencils (red, yellow, green, blue, black, purple) for drawing *sticks* diagrams during the first two weeks of the course.
- The homeworks are designed using CAD tools on Sun work stations and LINUX PCs.

- Arrangements for laboratory access will be announced later.
- A subsequent memo will describe the laboratory regulations.
- This course is always under development, and its content is subject to change. Constructive suggestions from students are greatly appreciated.

ASSUMED BACKGROUND:

- Elementary Transistor Electronics
- Boolean Algebra
- MOS Digital Logic Design – combinational and sequential circuits, SSI & MSI
- SR, D, T, and JK Flip-Flops and SR and D Latches
- Number Systems (Bases 2, 8, and 16) and Coding systems
- Signed Magnitude, Ones-complement, and Twos-complement representations
- Register Transfer Level Design
- Elementary Diode and Transistor Theory
- Elementary Microprogramming
- Interrupt Systems
- Microprocessors and Minicomputers
- Electrical Network Theory

If you are unfamiliar with any of these concepts, you should drop this course.

GRADING:

Homeworks 1-10	40%
Midterm Examination	30%
Final Examination	30%
Total	100%

The midterm will be on Nov. 8, 2006. Homework is due at the beginning of lecture on the due date. Late homework gets a 0 grade. The only exceptions are for documented illnesses, accidents, or deaths in the family. If you miss an examination or a homework assignment for a valid reason, please notify us (if possible) during the examination or before the homework is due.

Students are expected to work independently on both homework and examinations. NO COLLABORATION is permitted, unless you are otherwise instructed. Your work must be your own. Students who are caught cheating will be prosecuted to the full extent of the Rutgers University Honor Code – this includes electronic cheaters.

Statute of limitations policy: You have one week after the day each homework or examination is returned to you to ask for a grade change. Grades will be changed only if:

1. We added up your score wrong.

2. We made an error in grading a particular problem.

At the end of the term, we will not argue about points on Homework #1, etc. No exceptions will be made. No incompletes will be given for this course, unless there is a documented illness, accident, or death in the family.

MAJOR CHANGES:

1. With the third edition of the textbook, the material for this course has expanded so much that it has been split into two courses: *Concepts in VLSI Design* and *Deep Sub-micron VLSI Design*. Also, the short and large projects have been deleted and moved to the spring course 332:480. More homework and a final exam have been added to this course. In order to complete your undergraduate design elective, you must take the companion course to this one, 14:332:480 *Capstone Design – VLSI Design*, in the spring of 2006, which is exclusively a *System-on-a-Chip* (SoC) team design project course.

2. Since nanotechnology is the future of ULSI design, we are introducing it into the course.

3. We no longer allow analog circuit design projects in this course, as there is a course, 16:332:577 *Analog and Low-Power Digital VLSI Design*, that deals with analog design.

4. Graduates of this course are highly demanded by semiconductor and computer companies, PROVIDED THAT THEY GET AN "A" IN THIS COURSE AND HAVE A HIGH GPA IN OTHER COURSES. The job market was abysmal in 2003, but is now very robust. Companies that have hired students who took this course recently include Qualcomm, Broadcom, Centerpoint, Conexant, Intel, IBM, Sun Microsystems, Trans-Meta Corp, Advanced Micro Devices, AT&T, Lucent Technologies, Agere, LSI Logic Corp., IBM, Sun Microsystems, Compaq, Texas Instruments, Sarnoff Laboratories, Lockheed-Martin, Hewlett-Packard, Viragelogic Corp., Mentor Graphics, and Synopsys.

5. Automatic logic synthesis software translates your chip description in the Verilog or VHDL hardware description languages into logic gates. Use Verilog or VHDL and run the Synopsys system to synthesize your logic for VLSI Design.

GRADING PROCEDURE:

The course grading is intended to encourage you to use a structured design methodology, in order to accelerate your design activities. All layouts and circuits will be graded according to this procedure:

1. If there is no logic schematic from the Cadence System, the grade is 0.

2. If there are no convincing logic simulation results from the Cadence System, the grade is 0.

3. For every redundant logic signal in the circuit, you lose 2 points The Rutgers Automatic Test-Pattern Generator **EST** will find these redundant logic gates in your circuit automatically. You are REQUIRED to supply the **spectralATPG** or **EST** commentary for each of your logic designs.

4. If you do not list the logic level circuit test-patterns, for purely logic circuits in Homeworks 2 through 10, the grade is 0.

5. You must supply an automatically-generated module layout from the Standard Cell Place and Route software for certain layouts after Homework III or the grade is 0. You may still manually lay out these modules with the Layout Editor if you are dissatisfied with the

automatically created layout. Note that the layout compactor can be used to squash an automatically-generated layout.

6. For all layouts, we will subtract 2 points for every logic error and 1 point for every physical design rule error. Then, we will multiply the remaining score by the ratio of the solution layout area to your layout area. The net effect is that layouts with logic and design rule errors or that use excessive chip area are severely penalized. Hand drawn layouts (with colored pencils on paper) will get a grade of 0.

7. If you do not provide analog simulation results for the circuit extracted from the layout, the grade is 0.

The purpose of this grading procedure is not to harass you or embarrass you, but to save you ENORMOUS amounts of time during your chip design. It is now routine in the semiconductor industry for a designer to rapidly produce a 10 million transistor chip using CAD tools and following the structured design methodology taught in this course.

SCHEDULE:

Topic	Powerpoint Module	Dates	Home-work
TRANSISTORS AND FABRICATION			
Transistor History	1 (38)	9/6/06	
Trends in ULSI Technology for the Next 15 Years	2 (63)	9/11/06	
The VLSI Transistor and CMOS Fabrication	3 (55)	9/13/06	1
MUXes, Latches, Flip-Flops & Layout	4 (52)	9/18/06	
MIPS Processor Example	5 (44)	9/20/06	
DELAY CALCULATIONS			
CMOS Transistor Theory	6 (34)	9/25/06	2
Resistance and Capacitance Calculation for Transistors	7 (33)	9/27/06	
DC & Transient Response	8 (88)	10/2/06	3
Logical Effort	9 (47)	10/4/06	
Wires	10 (40)	10/9/06	
LOGIC			
Combinational Circuits	11 (38)	10/11/06	4
Circuit Families	12 (50)	10/16/06	
Sequential Circuits	13 (61)	10/18/06	
Logic Gate Families and Layout	14 (42)	10/23/06	5
SIMULATION			
SPICE Simulation	15 (29)	10/25/06	
DATA PATH DESIGN			
Adders	16 (26)	10/30/06	
Datapath Functional Units	17 (37)	11/1/06	6
SRAM	18 (69)	11/6/06	
MIDTERM		11/8/06	
TESTING			
Introduction to Testing	19 (45)	11/13/06	7
Testing Methods	20 (38)	11/15/06	
Built-In Self-Testing	21 (27)	11/20/06	
IEEE Boundary-Scan Standard and System Test	22 (30)	11/27/06	8
RELIABILITY AND POWER			
Circuit Pitfalls and Reliability	23 (43)	11/29/06	9
Power Estimation	24 (19)	12/4/06	
Packages and Power	25 (21)	12/6/06	
Pads	26 (31)	12/11/06	10
SCALING			
Scaling	27 (55)	12/13/06	
Case Study: Intel Processors	28 (13)	12/13/06	
Fab. Line Tour at Micron Technologies, Manassas VA	TBA		

HOMEWORK AND FINAL EXAM TOPICS:

1. Homework 1: Sticks Diagrams, Logic Gates, and MUXes
2. Homework 2: Addition/Subtraction Circuits
3. Homework 3: Latches, Flip-Flops, and Layout
4. Homework 4: Parasitic R, C, and L Estimation
5. Homework 5: Decoders and Dynamic Logic
6. Homework 6: SRAM Design
7. Homework 7: Dynamic Two-Phase Clocking
8. Homework 8: Cell Assembly and Testing
9. Homework 9: Multiplier Design
10. Homework 10: Standard Cell ALU Design
11. Midterm: Everything so far
12. Final Exam: Everything

REFERENCE BOOKS:

- H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Reading, MA: Addison-Wesley, 1990, ISBN # 0-201-06008-6.
- M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory, & Logic VLSI Circuits*, 1st Edition. Boston: Kluwer Academic Publishers, 2000, ISBN #0-7923-7991-8.
- *Cadence Design System Manuals* (on-line).
- S. A. Campbell, *The Science and Engineering of Microelectronic Fabrication*, New York: Oxford U. Press, 1996, ISBN # 0-19-510508-7.
- T. Dillinger, *VLSI Engineering*. Englewood Cliffs, NJ: Prentice Hall, 1988, ISBN # 0-13-942731-7 025.
- J. E. Franca and Y. Tsividis, *Design Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, Englewood Cliffs, NJ: Prentice-Hall, 1994, 2nd Edition, ISBN # 0-13-203639-8.
- S. Ghandhi, *VLSI Fabrication Principles. Silicon and Gallium Arsenide*, 2nd Edition, New York: John Wiley & Sons, 1994, ISBN # 0-471-86833-7.
- C. Hu, editor, *Nonvolatile Semiconductor Memories, Technologies, Design, and Applications*. Piscataway, NJ: IEEE Press, 1991, ISBN # 0-87942-269-6.
- S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*. New York: McGraw-Hill, 1996, ISBN # 0-07-038046-5.
- Tracy Kidder, *The Soul of a New Machine*. Boston: Little, Brown and Co., 1981, ISBN # 0-316-49170-5. This book won the Pulitzer Prize.

- K. Lee, M. Shur, T. A. Fjeldly, and T. Ytterdal, *Semiconductor Device Modeling for VLSI*, Englewood Cliffs, NJ: Prentice-Hall, 1993, ISBN # 0-13-805656-0.
- B. Leung, *VLSI for Wireless Communication*, Upper Saddle River, NJ: Prentice-Hall, 2002, ISBN # 0-13-861998-0.
- C. Mead, *Analog VLSI and Neural Systems*, ISBN # 0-201-05992-4.
- J. Milman and C. Halkias, *Integrated Electronics, Analog and Digital Circuits and Systems*, New York: McGraw-Hill Book Co., 1992, ISBN # 0-074-62245-5.
- Muroga, *Logic Design & Switching Theory*, Krieger Publishing Co., ISBN # 1-57524-036-X.
- J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits A Design Perspective*, 2nd edition, Upper Saddle River: NJ, Pearson Education, Inc., 2003, ISBN #0-13-597444-5.
- K. Roy and S. C. Prasad, *Low-Power CMOS VLSI Circuit Design*, New York: John Wiley & Sons, 2000, ISBN #0-471-11488-X.
- Masakazu Shoji, *CMOS Digital Circuit Technology.* Englewood Cliffs, NJ: Prentice Hall, 1988, ISBN # 0-13-138850-9.
- Michael John Sebastian Smith, *Application-Specific Integrated Circuits.* Reading, MA: Addison Wesley Longman, Inc., 1997, ISBN # 0-201-73357-9.
- S. M. Sze, *VLSI Technology*, second edition. New York: McGraw-Hill Book Co., 1988, 2nd Edition, ISBN # 0-07-062735-5.
- D. Thomas and P. Moorby, *The Verilog Hardware Description Language*, Boston: Kluwer Academic Publishers, 5th Edition, 2003, ISBN # 1-4020-7089-6.
- R. R. Troutman, *Latchup in CMOS Technology, The Problem and Its Cure.* Boston: Boston: Kluwer Academic Publishers, 1986, ISBN # 0-89838-215-7.
- J. P. Uyemura, *CMOS Logic Circuit Design*, Boston: Kluwer Academic Publishers, 1999, ISBN # 0-7923-8452-0.
- J. P. Uyemura, *Introduction to VLSI Circuits and Systems*, New York: John Wiley & Sons, 2002, ISBN # 0-471-12704-3.
- John F. Wakerley, *Digital Design Principles and Practices*, Prentice Hall.
- W. Wolf, *Modern VLSI Design System-on-Chip Design*, Upper Saddle River, NJ: Prentice-Hall, 2002, 3rd Edition, ISBN # 0-13-061970-1.
- K.-S. Yeo, S. S. Rofail, and W.-L. Goh, *CMOS/BiCMOS ULSI Low Voltage, Low Power*, Upper Saddle River, NJ: Prentice-Hall, 2002, ISBN # 0-13-032162-1.