RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
16:332:574 CAD Digital VLSI Design
Assignment V
Assigned: November 15, 2004
Due November 22, 2004

Reading Assignment: Chapter 6 of Weste and Harris.

No collaboration is permitted on this assignment. Your work must be your own. You must turn in these specific items for each question to receive credit:

- Cadence logic schematic.
- Cadence Verilog logic simulation.
- Cadence switch-level schematic.
- Cadence Spectre switch-level simulation.
- Cadence layout.
- Cadence Spectre mode simulation for the layout.

1. (**Dynamic Domino CMOS Logic Design.**) Implement the Boolean function

$$H = (A + (B \cdot C) + (E \cdot F) + G) \tag{1}$$

in CMOS dynamic n-Domino logic (see the schematic in Figure 6.28 (a)). Assume that when the clock ϕ is low, the logic output is precharging to logic 1 and when ϕ is high, the logic output is evaluating (this is done by the n-tree). ϕ is the only clock signal you will need. Keep in mind that the precharger is an p-FET and the evaluator is an n-block. Watch out for logic errors! Include an output inverter in this design. Turn in all of the things asked for at the start of this assignment. Would this gate be faster if it were implemented in p-Domino logic? If so, why? If not, why not?

2. (**Clocked Dynamic CMOS Logic.**) Implement the Boolean function

$$J = \overline{((A \cdot B) + C) \cdot (D + E + F) \cdot G} \tag{2}$$

as dynamic clocked CMOS logic C^2MOS. Turn in all of the things asked for at the start of this assignment.