Characteristics of the ITC'99 Benchmark Circuits

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Outline

- **Why Benchmark?**

- **Some History.**

- **Soliciting Benchmarks**

- **Benchmark Characteristics**

- **Next Steps**

- **Call for Participation**

Why Benchmark?

- **Current benchmarks are outdated - too simple, too small.**

- **Need widely available, modern designs to spur research on DFT.**

- **Benchmarks foster innovation by:**

  - **Focusing research on most valuable topics.**

  - **Allowing better sharing, comparison of research results.**

  - **Encouraging healthy competition.**

- **We want to help university innovation on DFT and ATPG to catch up to and outpace industry.**

Goals

- **Get large, realistic designs.**

- **Designs should have:**
  - **Memories**
  - **Multiple clock domains**
  - **Internal tristate busses**
  - **Inouts**
  - **Reasonable number of gates and FFs.**
  - **RTL and/or Behavioral Descriptions**

Goals (2)

- **Test Methods Targeted:**

  – **Non-scan sequential ATPG**

  – **RTL and Behavioral Level ATPG**

  – **RTL and Behavioral Level DFT**

  – **Theoretical Fundamentals of ATPG for circuits with realistic features.**

- **Not Targeted**

  – **Full scan DFT**

  – **Combinational ATPG**

- **Not Targeted Yet**

  – **Realistic fault and defect models.**

History

- **First call for benchmarks made at 1998 ITSW.**

- **Support from ITC Program Committee in 1998 meetings.**

- **Website set up - http://www.cerc.utexas.edu/itc99-benchmarks/bench.html**

- **Effort made an official activity of TTTC - Scott Davidson vice Chair of Test Synthesis TAC.**

- **Mailing list set up - 150 members so far.**

- **Meeting held at ITC'98.**

- **Coordinating with SRC/Sematech benchmark effort - meeting held at ICCAD, November 1998**

Soliciting for Benchmarks

- **Done using Mailing List**

- **Done at ITC.**

- **Guidelines**

  - **Anonymity for companies**

  - **No support required!**

  - **Signal names disguised. Functionality can be broken.**

  - **We took what they had.**

- **Best candidates - cancelled chips, obsolete products.**

- **It turned out that universities had some good stuff too.**

The Benchmarks

- **Three circuits from industry**

    - **Two real ASICs**

    - **One module of a real design.**

- **Two designs from universities**

    - **Torch - a MIPS-like processor from Stanford**

    - **CMUDSP - Based on the Motorola DSP56002.**

- **One odd combinational circuit.**

- **22 RTL circuits from Politecnico di Torino**

- **3 RTL versions of small ISCAS89 Benchmarks from U. Mich.**

I99-1

- **5 - 6 K gates.**

- **2 phase latch design**

- **5 input mux driven by complementary enables.**

- **Gate level Verilog**

- **I/Os**

    - **120 Inputs**

    - **250 Outputs**

    - **14 Inouts**

- **Primitive based library**

I99-2

- **Industrial ASIC, approx 20 K gates**

- **LSI Logic Library used - Verilog models included.**

- **Datapath design.**

- **Four phase clock**

- **Several internal tristate busses, no memories**

- **Gate level Verilog netlist.**

- **No scan - (ad hoc DFT)**

- **I/Os**

  - **31 Inputs**

  - **88 Outputs**

  - **176 Inouts**

I99-3

- **Industrial ASIC**

- **Gate level Verilog, Mitsubishi Library**

- **Several clock domains**

- **Several FIFOs, RAMs**

- **Includes fully compliant boundary scan, internal scan.**

- **I/Os**
    - **72 Inputs**
    - **32 Outputs**
    - **30 Inouts**

- **Looking for RTL version.**

- **Needs some work before ready for release.**

I99-4 - The Torch Processor

- **Developed at Stanford - see http://www-flash.Stanford.EDU/torch/**

- **Superset of MIPS R2000/R3000 instruction set.**

- **RTL level Verilog**

- **Set of test vectors and simulators included.**

- **No Scan**

- **I/Os**

  - **30 Inputs**

  - **12 Outputs**

  - **96 Inouts**

I99-5 - CMUDSP

- **Subset of Motorola DSP56002, crippled to be non-commercial.**

- **Code and some documentation available at**

  http://www.ece.cmu.edu/~lowpower/benchmarks.html

- **Behavioral level and Structural Verilog available.**

- **Scan inserted at Structural Verilog level. Need volunteer to remove it.**

- **Gate count - 14,550. Internal memories included.**

- **Not fully debugged yet, but should be fine for ATPG and DFT.**

- **Proprietary library referenced in RTL. Needs to be mapped.**

I99T<1-22> - Torino Benchmarks

- **22 sequential benchmarks in RTL (VHDL) and gate level (EDIF)**

- **Sizes range from 45 gates, 5 FFs to 98,000 gates and 6600 flip-flops.**

- **Larger designs are compositions of smaller designs.**

- **Designs are single clock, no Inouts, no tristate busses, no memories.**

- **Primitive library - self contained.**

- **See link from ITC99 benchmark page for more details.**

I99S<n>

- **RTL Versions of ISCAS Benchmarks, in Verilog**

- **From University of Michigan (Mark Hansen)**

- **Location: http://www.eecs.umich.edu/~mhansen/imodels/ISCAS_HLM.htm**

- **4 combinational benchmarks, 3 sequential (s208.1, s298 and s344/s349)**

  – **Also 4 74xxx circuits in Verilog (adder, ALU, etc.)**

- **Page also includes block diagrams of the benchmarks.**

I99C1

- **Combinational circuit, extracted from an industrial design.**

- **Gate level netlist, using generic library.**

  - **I have translated it to Verilog. Translation unverified as of yet.**

- **Vectors included.**

- **First stab does give low fault coverage (high efficiency) with an industrial ATPG**

  - **Library not verified. Results inconclusive.**

- **I/Os**

  - **128 Inputs**

  - **8 Outputs**

A New Hope

- **Sun has announced open source Microprocessors!**

    – **Actually Community Source Licensing**

- **Goal is to allow start-ups to design before paying royalties.**

- **Registration procedure will be required.**

- **Processors are:**

    – **picoJava core - end of March**

    – **32 bit Sparc V.8 - end of Summer**

    – **64 bit SparcV.9 - end of Year.**

- **See http://www.sun.com/990302/scsl/**

Next Steps

- **Clean up circuits requiring more work.**

- **Publicity (press release).**

- **Translate libraries needing translation.**

- **Close on standard Library**

- **Define presenters at ITC'99 session.**
  - **Need ground rules for presentations.**
  - **No one is expected to do them all!**

- **Later, we should lay out some of these, to allow defect level test work.**

- **We will also look for more benchmarks.**

Call for Participation

- **Need help in:**

- **Characterizing the Benchmarks**

- **Synthesizing Torch, CMUDSP**

- **Library Mapping.**

- **Web page design - registration and downloads.**

- **Volunteers to run the benchmarks with your tools.**

- **Presenting the Results:**

- **Panel format at ITC99 - Sept. 30, afternoon**

- **Proposal submitted to Design & Test for special issue in 2000.**

- **Many papers thereafter.**

- **Who will be First?**