RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
16:332:574 CAD Digital VLSI Design
Assignment IX
Assigned: December 8, 2006
Due December 13, 2006

Reading Assignment: Review Chapter 4 in Weste and Harris.
No collaboration is permitted on this assignment. Your work must be your own.

1. (**Elmore Delay.**) Find the worst-case Elmore parasitic delay of an n-input NOR gate.

2. (**Logical Effort.**) Design a circuit at the gate level to compute the following function:

```
if (a == b) y = a;
else y = 0;
```

   Let a, b, and y be 16-bit busses. Assume the input and output capacitances are each 10 units. Your goal is to make the circuit as fast as possible. Estimate the delay in FO4 inverter delays using Logical Effort if the best gate sizes were used. What sizes do you need to use to achieve this delay?