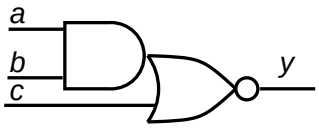
RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
16:332:574 CAD Digital VLSI Design
Assignment VIII
Assigned: December 4, 2006
Due December 8, 2006

Reading Assignment: Study the test generation slides for the course.
No collaboration is permitted on this assignment. Your work must be your own.

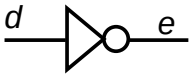
1. (**Test Pattern Generation.**) Calculate the test patterns for each of the three following circuits, and use the table format provided.

   (a) First circuit:



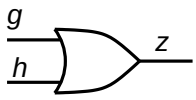
		Input Pattern			Output Response
		a	b	c	y
a	sa0				
	sa1				
b	sa0				
	sa1				
c	sa0				
	sa1				
y	sa0				
	sa1				

   (b) Second circuit:



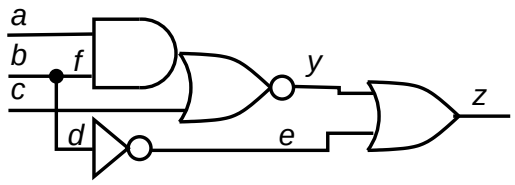
		Input Pattern	Output Response
		d	e
d	sa0		
	sa1		
e	sa0		
	sa1		

(c) Third circuit:



		Input Pattern		Output Response
		f	g	z
f	sa0			
	sa1			
g	sa0			
	sa1			
z	sa0			
	sa1			

2. (**Test Pattern Generation.**) Now calculate the tests for the circuit that combines these three circuits, using the table provided. Why aren't all of the input and output faults of the three subcircuits still testable? Write an essay proposing a solution to this problem. This example illustrates why separately testable subcircuits cannot simply be combined into a more complex circuit, with their testability preserved.



		Input Pattern			Output Response
		a	b	c	z
a	sa0				
	sa1				
b	sa0				
	sa1				
c	sa0				
	sa1				
y	sa0				
	sa1				
d	sa0				
	sa1				
e	sa0				
	sa1				
f	sa0				
	sa1				
g	sa0				
	sa1				
z	sa0				
	sa1				