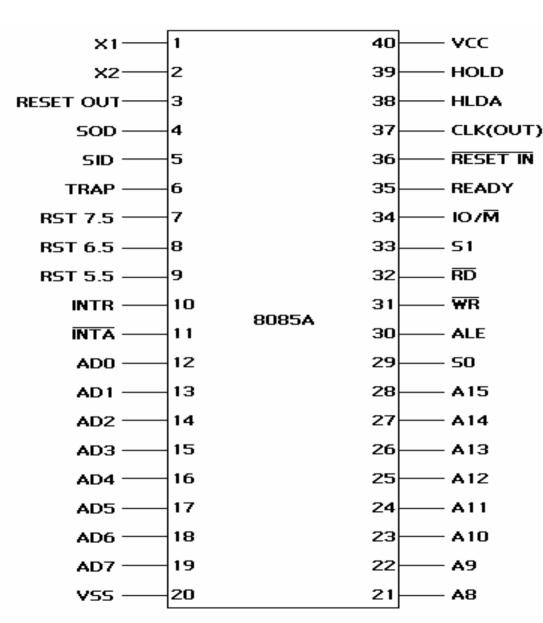
# Designing a counter

O to 99 seconds.



#### 8085 Microprocessor chip



Pin Configuration of 8085A Microprocessor

Signals of 8085 can be classified as:-

- Address bus-A<sub>15</sub>-A<sub>8,</sub>
- Data bus-AD<sub>7</sub>-AD<sub>0</sub>
- Control and Status signal-

ALE RD'

WR' IO/M'

 $S_1$   $S_0$ 

 Power supply and frequency signal-

 $V_{SS}$   $V_{CC}$ 

 $X_1$   $X_2$ 

CLK RESET IN'

**RESET OUT** 

Externally initiated signal-

INTR INTA'

TRAP RST 7.5

RST 6.5 RST 5.5

HOLD HLDA

READY

Serial I/O ports-

SID

SOD

## Basic concept of how 8085 works

The three main operations are:-

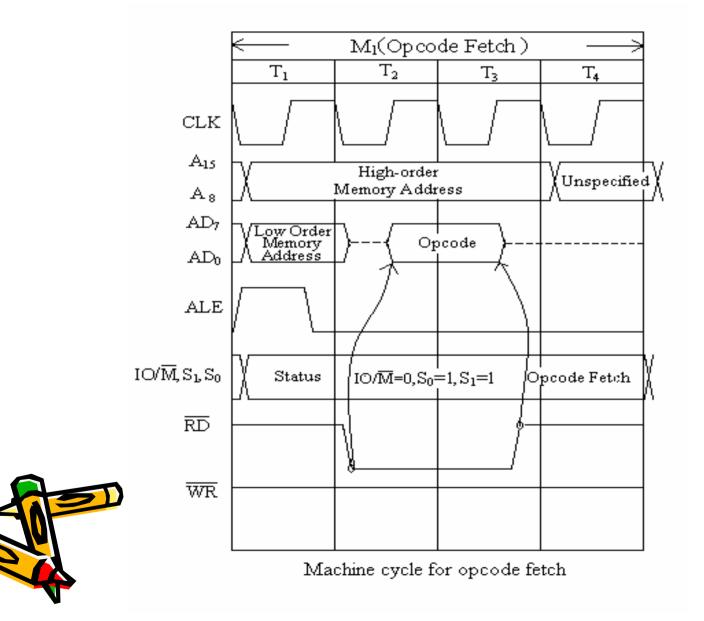
Opcode Fetch

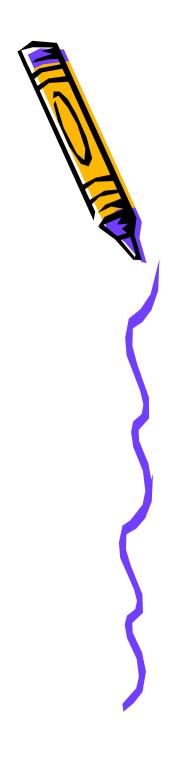
Memory Read

Memory Write

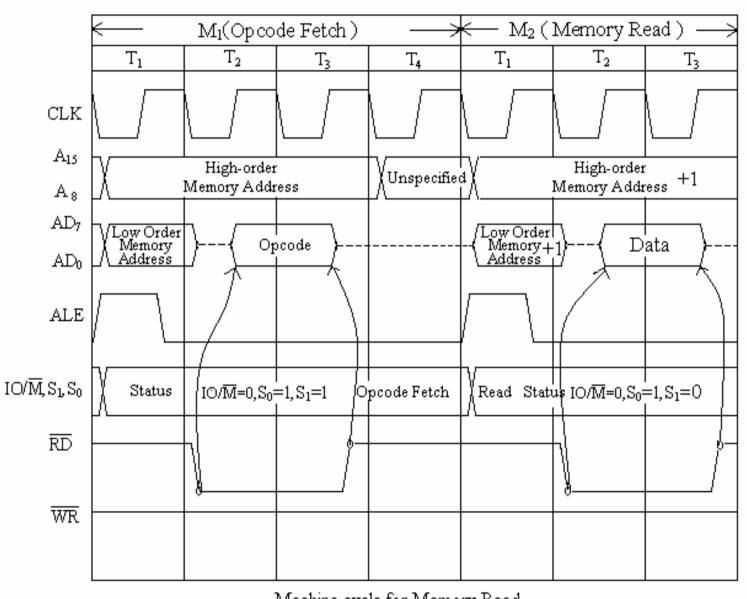


#### Opcode Fetch





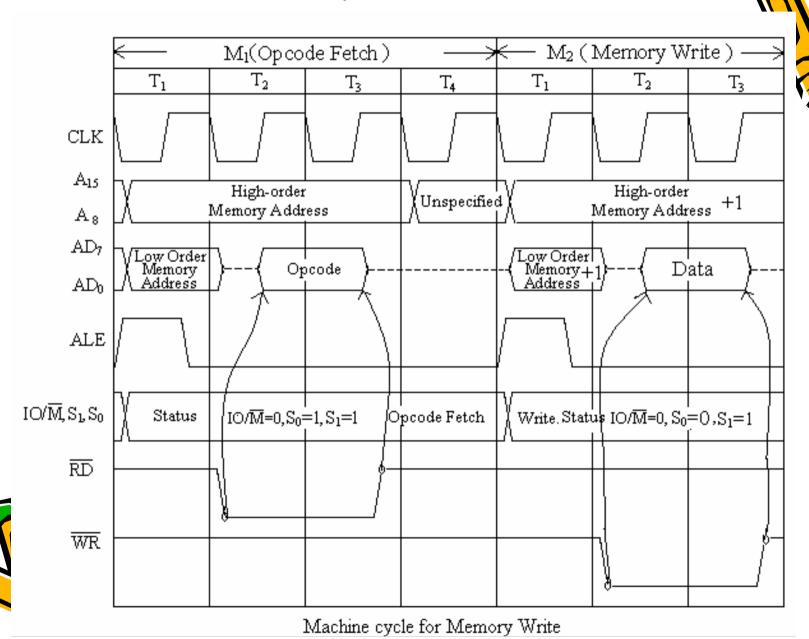
#### Memory Read





Machine cycle for Memory Read

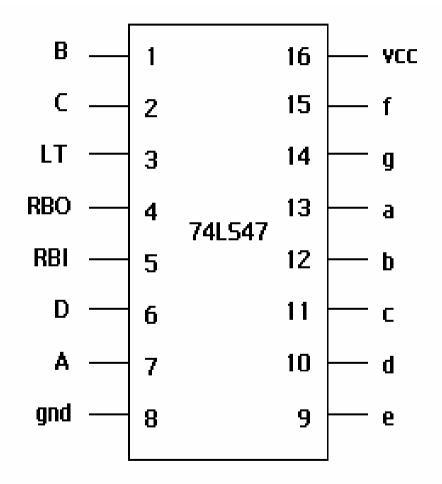
#### Memory Write



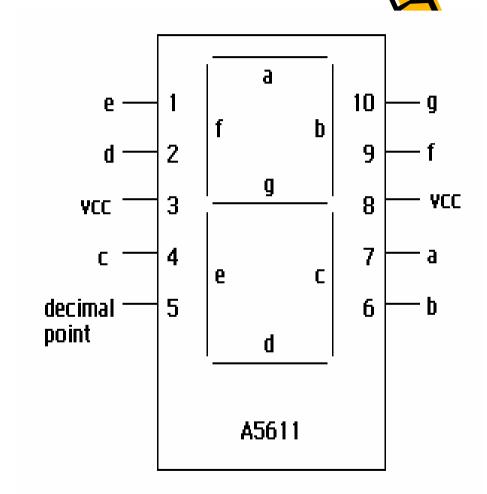
8255 Programmable Peripheral Interfacing Chi

PA3 ——1		40				
PA22		39 PA5	C:			
PA13		38 PA6	Signals of 8255			
PAO4		37—— PA7				
RD5		36 WR	<ul> <li>Control signals-</li> </ul>			
<u> </u>		35 RESET	RD' WR'			
GND7		34 DO	$CS' A_0 A$			
A1 ——8		33D1				
A0 ——9		32 D2	RESET			
PC7 —— 10		31 D3	<ul> <li>Data lines-</li> </ul>			
PC6 ——11	8255A	30 D4	$D_7\text{-}D_0$			
PC5 ——12		29—— D5	<ul> <li>I/O Port Lines-</li> </ul>			
PC4 ——13		28 D6	Port A - PA7-PA0			
PCO ——14		27 D7	Port B - PB <sub>7</sub> -PB <sub>0</sub>			
PC1 ——15		26 — VCC	,			
PC2 ——16		25 PB7	Port $C - PC_7 - PC_0$			
PC3 ——17		24 PB6	<ul> <li>Power supply-</li> </ul>			
PB0 ——18		23—— PB5	GND V <sub>cc</sub>			
PB1 ——19		22 PB4				
PB220		21 —— PB3				

#### 7-Segment Decoder/Driver and 7-Segment Disp



Pin Diagram of 74LS47, BCD to 7-Segment Decoder/Driver

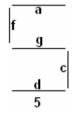


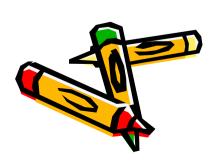
Pin Diagram of A5611, Common Anode 7-Segment Display

#### NUMERICAL REPRESENTATION ON THE SEVEN-SEGMENT DISPLAY

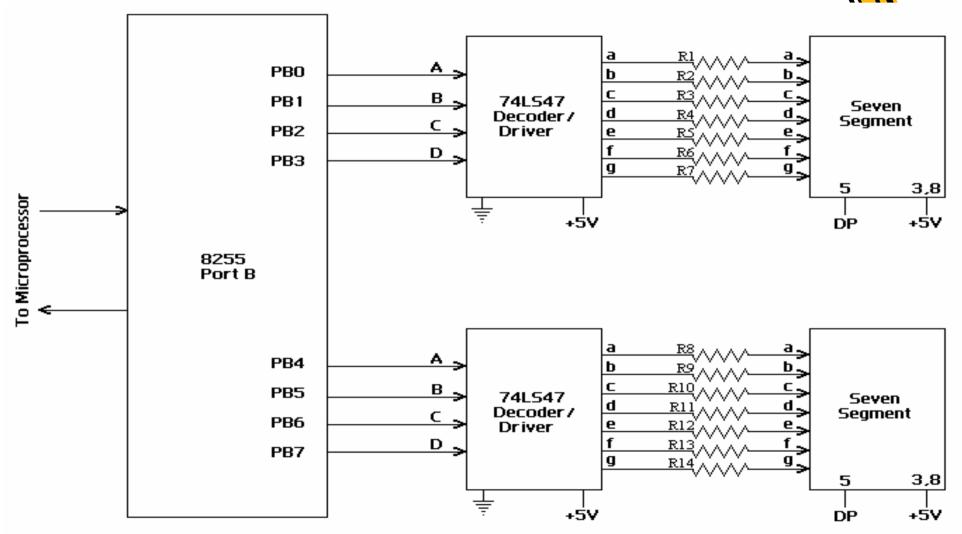






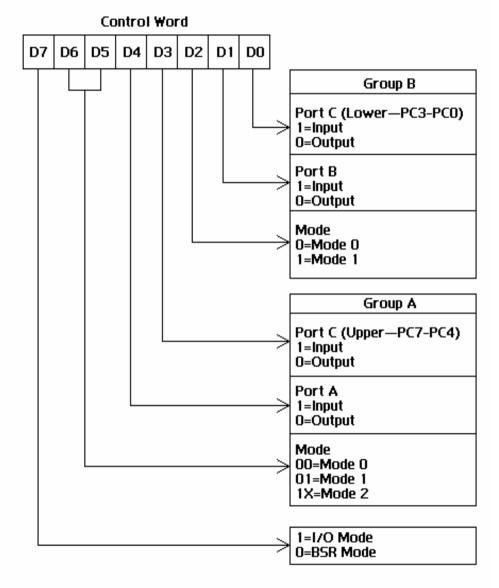


# Interfacing the 8255 with the 7-Segment Decoder/Driver and the 7-segment Display



R1-R14- Resistence of 220ohms

#### The control word of the 8255



8255 Control Word Format

How to design the control word

Example:-

8255 in I/O Mode

Port A-Input

Port B-Output

Port C(Upper)-Output

Port C(Lower)-Input

Port A-Mode 1

Port B-Mode O

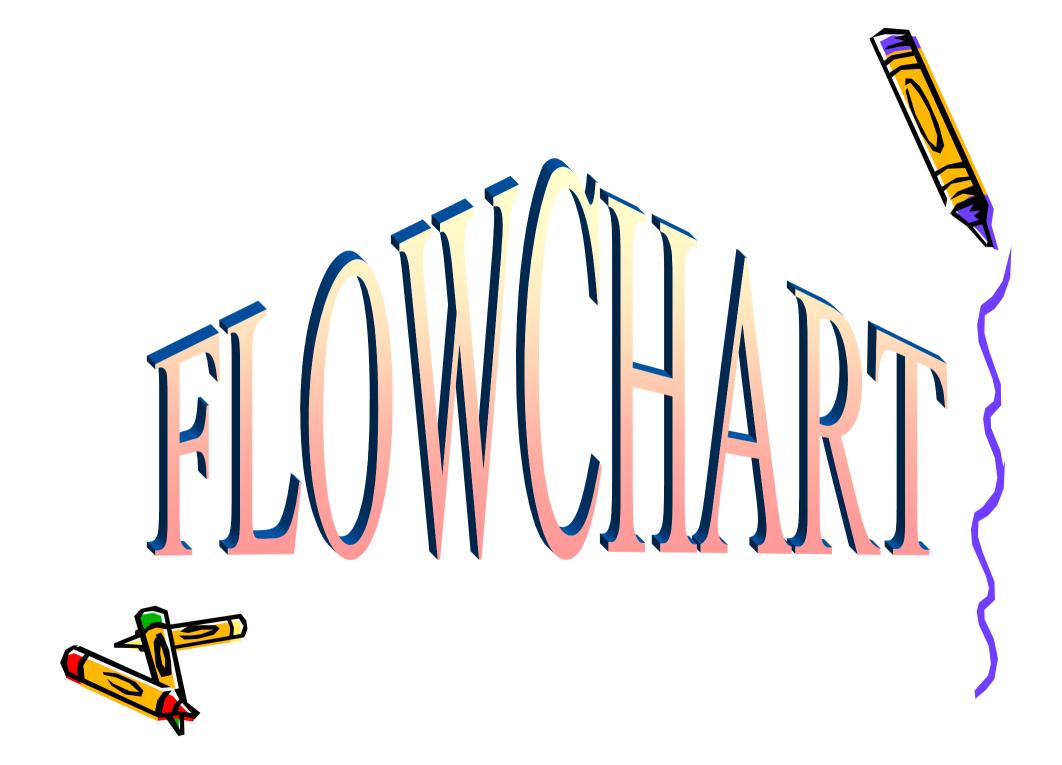
So the control word is:-

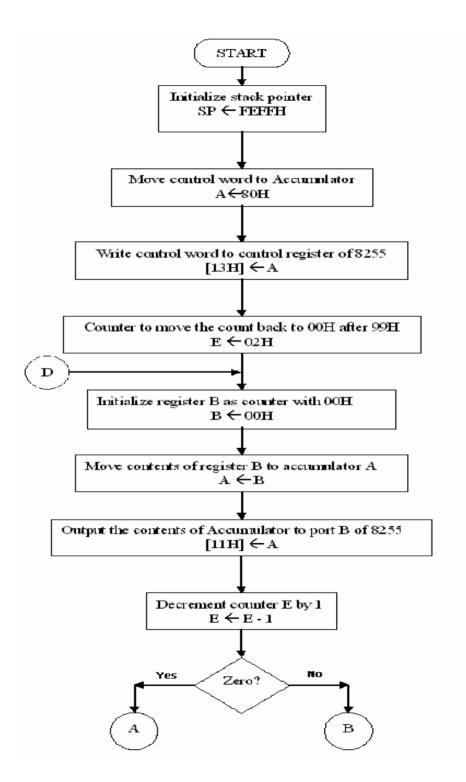
 $D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$ 1 0 1 1 0 0 0 1 = B1H

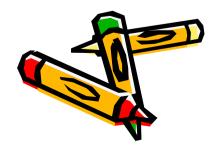
To write it in the control register:-

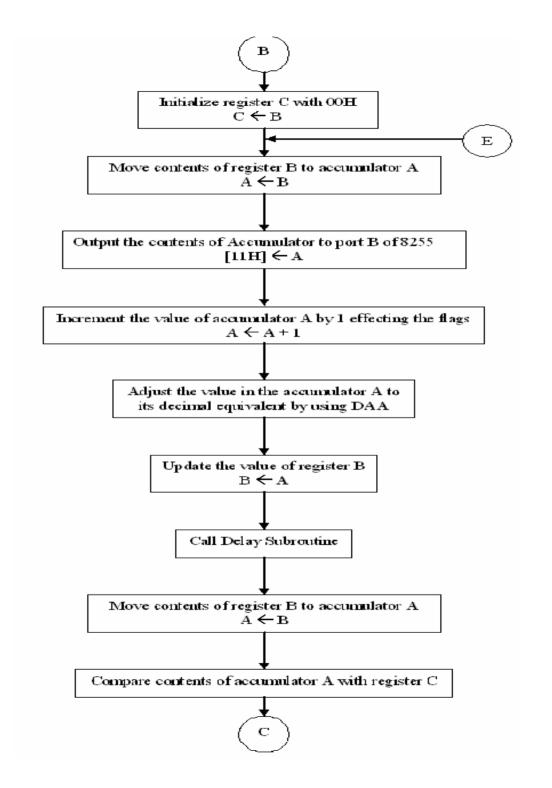
MVI A,B1H OUT 13H

HLT

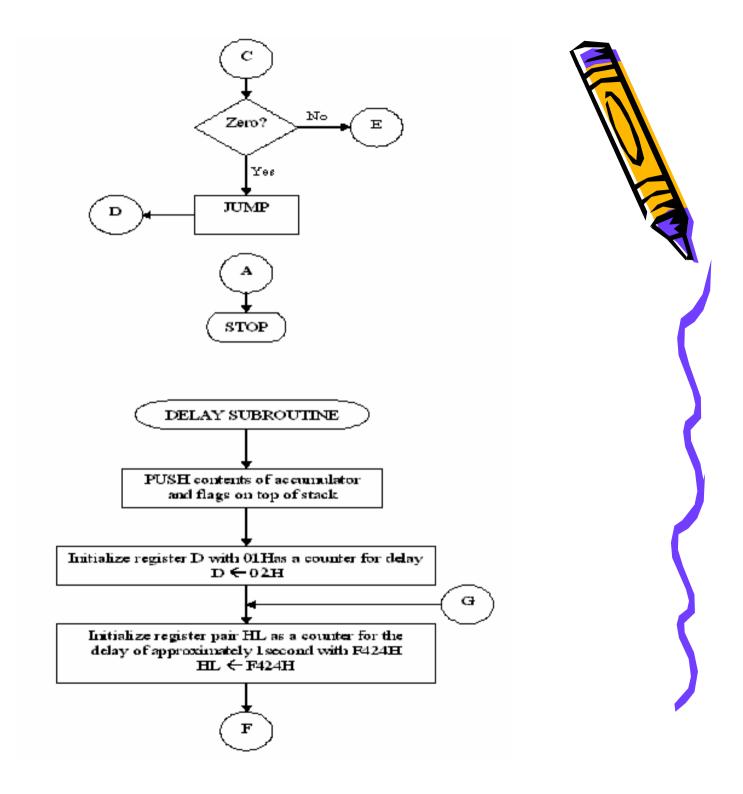




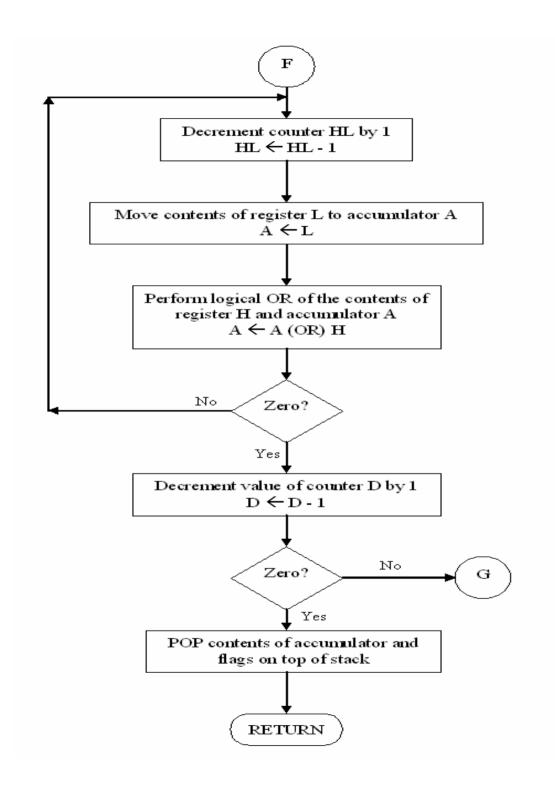














#### PROGRAM

#### Main

LXI SP.FEFFH

MVI A,80H

OUT 13H

MVIE,02H

LBL: MVIB,00H

MOV A,B

OUT 11H

DCR B

JZ STP

MOV C.B

LOOP: MOV A,B

OUT 11H

ADI 01H

DAA

MOV B,A

CALL DELAY

MOV A.B

CMP C

JNZ LOOP

ЛМР LBL

STP: HLT



DELAY: PUSH PSW

MVID,02H

LOOP2: LXI H,F424H

LOOP1: DCXH

MOVAL

ORA H

JNZ LOOP1

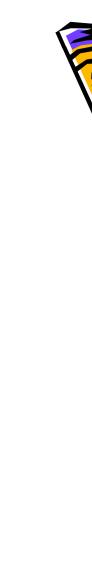
DCR D

JNZ LOOP2

POP PSW

RET



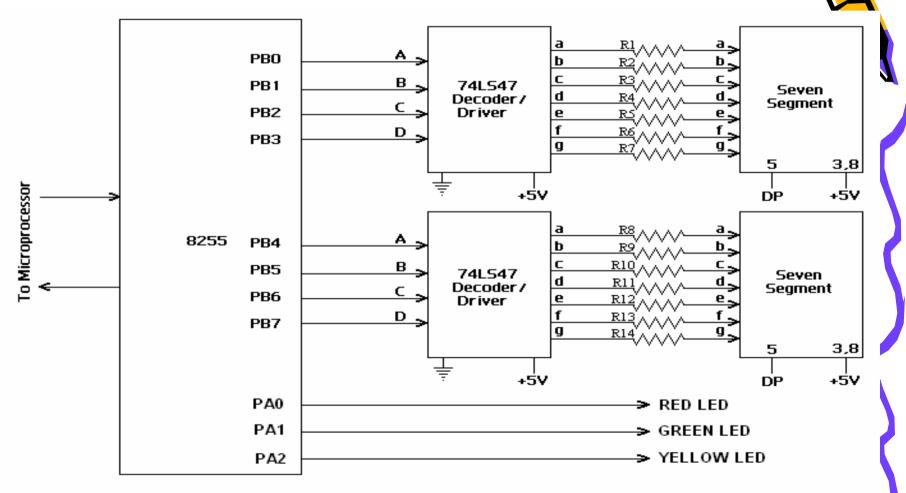


# One of the application of this counter

# Controlling the Traffic Signal Lighting



## Interfacing the 8255 with the 7-Segment Decoder/Diversity the 7-segment Display along with the lights





R1-R14- Resistence of 220ohms

### PROGAM FOR CONTROLLING THE TRAFFIC LIGHTS

RET

Main		Subroutine Count		
	LXI SP,FEFFH			PUSH PSW
	MVI A,80H			MVIE.02H
	OUT 13H		LBL:	MVIB,00H
LOOP3:	MVI A,01H			M≎V A,B
	OUT 10H			OUT 11H
	CALL COUNT			DCRE
	MVI A,02H			JZ STP
	OUT 10H			MOV C,B
	CALL COUNT		LOOP:	MOV A.B
	MVI A,04H			OUT 11H
	OUT 10H			ADI 01H
	CALL DELAY			DAA MOVB,A
	CALL DELAY			CALL DELAY MOV AB
	CALL DELAY			CMP C
				JNZ LOOP
	CALL DELAY			JMP LBL
	JMP LOOP3		STP:	POP PSW

HLT

#### Suroutine Delay

DELAY: PUSH PSW

MVID,02H

LOOP2: LXI H,F424H

LOOP1: DCXH

MOV AL

ORAH

JNZ LOOP1

DCR D

JNZ LOOP2

POPPSW

RET

### Acknowledgement:-

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    - Prof. Raj Kumar Panda, Department of Computer Science, Vidyasagar College
- \*Mr. Sourov Saha, Department of Computer Science, Vidyasagar College
- Mr. Bijon Kumar Pal, Department of Computer Science, Vidyagar College
  - \* Mrs. Nilima Das

# Thank You I



Presented By:-

Moumita Guha Roy Dipendu Ghosh

