RUTGERS UNIVERSITY
Department of Electrical and Computer Engineering
332:574 CAD Digital VLSI Design
Project Status Report and Deadlines
November 28, 2005

332:574													
Project	Activity, Due Date, and Grade Penalty												
	Project Pro-Posal	Power Est.	Block Diag.	Work Assign.	Revised Block Diagram	Spec. & Block. Diagram &	Verilog Desc.	Short Proj.	Logic Sch. & Sim.	Logic Sim. with Frame	ATPG Results	Project Presentations	Interim Project Report
DUE	9/15	9/20	9/20	9/27	10/4	10/22	12/8	11/10	12/5	12/12	12/8	12/13	12/13
PENALTY	A→B+	B+→B	B→C+	C+→C	C→D+	D+→D	D→F+	F+→F	F→F	F→F	A→F	A→F	A→F
HDTV Receiver SoC													
Varadan Savulimedu	A	A	A	A	A	A	A	A					