```
module binary(y,x);
  input [31:0] x;
  output [31:0] y;
  reg [31:0] y1;
  reg [31:0] mul;
   reg [31:0] binval;
  reg[31:0] i=0;
 reg[31:0] count;

  always@(x) begin
    y1=0;
    mul=25;
    binval=0;

    while(mul>0)begin
      binval[i]= (mul%2);
      mul=mul/2;
      i=i+1;
    end



   for(count=0;count<i;count=count+1)
   begin
 if(binval[count]==1)begin
      y1=y1+(x<<(count));
   end

 end

  end
  assign y=y1;

endmodule
```