Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 5th Semester Mid Semester Examination, September, 2023

Computer Architecture and Organization II (CS-3103)

Full Marks: 30 Time: 2 hours

Answer all questions

1A) What do you mean by structural hazard in instruction pipeline? Consider following program segment

i1 : R10 ← Memory(205)
i2 : R12 ← R10
i3 : R10 ← R10 + 1
i4 : R12 ← R12 * R10
i5 : Memory(205) ← R10

Indicate the cases of structural hazards if only one copy of each functional unit is available in CPU. 4

B) Define branch *delay slot* . Follow execution of the program segment (given below) in a 4-stage (IF, ID, OF, EX) pipeline.

```
L1: LOAD R10,M(R12)
    SUB R13, R13, R10
    BNEZ L1
    STORE R14,M(R13)
```

i) Identify the branch delay slot.
ii) Suggest solutions to manage the branch delay slot. 6

2A) Define EREW and CRCW SIMD computer. Describe the method of broadcasting a message x in such computers. Estimate the worst case search time to find the element x from a table of N elements in (i) EREW; (ii) CRCW SIMD computer. 6

B) Design a shuffle-exchange interconnection network for an SIMD machine with 8 processing elements PE0 to PE7. Find the number of shuffle/exchange operations needed to transfer an information from PE1 to PE7. 4

3A) Following nested loop is in execution. Elements of matrix A are stored in row major order in memory. Show how cache misses for A can be reduced by loop interchange technique. 4

```
for j=1 to 10 with incr 1
   for i=1 to 20 with incr 1
      A[i][j] = 2*B[j][1];
```

B) Define Write-Invalidate and Write-Update protocol in cache coherence. Identify the events - (read/ write) hit/miss that occurred for the sequence of operations (1) to (6)

(1) P 1 reads X; (2) P 2 reads X; (3) P 2 updates X=5; (4) P 2 reads X;
(5) P 1 updates X=20; (6) P 2 reads X.

also find the value of X at main memory (M), Cache 1 and Cache 2 in a system with two processors P1 (with Cache 1) and P2 (with Cache 2) and bus-based shared main memory (M), after each operation in a Write-Invalidate and Write-Update protocol. 6

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