Blank Quiz

Total points 8/10

1. The series of branch outcomes stored in an 1-bit prediction buffer is 10101010 (1 represents taken branch and 0 is for untaken branch). When the predictor is initialized as 0 then the number of mispredictions is

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✓ Untitled Question 2/2

- ○ 1
- ○ 4
- ◉ 8 ✓
- ○ 2

✓ 2. Let consider execution in a pipeline system, realizing conventional 2-bit prediction scheme for branch control instructions of the following program segment consisting of three consecutive loops L1 (of 1000 iterations), L2 (of 100 iterations) and L3 (of 10 iterations) in sequence. That is, L3 follows L2 and L2 follows L1. The content of 2-bit prediction counter, when execution of L2/L3 is started, is 2/2

- ○ Not known
- ◉ 10/10 ✓
- ○ 00/00
- ○ 10/11

✓ 3. Let consider execution of the program segment: I1: R1 = Memory(A); I2: R2 = R2 + R1; I3: R3 = R3 + R4; I4: R4 = R4 * R5. The dependencies between I1 and I2, I2 and I3, and I3 and I4 are 2/2

- (●) RAW, None, WAR ✓
- ( ) WAR, None, RAW
- ( ) None of the options given
- ( ) WAR, WAW, RAW

✓ 4. In a 6-stage instruction pipelined processor, to avoid structural hazard, stalls are introduced. The average number of stall cycles required per instruction is 1. The speedup in this pipelined processor is, therefore, 2/2

- (●) 3 ✓
- ( ) 6
- ( ) 1
- ( ) 2

✗ 5. The solution for handling out-of-order exceptions in k-stage instruction pipeline, a status vector register SVi is associated with each instruction. N types of exceptions can be possible in the system. The minimum number of status vectors required for this system is, therefore, 0/2

- ○ k-1
- ○ N+1
- ◉ N ✗
- ○ k

Correct answer

- ◉ k