4-12-15

Indian Institute of Engineering Science and Technology, Shibpur
B. E. Part-III (CST) 5th Semester Examinations, 2015

Subject: Computer Architecture and Organization II — Paper: CS-504
Time: 3 hours — Full marks: 70

Answer any four

1 a) Differentiate among the RAW, WAR and WAW data hazard types. 7.5
b) Consider the following code sequence: 7

SW 512(R0), R3; => M[512] <-- R3
LW R1, 1024(R0); => R1 <-- M[1024]
LW R2, 512(R0); => R2 <-- M[512]

Identify the cases of possible data hazard (RAW/WAR/WAW).

c) Define branch delay slot. 3

2 a) Define compulsory, conflict and capacity miss? 6
b) In a system, the cache size (volume of cache interfaced) is 1MB; memory block size is 16KB. If cache size of the system is increased to 2MB, keeping all other components/parameters intact, then clarify its impact on compulsory/conflict/capacity miss. 6

c) A program accesses each element of a 64 x 64 matrix 16 times in course of its execution. The data cache can accommodate 1024 matrix elements and 64 matrix elements per block/page. How many compulsory data cache misses occur during the program execution? 5.5

3 a) Describe snoopy protocol based on the write-invalidate policy, implemented to enforce cache coherence in a multiprocessor system. 7
b) Consider a dual-processor (P1 and P2) system. Each processor having its own direct mapped private cache (C1 and C2), flushed (empty) initially, of two page size. The main memory MM is shared. The system follows write-through cache policy and snoopy protocol for maintaining cache coherence. Consider the following sequence of page references, where bold face page numbers represent write to page and the remaining are for read

Time step ::	1	2	3	4	5	6	7	8
Processor 1:	0	**0**	1	0	1	**1**	2	0
Processor 2:	0	**1**	0	1	0	**2**	2	3

Show traces of the execution of references by two processors indicating hits in C1 and C2 when the system follows
i) Write-invalidate policy; ii) Write-update policy. 7

c) Describe in brief the loop interchange technique to reduce cache miss rate. 3.5

4 a) Indicate the basic features of an ERCW shared memory SIMD computer. Describe method of broadcasting a message in such an SIMD computer. 6
b) A table T contains n elements. Estimate the worst case search time to find an element x from T in (i) ERCW; (ii) CREW SIMD computer. 6
c) Define the function of a 2x2 crossbar switch. Construct an 1x8 demultiplexer using 2x2 crossbar switches. 5.5

5 a) Describe, in brief, the architecture of a static data flow machine. Explain the basic differences between static and dynamic data flow computation model. 7

b) Define execution in a VLIW architecture of degree 3. Explain the differences between superscalar and VLIW architectures in terms of hardware requirement. 7

c) State a methodology for handling out-of-order exceptions in instruction pipeline. 3.5

6 a) Distinguish between UMA and NUMA. 6

b) What is loop unrolling? How does it help in ILP? -Explain with an example. 6

c) What is `data speculation'? Describe a data value prediction scheme. 5.5

7. Write short notes on the following 10+7.5

a) RAID 5 and RAID 6.

b) 1-bit and 2-bit prediction schemes.

P8/2