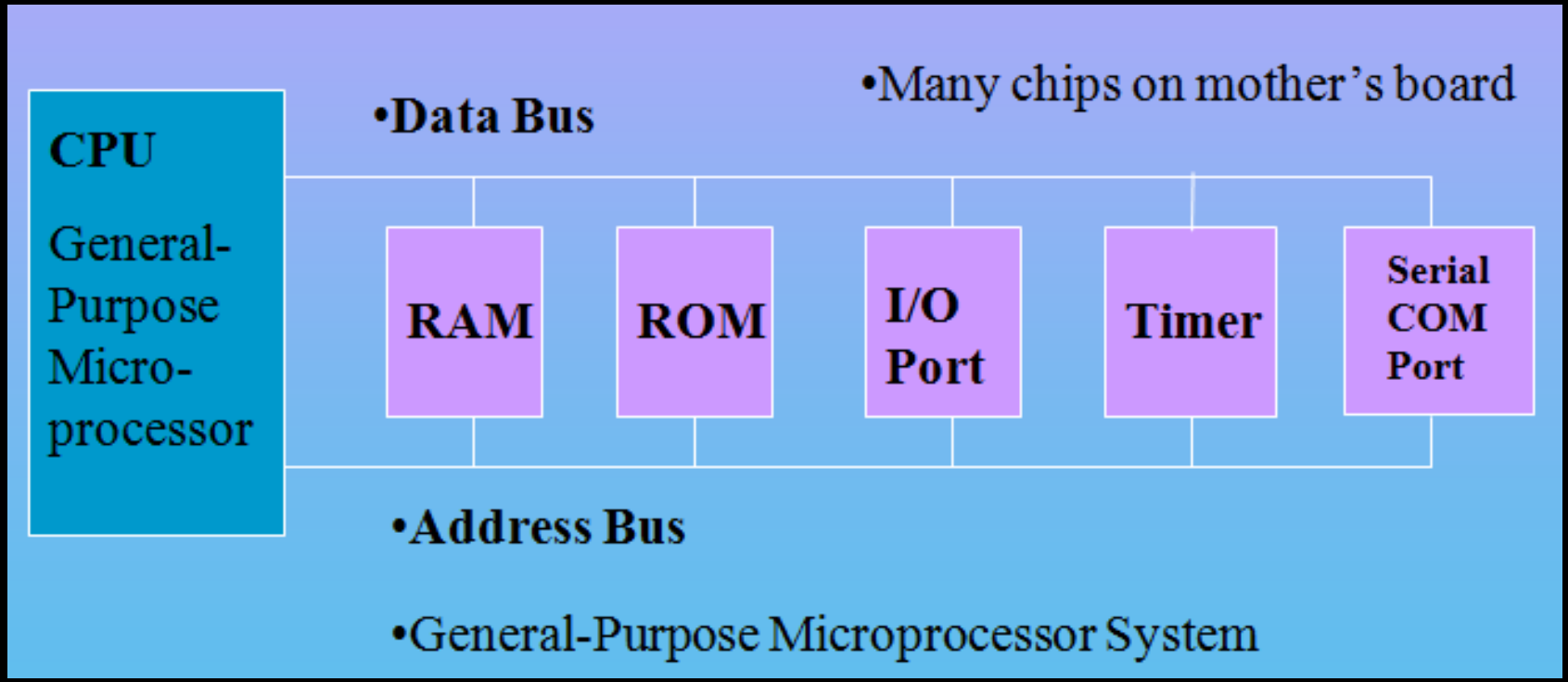
8051 Microcontroller

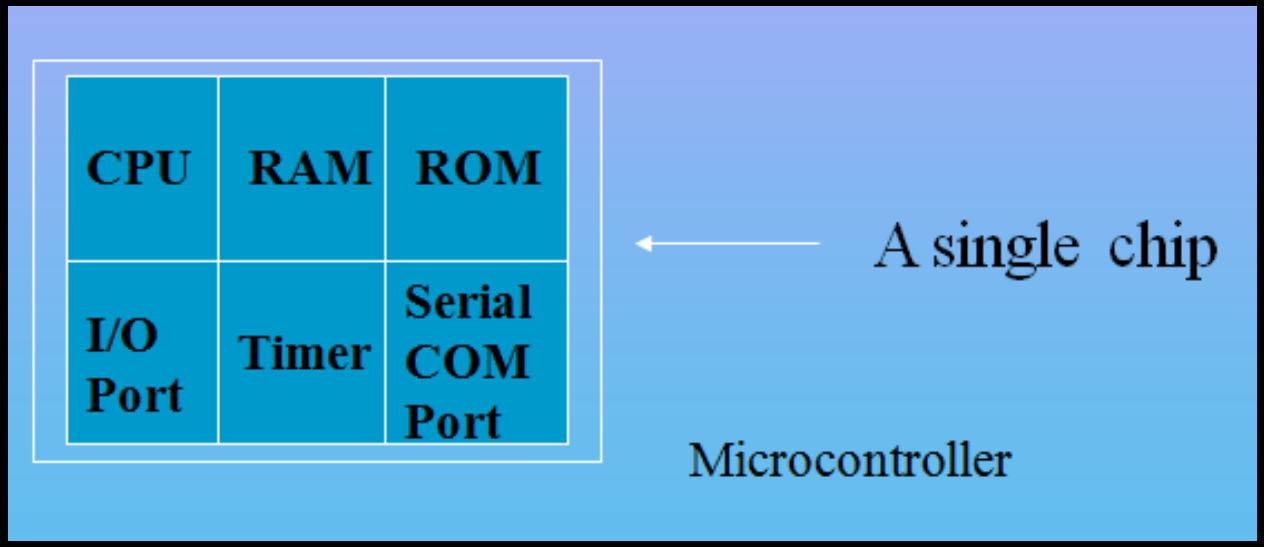
Microprocessor Based System

CPU
External RAM, ROM, I/O
(No internal RAM, ROM, I/O ports in the CPU)



Microcontroller

- A smaller computer on a CHIP
- On-chip RAM, ROM, I/O Ports, Timer, Serial Controller…
- Example: Motorola’s 6811, Intel’s 8051, Atmel 32



Microprocessor vs. Microcontroller

Microprocessor

- CPU is stand-alone, RAM, ROM, I/O, timer are separate
- Designer can decide on the amount of ROM, RAM and I/O ports.
- Expansive
- Versatility
- General-purpose

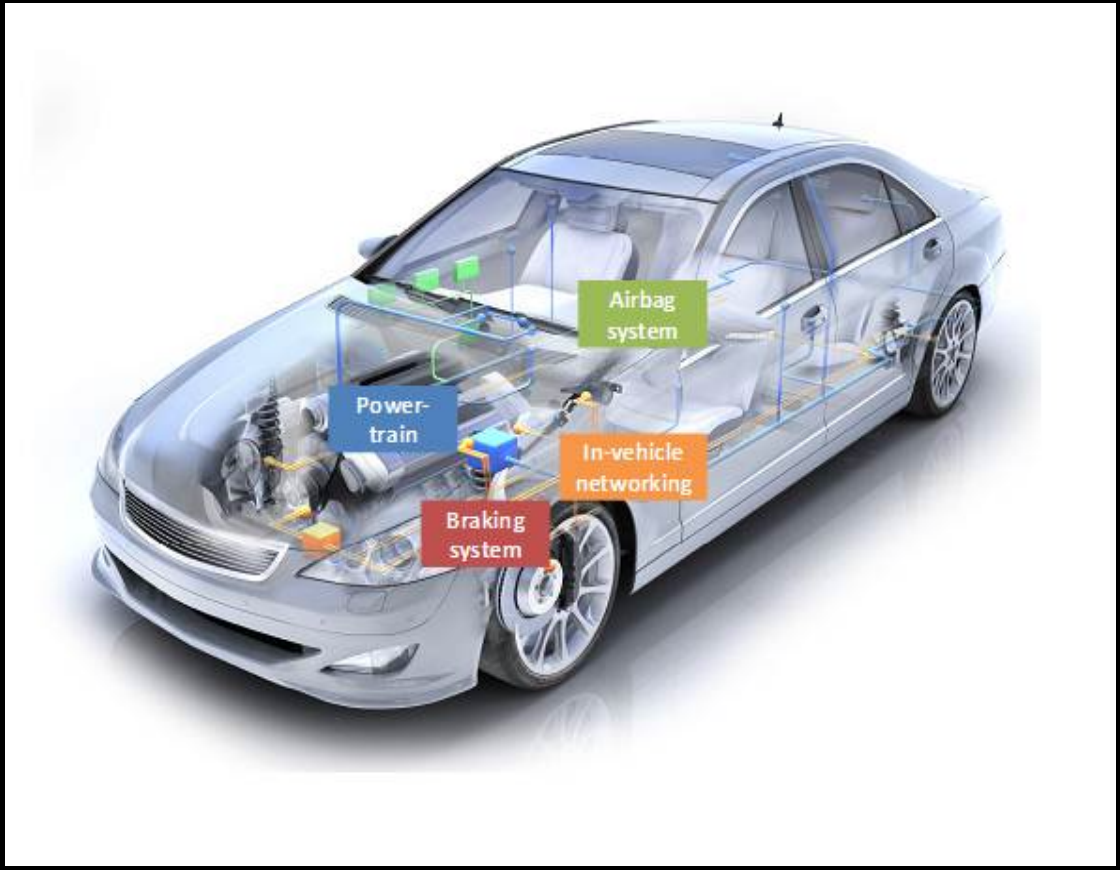
Microcontroller

- CPU, RAM, ROM, I/O and timer are all on a single chip
- Fixed amount of on-chip ROM, RAM, I/O ports
- Not Expansive
- Single-purpose
- Special Purpose.

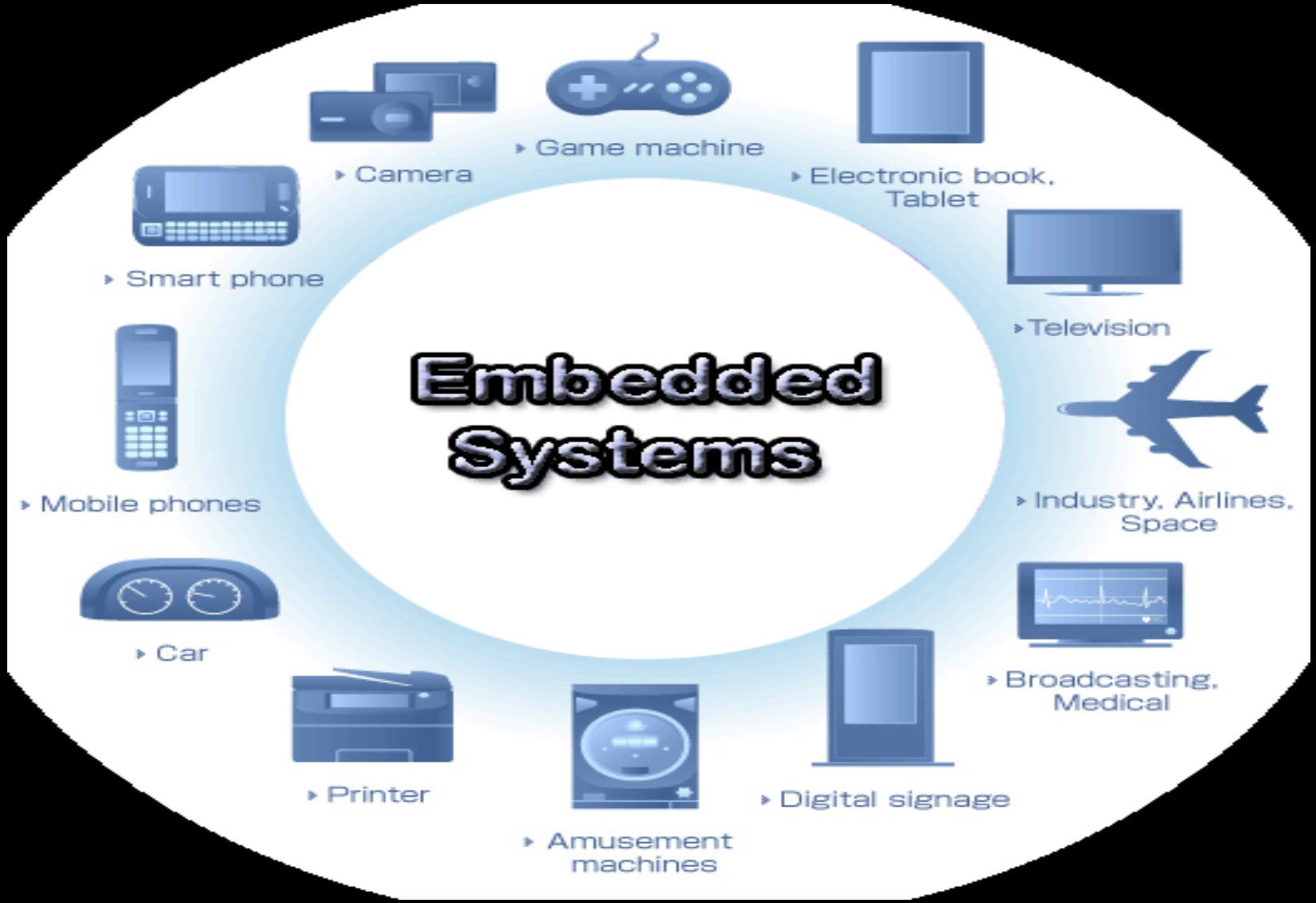
µC based Embedded Systems

- Special purpose computer system usually completely inside the device it controls
- Has specific requirements and performs pre-defined tasks
- Cost reduction compared to general purpose processor
- Different design criteria
  - Performance
  - Reliability
  - Availability
  - Safety

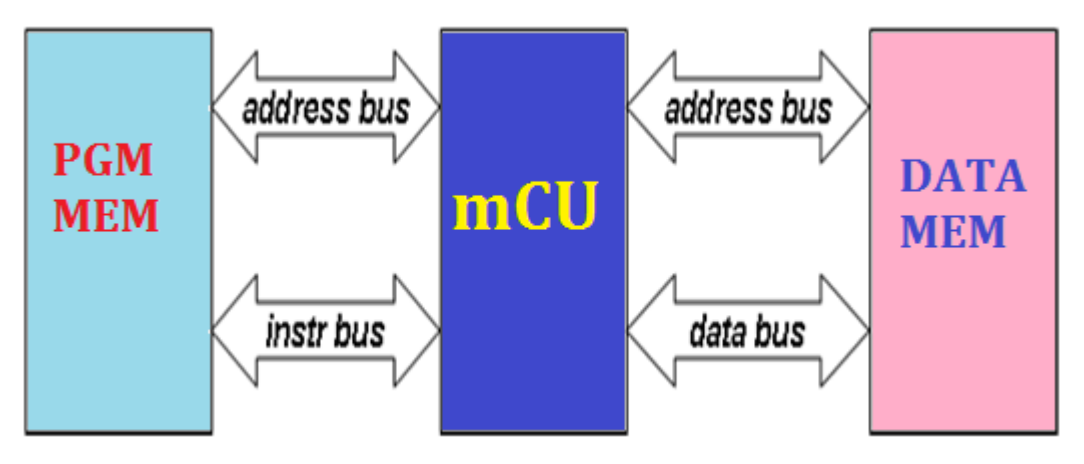
Embedded Systems Examples



Examples


Embedded Systems
Camera
Game machine
Electronic book, Tablet
Smart phone
Television
Mobile phones
Industry, Airlines, Space
Car
Broadcasting, Medical
Printer
Digital signage
Amusement machines

Harvard Architecture



In Harvard Architecture the data and instructions are stored in separate memory units each with their own bus.

Advantages:

- Speeding up the data transfer rate,
- Permits the designer to implement different bus widths and word sizes for program and data memory space.

8051 CPU Operation

1. Features
2. Pin Diagram
3. Block Diagram

8051 Microcontroller

- Intel introduced 8051, referred as MCS-51, in 1981.
- The 8051 is an **8-bit processor**
  - The CPU can work on only 8 bits of data at a time
- The 8051 became widely popular after allowing other manufactures to make and market any flavor of the 8051.

Features of 8051

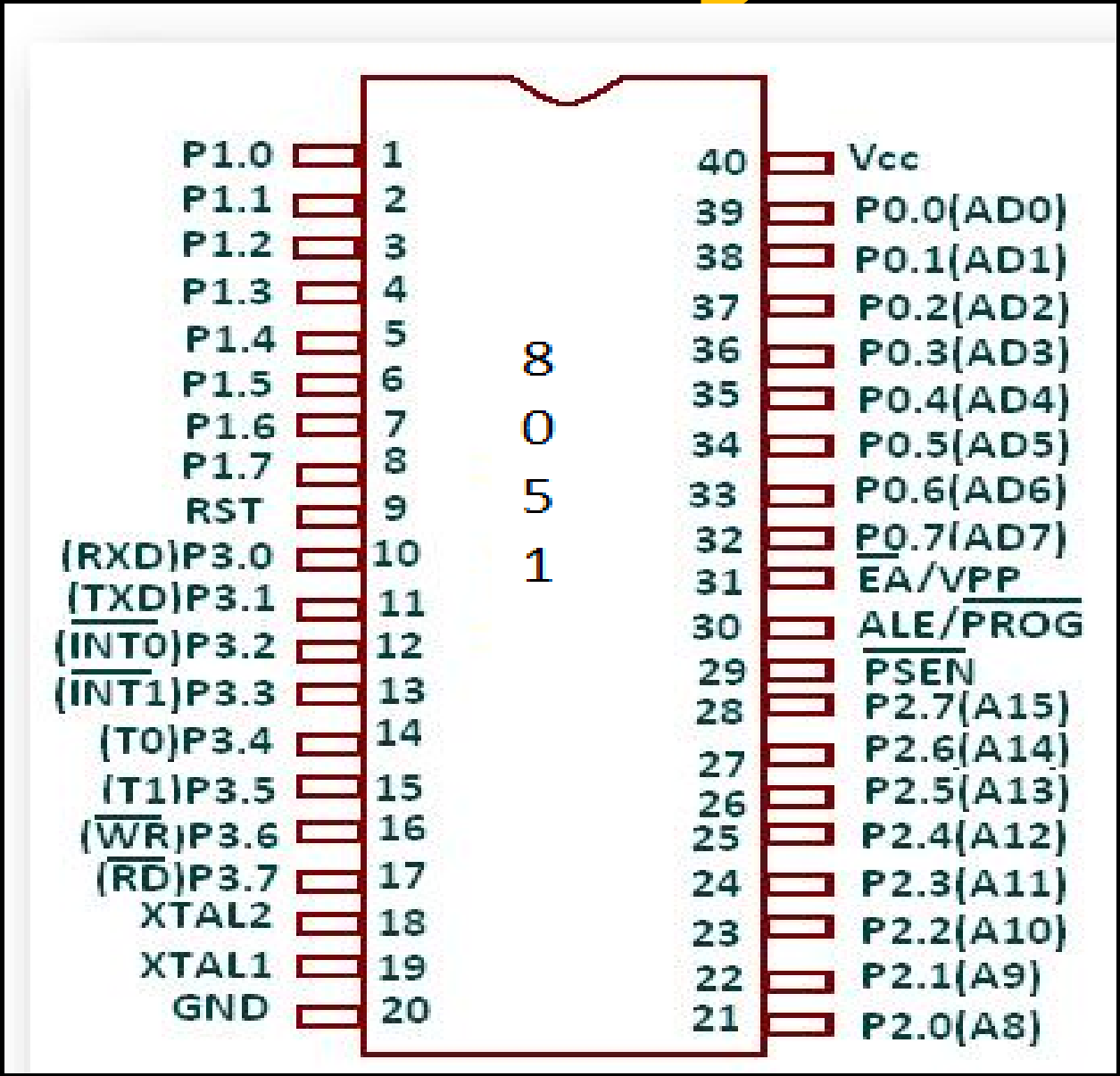
8 bit Processor
4KB Internal ROM
128 Bytes Internal RAM
Four 8 BIT I/O PORTS (32 I/O LINES)
Two 16 Bit Timers/Counters
On Chip Full Duplex UART for Serial Communication
5 Vector Interrupts (2 External, 3 Internal -
Timer0,Timer1,Serial)
On Chip Clock Oscillator
16 bit Address bus
64k External Code Memory
64k External Data Memory
16-bit program counter to access external Code Memory and
16 bit Data Pointer to access external Data Memory
128 user defined flags
32 General Purpose Registers each of 8 bits

8051 Family

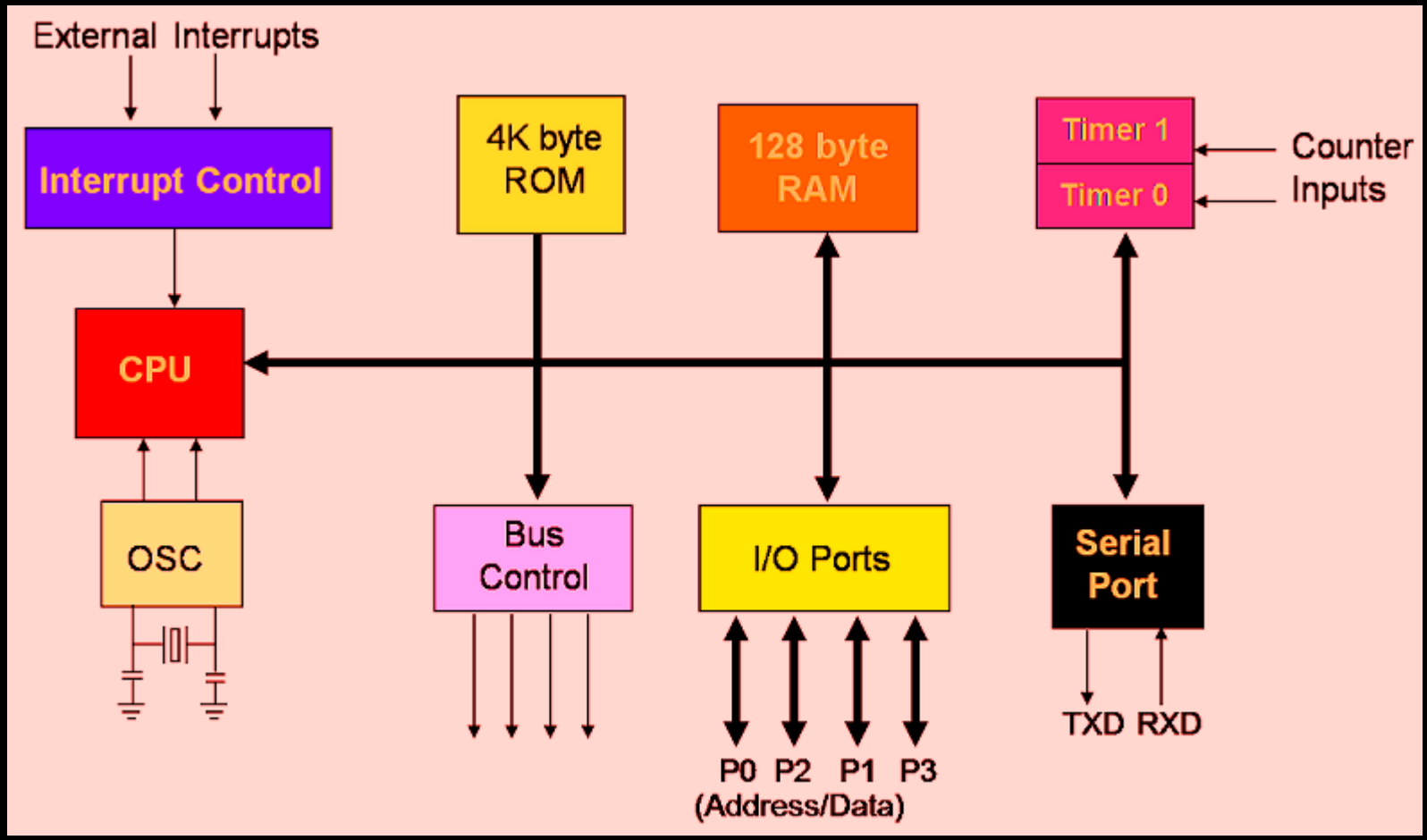
- The 8051 is a subset of the 8052
- The 8031 is a ROM-less 8051
  - Add external ROM to it
  - You lose two ports, and leave only 2 ports for I/O operations

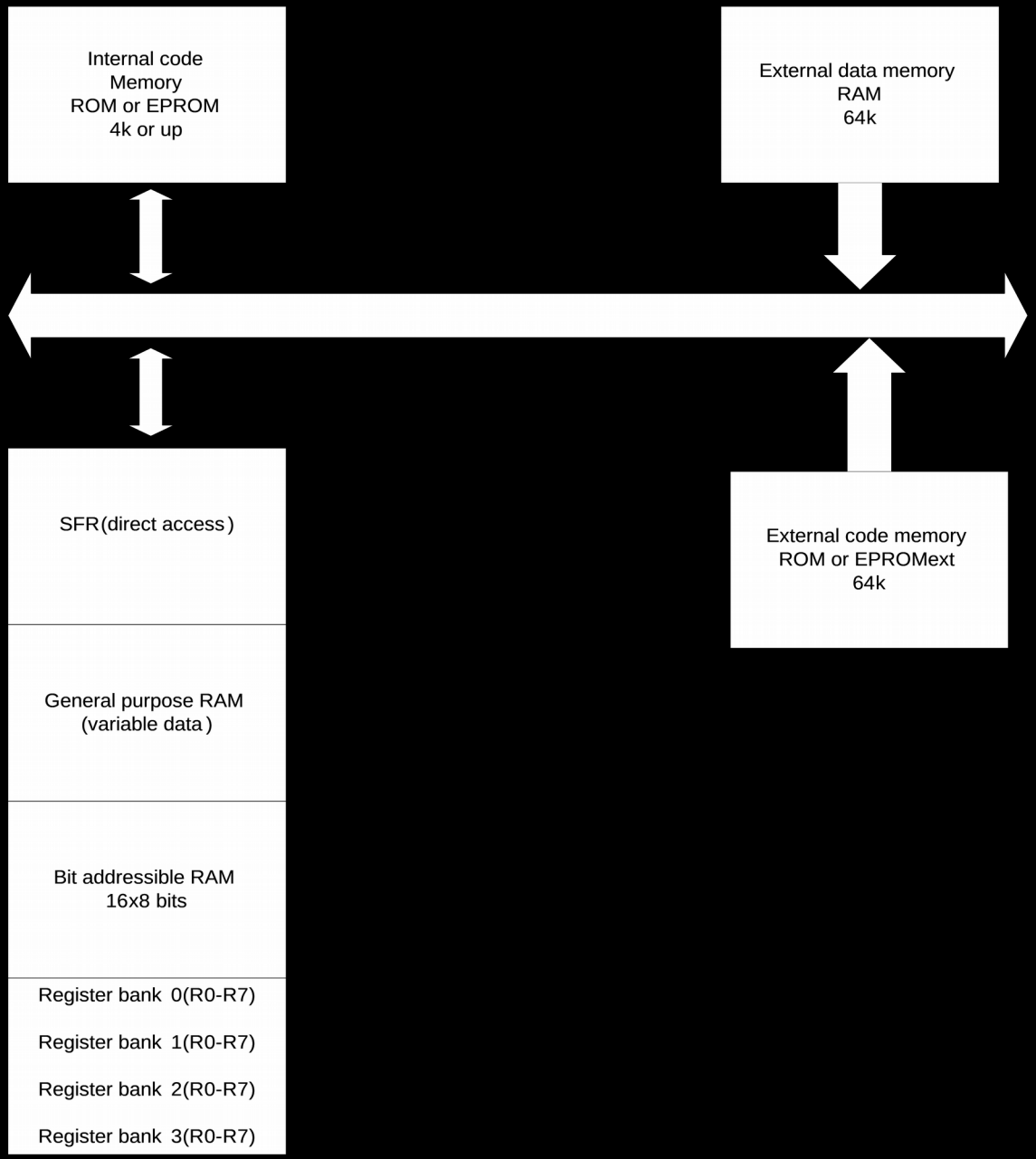
Feature	8051	8052	8031
ROM (on-chip program space in bytes)	4K	8K	0K
RAM (bytes)	128	256	128
Timers	2	3	2
I/O pins	32	32	32
Serial port	1	1	1
Interrupt sources	6	8	6

Pin Diagram


P1.0 1
P1.1 2
P1.2 3
P1.3 4
P1.4 5
P1.5 6
P1.6 7
P1.7 8
RST 9
(RXD)P3.0 10
(TXD)P3.1 11
(INT0)P3.2 12
(INT1)P3.3 13
(T0)P3.4 14
(T1)P3.5 15
(WR)P3.6 16
(RD)P3.7 17
XTAL2 18
XTAL1 19
GND 20
8051
40 Vcc
39 P0.0(AD0)
38 P0.1(AD1)
37 P0.2(AD2)
36 P0.3(AD3)
35 P0.4(AD4)
34 P0.5(AD5)
33 P0.6(AD6)
32 P0.7(AD7)
31 EA/VPP
30 ALE/PROG
29 PSEN
28 P2.7(A15)
27 P2.6(A14)
26 P2.5(A13)
25 P2.4(A12)
24 P2.3(A11)
23 P2.2(A10)
22 P2.1(A9)
21 P2.0(A8)

Block Diagram of 8051



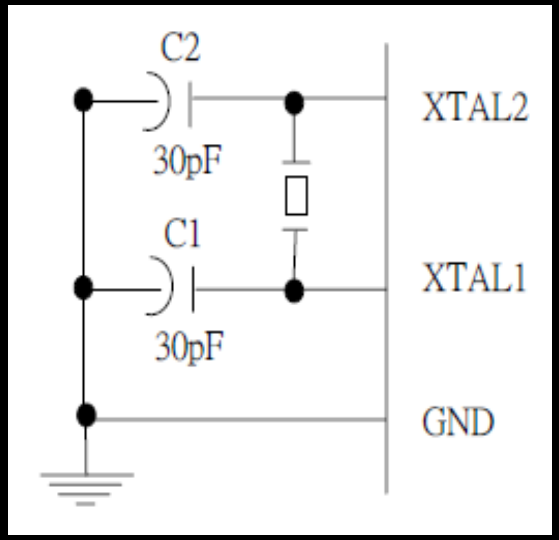

Internal code
Memory
ROM or EPROM
4k or up
External data memory
RAM
64k
SFR(direct access)
General purpose RAM
(variable data)
Bit addressible RAM
16x8 bits
Register bank 0(R0-R7)
Register bank 1(R0-R7)
Register bank 2(R0-R7)
Register bank 3(R0-R7)
External code memory
ROM or EPROMext
64k

Pin Description of the 8051

- 8051 family members (e.g., 8751, 89C51, 89C52, DS89C4x0)
  - Have **40 pins** dedicated for various functions such as I/O, RD, WR, address, data, and interrupts.
  - Come in different packages, such as
    - *DIP(dual in-line package),*
    - *QFP(quad flat package), and*
    - *LLC(leadless chip carrier)*
- Some companies provide a 20-pin version of the 8051 with a reduced number of I/O ports for less demanding applications

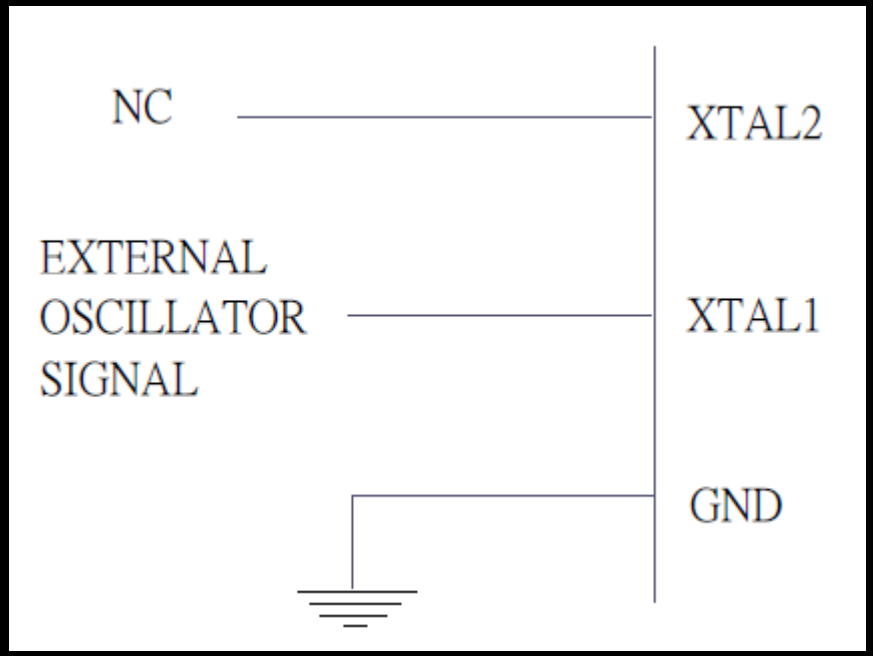
XTAL1 and XTAL2

- The 8051 has an on-chip oscillator but requires an external crystal to run it
  - A quartz crystal oscillator is connected to inputs XTAL1 (pin19) and XTAL2 (pin18)
  - The quartz crystal oscillator also needs two capacitors of 30 pF value
  - The original 8051 operates at 12 MHZ



XTAL1 and XTAL2 .....

- If you use a frequency source other than a crystal oscillator, such as a TTL oscillator:
  - It will be connected to XTAL1
  - XTAL2 is left unconnected



RST

- RESET pin is an input and is active high (normally low)
- Upon applying a high pulse to this pin, the microcontroller will reset and terminate all activities
- This is often referred to as a power-on reset
- Activating a power-on reset will cause all values in the registers to be lost

RESET value of some 8051 registers

we must place the first line of source code in ROM location 0

Register	Reset Value
PC	0000
DPTR	0000
ACC	00
PSW	00
SP	07
B	00
P0-P3	FF

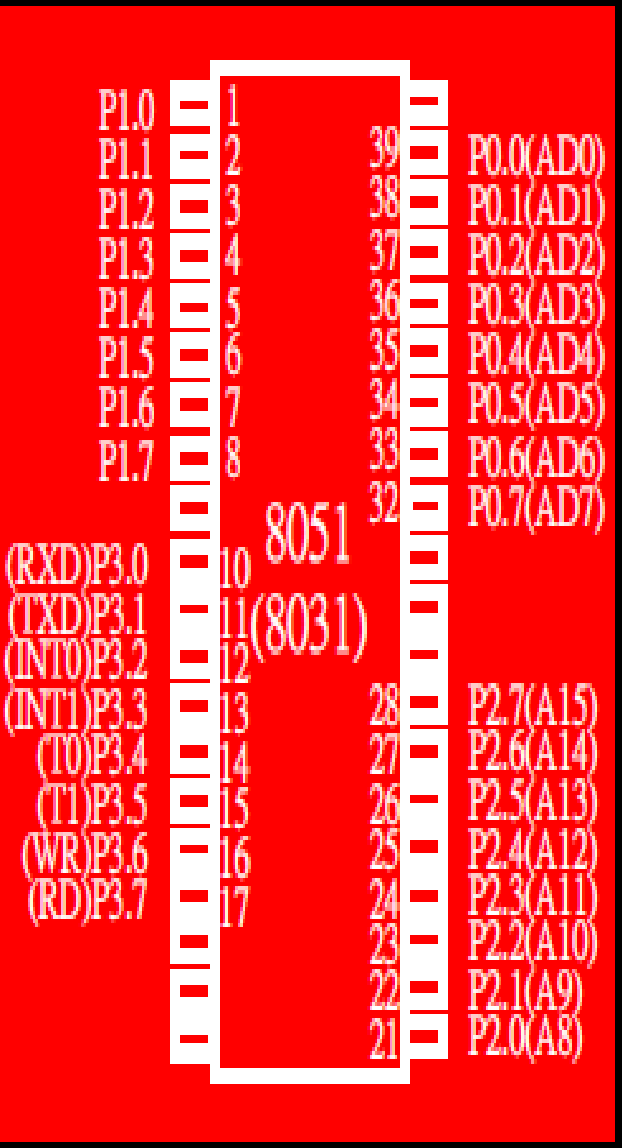
EA’

- EA’, **“external access’’**, is an input pin and must be connected to Vcc or GND
- The 8051 family members all come with on-chip ROM to store programs and also have an external code and data memory.
- Normally EA pin is connected to Vcc (Internal Access)
- EA pin must be connected to GND to indicate that the code or data is stored externally.

PSEN’ and ALE

- PSEN, **“program store enable’’**, is an output pin
- This pin is connected to the OE pin of the external memory.
- For External Code Memory, PSEN’ = 0
- For External Data Memory, PSEN’ = 1
- ALE pin is used for demultiplexing the address and data.

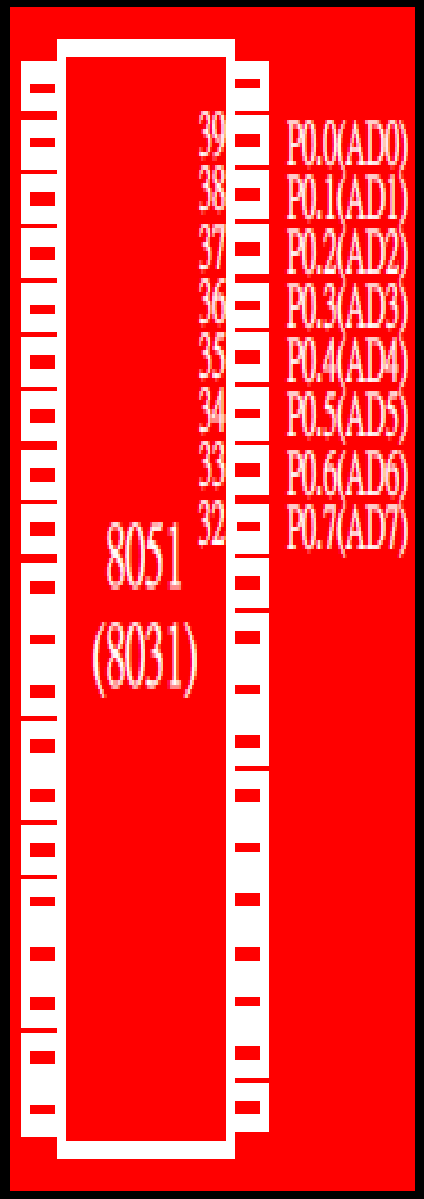
I/O Port Pins



The four 8-bit I/O ports **P0, P1, P2 and P3** each uses 8 pins.

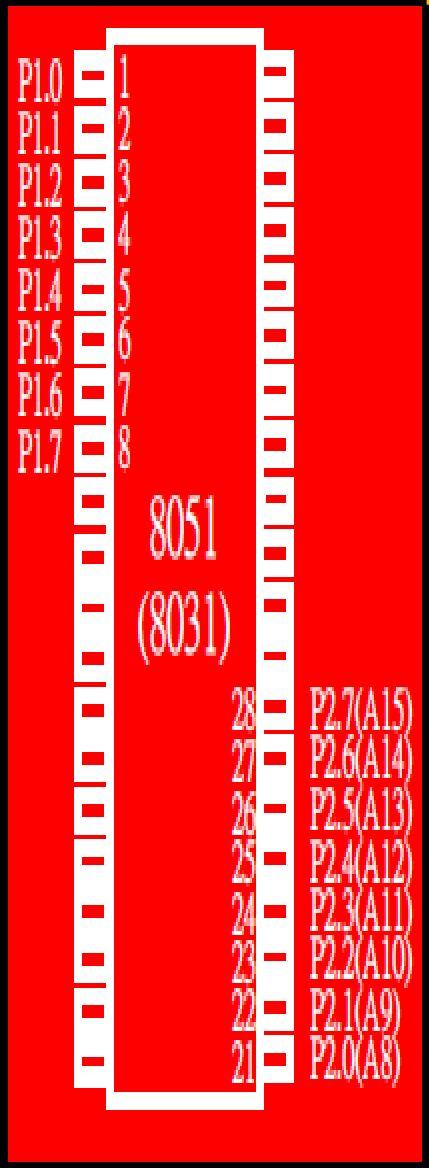
All the ports upon RESET are configured as output.

Port 0



- Port 0 is **also** designated as **AD0-AD7**.
- When connecting an 8051 to an external memory, port 0 provides both address and data.
- The 8051 multiplexes address and data through port 0 to save pins.
- **ALE** indicates if P0 has address or data.
  - *When ALE=0, it provides data D0-D7*
  - *When ALE=1, it has address A0-A7*

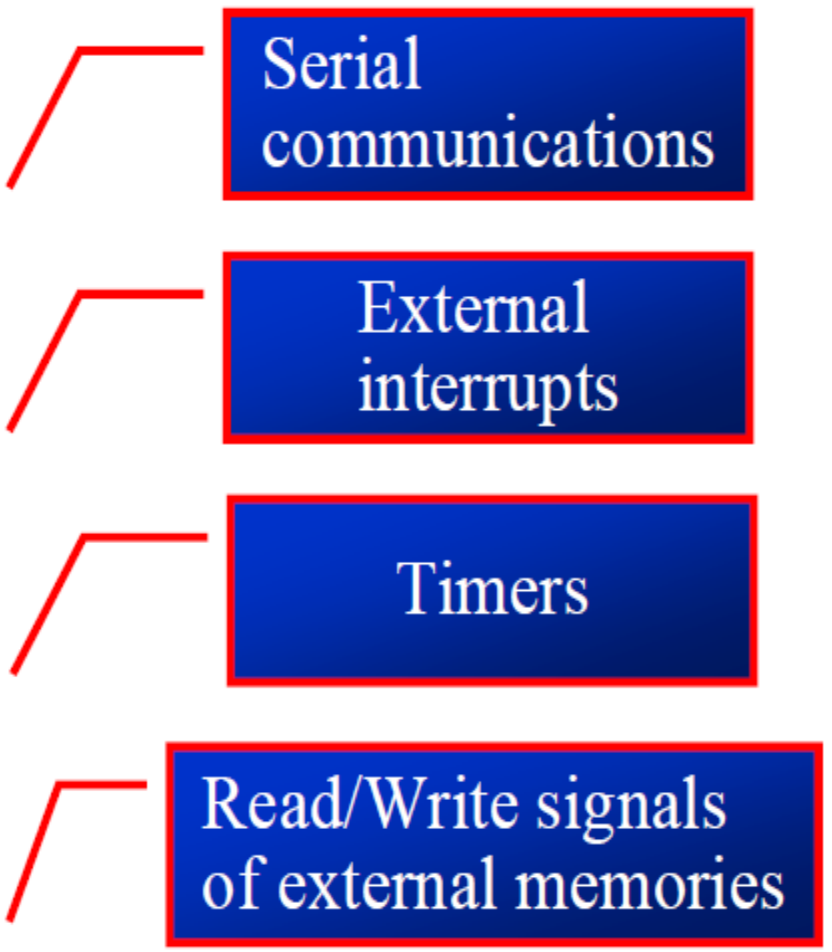
Port 1 and Port 2



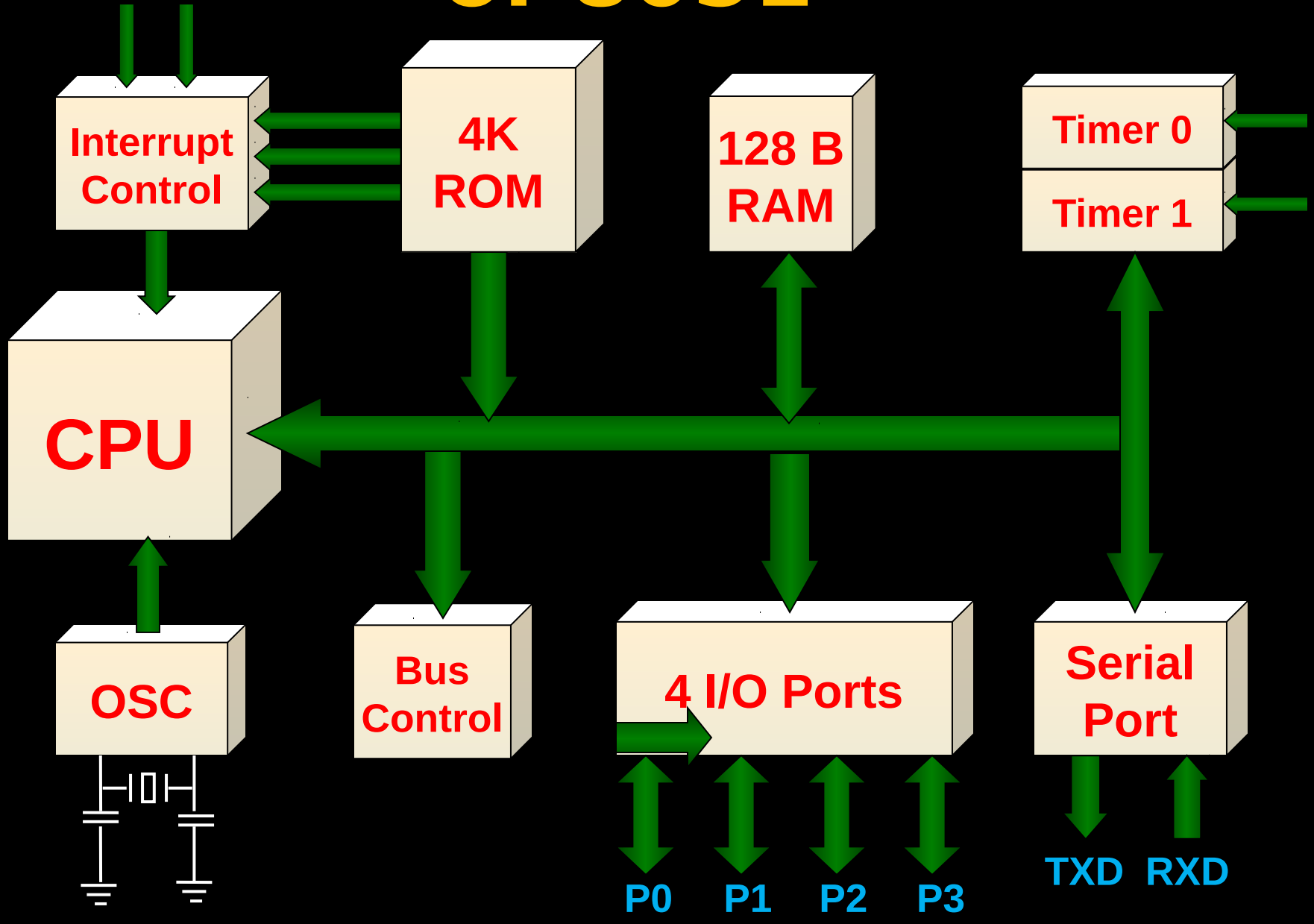
- In 8051-based systems **with no external memory connection**:
  - Both P1 and P2 are used as simple I/O.
- In 8051-based systems **with external memory connections**:
  - Port 2 must be used along with P0 to provide the 16-bit address for the external memory.
  - P0 provides the lower 8 bits via A0 – A7.
  - P2 is used for the upper 8 bits of the 16-bit address, designated as A8 – A15, and it cannot be used for I/O.

Port 3

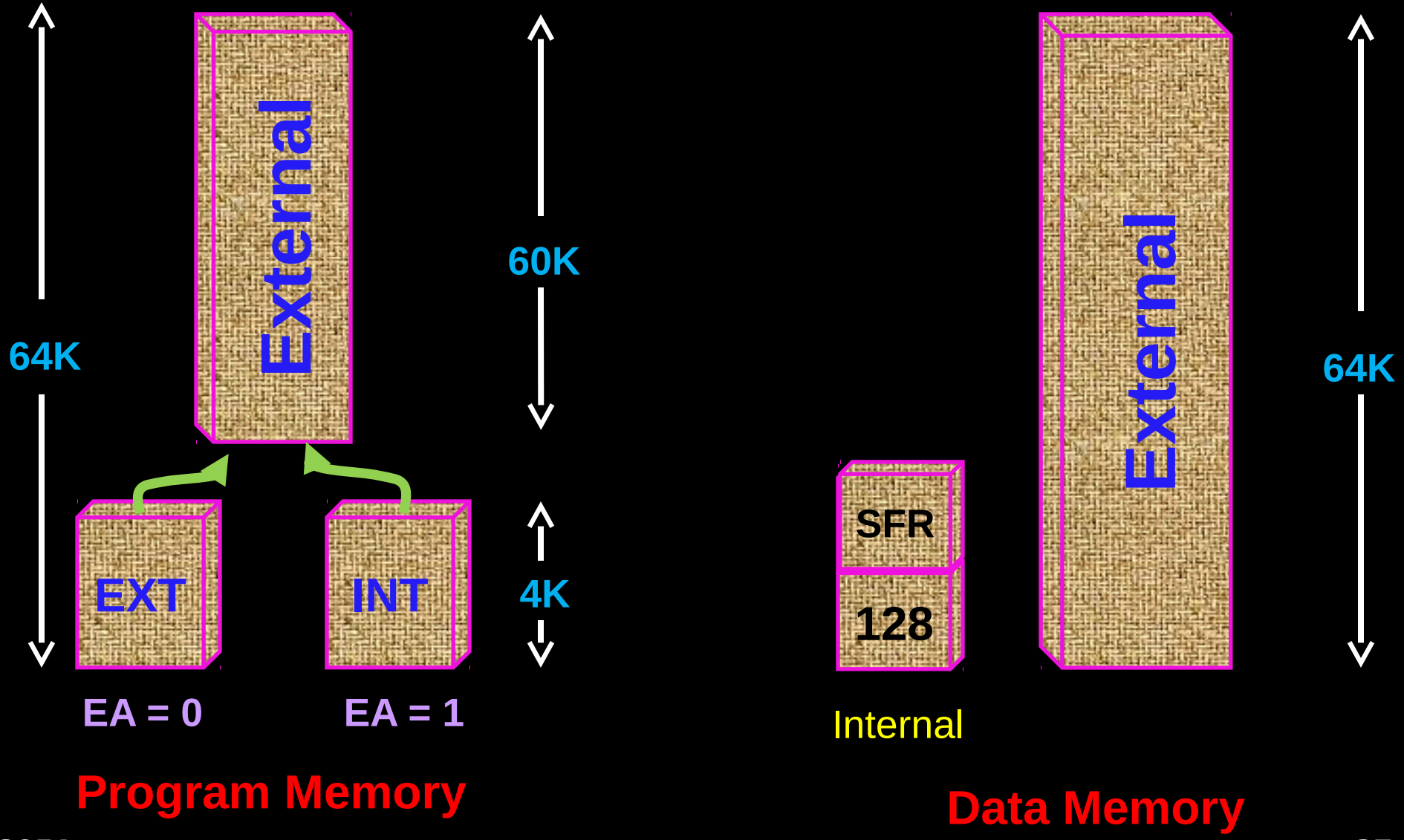
P3 Bit	Function	Pin
P3.0	RxD	10
P3.1	TxD	11
P3.2	$\overline{\text{INT0}}$	12
P3.3	$\overline{\text{INT1}}$	13
P3.4	T0	14
P3.5	T1	15
P3.6	$\overline{\text{WR}}$	16
P3.7	$\overline{\text{RD}}$	17



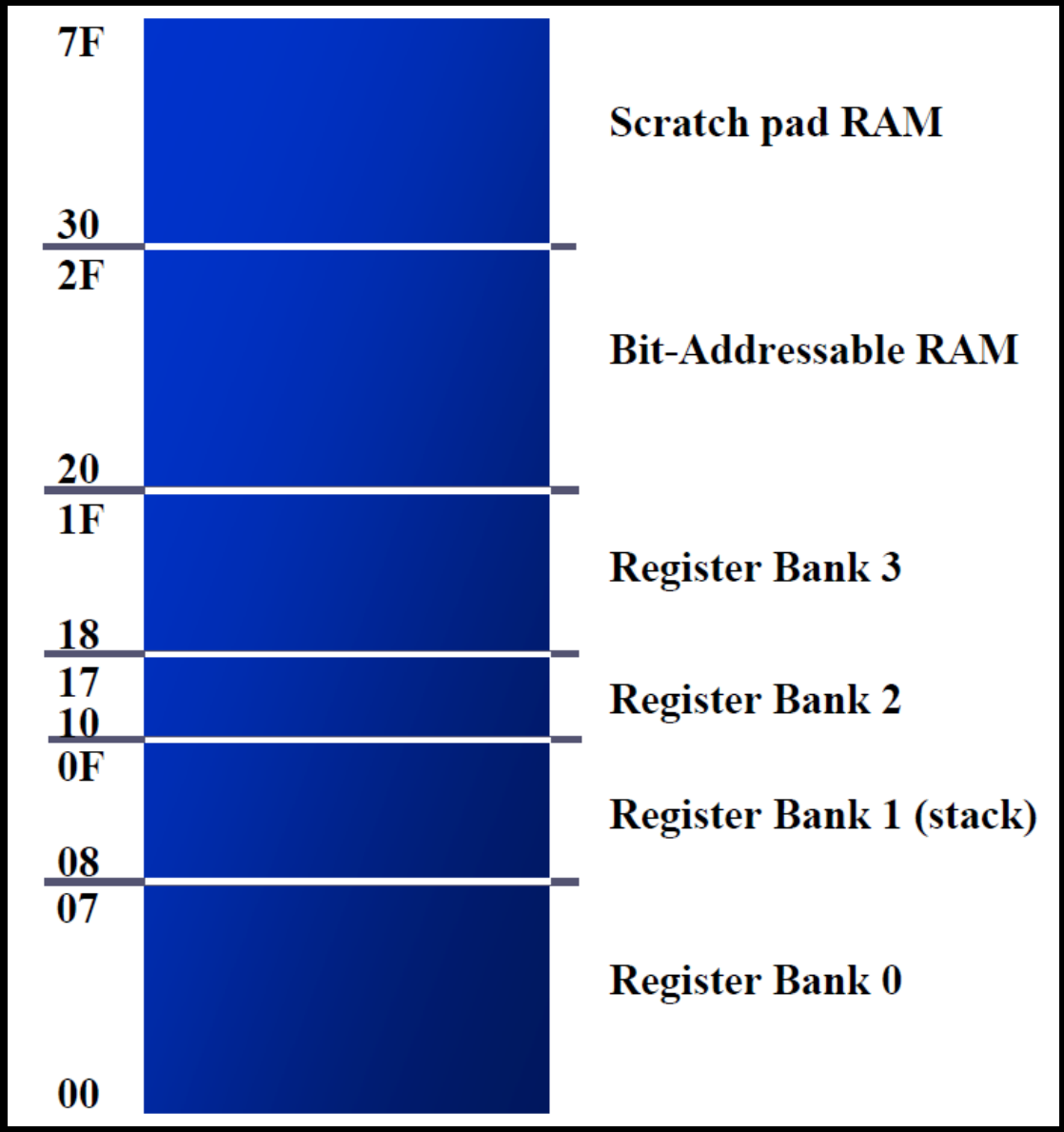
General Block Diagram of 8051



8051 Memory Structure

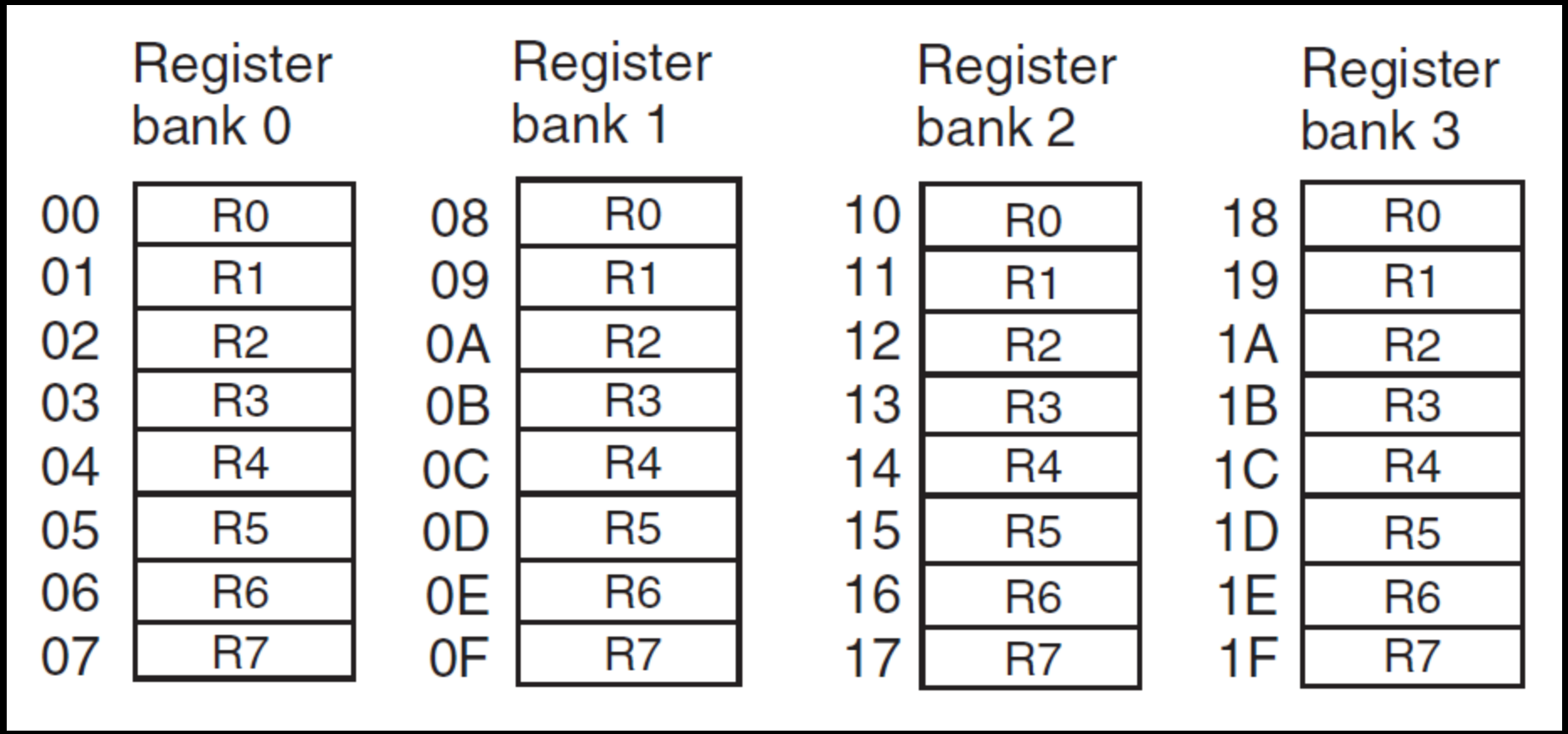


8051 RAM with addresses



8051 Register Bank Structure

8051 Register Banks with address



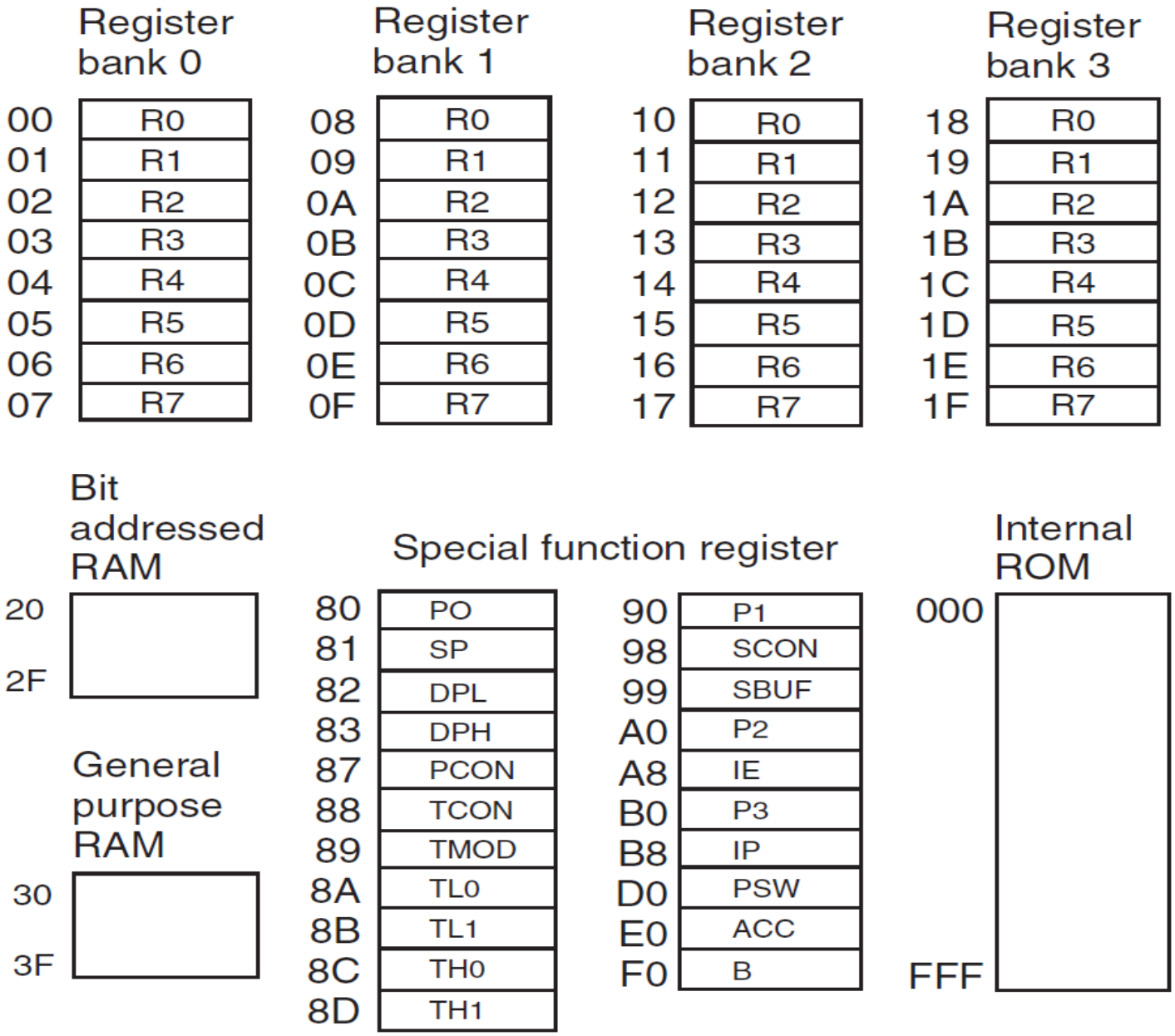


Figure C.3 80C51 programming model

8051 Addressing Modes

- The CPU can access data in various ways, which are called addressing modes

1. **Immediate**
2. **Register**
3. **Direct**
4. **Register indirect**
5. **External Direct**