Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 5th Semester Mid Semester Examination, September, 2022

Computer Architecture and Organization II (CS-3103)

Full Marks: 30 Time: 2 hours

Answer all questions

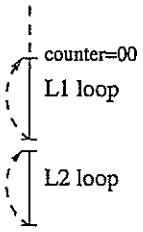
1A) Define "false sharing miss". State the cause and remedy of false sharing miss. 4

B) A bus based shared memory (MM) multiprocessor system consists of three processors P1, P2 and P3 with caches C1, C2, and C3 respectively. Each cache can accommodate *one* memory block at a time. The MM stores *two* blocks B1 and B2. The variables *x and y* are in B1. The variable *z* is in B2. Initially in MM $x = 10$, $y = 20$, and $z = 40$. The system follows snoopy based MESI model and write-invalidate scheme. Initially, C1, C2, and C3 are empty. Now, the following events occur in sequence

(1) P1 reads *y*, (2) P2 reads *y*, (3) P2 updates x = *x*-5, (4) P3 reads *y*,
(5) P1 updates y = *y*+2, (6) P3 reads *x*, (7) P2 updates *x* = 10, (8) P1 reads *x*.

i) Show the values of *x*, *y* and *z* in MM after each event.
ii) Show the states of cached blocks in C1, C2 and C3 after each event.
iii) Denote the case of false sharing miss if any. 6

2A) State basic principle of 2-bit branch prediction. A program, consisting of two consecutive loops L1 and L2 (Fig, 1), is executed in CPU_{test}. L1 and L2 iterate 3 and 2 times respectively. The CPU_{test} implements 2-bit history (counter) for loop branch prediction. The counter is initialized to '00' before execution of L1. Determine count value of 2-bit history counter after each iteration of L1 and L2. 4



B) Consider execution of the following code in a 5-stage pipeline (IF, ID/OF, EX, MEM, and WB):

```
load  R1, M(R3)
mult  R2, R1, R4
or    R4, R1, R9
and   R5, R1, R7
```

a) Find number of stalls required to eliminate data hazards if data forwarding is not allowed.
b) What speed-up is achieved if data forwarding is realized? Show details. 6

3A) Following nested loop is in execution. Elements of A are stored in row major order in memory. Show how cache misses for A can be reduced by loop interchange technique. 5

```
for i=1 to 10 with incr 1
   for j=1 to 20 with incr 1
      A[j][i] = 2*B[i][1];
```

B) Define write-update cache coherence scheme. Explain which approach, write-update or write-invalidate, leads to better performance if
a) Processor P1 writes x to V of block B and all other (P-1) processors read x of V.
b) P1 writes V hundred times followed by a read by other processor Pi. 5