20/11/19

Indian Institute of Engineering Science and Technology, Shibpur

BTech 5th Semester (CST) Examinations, 2019

Subject: Computer Architecture and Organization II — Paper: CS-502

Time: 3 hours — Full marks: 70

Answer any four

1a) A uni-processor system uses separate instruction cache and data cache with hit ratios h_i and h_d, respectively. The access time from the processor to either cache is C clock cycles, and the block transfer time between a cache and main memory is B clock cycles. Among all memory references made by the CPU, F_i is the percentage of references to instructions. Among blocks replaced in the data cache, F_{dir} is the percentage of dirty blocks (the cached copy is different from main memory copy). Assuming a write-back policy, determine the effective memory access time in terms of h_i, h_d, C, B, F_i, and F_{dir} for this memory system. 7.5

b) Assume a m/c performs with CPI 2.0 when all the memory accesses hit in the cache. The only data accesses are the load and store, and these are in total 40% of the total number of instructions executed. If the miss penalty is 20 clock cycles, compute the cases (i) where in all references hit and (ii) where in miss rate is 2%. 6

c) Find the CPI of two pipelined base scalar processors (P1 and P2), where P1 is with 4-stage instruction pipeline and P2 is with 8-stage instruction pipeline. 4

2a) Define ERCW and CREW SIMD computer. Describe the method of broadcasting a message x in such computers. Estimate the worst case search time to find the element x from a table of N elements in (i) ERCW; (ii) CREW SIMD computer. 10

b) Design a shuffle-exchange interconnection network for an SIMD machine with 8 processing elements PE0 to PE7. Find the number of shuffle/exchange operations needed to transfer an information from PE1 to PE5. 7.5

3a) Define write-invalidate and write-through schemes for cache coherence. The following steps describe the values of X in cache 1 of processor P1, cache 2 of processor P2, and main memory (MM) of a multiprocessor system, after different activities in write-invalidate scheme for maintaining cache coherence. The cache write policy is the write-back and X is in main memory block BX.

Activity	X at cache 1	X at cache 2	X at MM
1. Initial state	20	-	20
2. P2 reads X	A	B	C
3. P1 writes X=0	D	E	F

Find A, B, C, D, E and F. 7.5

b) Describe, in brief, the static model of data flow machine architecture with 16 processing elements and 64 cell blocks in memory section. 5

c) Define `Early restart' and `critical word first' schemes employed in cache system design. 5

4a) Consider the bus-based shared memory shown in Fig. 1. Let assume that the words X1 and X2 are in the same block B. The block B is in the caches (Cs) of P1 and P2 at time step 0. For the following sequence of events, identify the bus activity (cache miss/hit false/true) in a Write-Invalidate protocol. 7.5

Time step	Event	Bus activity (cache miss/hit false/true)
1.	P1 updates X1	
2.	P1 reads X2	
3.	P2 reads X2	
4.	P1 updates X1	
5.	P2 updates X2	
6.	P1 reads X2	

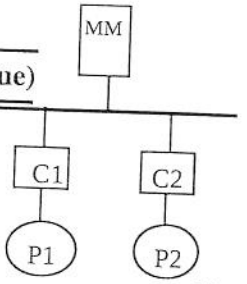

Fig. 1

b) Consider the following loop

for $i = 1$ to n with increment 2 do
f ();

Unroll the loop by inserting 4 copies of the body f() and find the number of loop iterations is reduced, for (i) $n = 100$; (ii) $n = 103$. 6

c) A multi-processor system with 2048-core processors implements limited directory protocol for its cache system. It allows up to 8 cores to have a cached copy of a block. The memory block/ cache line size is 128 bytes. How many directory state bits are required to track which caches are sharing a given block of memory and what is the ratio of directory state bits to data bits? 4

5a) Define a branch delay slot. Identify the branch delay slot in the following program segment:

```
L1:
load R1, M(R2)
Sub R3, R3, R1
Bnez  R3, L1
Store R4, M(R3)
```

Modify the program segment by moving an instruction to the delay slot. Evaluate its performance considering - (i) "predict taken" scheme, (ii) "predict-not-taken" scheme. 7.5

b) Take the following example program segments (i) and (ii)

(i)
```
for i = 1 to 55 do
    A[i] = A[i] * B[i];
for j = 1 to 55 do
    B[j] = A[j] * A[j];
```

(ii)
```
for i = 1 to 55 do
    begin
      A[i] = A[i] * B[i];
      B[i] = A[i] * A[i]
    end
```

Compute the total number of cache misses during execution of (i) and (ii). Assume each element of A and B forms a memory block and the cache can accommodate one element of A and one element of B at a time. 5

c) Describe, in brief, the loop interchange technique to reduce cache miss rate. 5

6a) Define RAW, WAR, and WAW data hazards. Consider the following code sequence:

```
SW  512(R0), R3     ; M[512] ← R3
LW  R1, 1024(R0)    ; R1 ← M[1024]
LW  R2, 512(R0)     ; R2 ← M[512]
```

Identify the case of possible data hazard. Define its type (RAW/WAR/WAW). 7.5

b) State key features of (i) *in-order issue in-order completion,* (ii) *in-order issue out-of-order completion, and* (iii) *out-of-order issue out-of-order completion* superscalar schemes. 5

c) A CPU has a 64 KB direct mapped cache with 128-byte block size. Suppose A is a two-dimensional array of size 512x512 with elements that occupy 8-bytes each. Consider the following C code segment

```
for (i = 0; i<512; i++) {
    for (j =0; j<512; j++) {
        x+ = A[j][i];
} }
```

Find the number of compulsory and conflict cache misses experienced by the program segment. 5

7. Write short notes on the following

a) pseudo-associative cache and *hit* time. 7.5

b) 4^3x3^3 delta network. 10