Assignment – Computer Architecture and Organization – II, 2021
Instructor: Biplab K Sikdar

Cache Design

1, Consider the dual processor system shown in Fig. 1

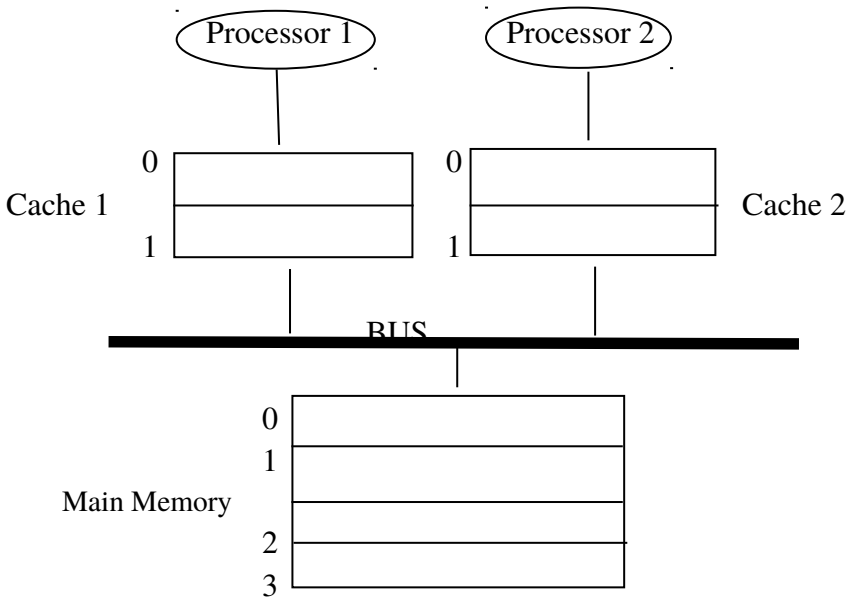

Fig. 1

using write-through caches to maim memory. To maintain cache coherence the system uses snoopy protocol based on the write-invalidate policy.

Consider the following sequence of memory access events, where bold face numbers are for writes and the remaining are for read

Processor #1	0	**0**	1	0	1	**1**	2	0
Processor #2	0	**1**	0	1	0	**2**	2	3
	1	2	3	4	5	6	7	8

(i) Trace the execution of this reference by two processors.
(ii) Calculate the number of hits in Cache 1 and Cache 2

Assume both the caches are initially flushed (empty) and implement direct mapping.

2. Consider the bus-based shared memory shown in Fig. 2. Let assume that the words X1 and X2 are in the same block B. The block B is in the caches (Cs) of P1 and P2 at time step 0. For the following sequence of events identify each miss as a true sharing miss, a false sharing miss, or a hit in a Write-Invalidate protocol.

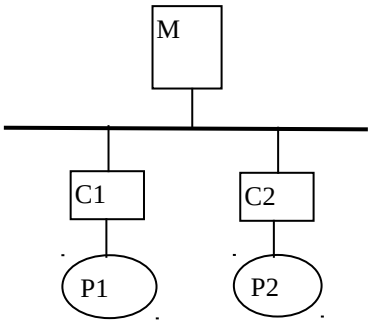

Fig. 2

Time step	Event	Bus activity (cache miss/hit false/true)
1	P1 updates X1	
2	P1 reads X2	
3	P2 reads X2	
4	P1 updates X1	
5	P2 updates X2	
6	P1 reads X2	