Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 5th Semester Examinations, 2020

Computer Architecture and Organization II (CS-502)

Full marks: 70 Time: 1 hour 30 minutes

Answer any four

1. Consider the bus-based shared memory (Main memory M) system with two processors - Processor 1 (P1) and Processor 2 (P2), shown in Figure yy. Assume X in memory was originally set to 10 and then following operations were performed in the order given:
(1) P 1 reads X; (2) P 2 reads X; (3) P 2 updates X=5; (4) P 2 reads X;
(5) P 2 updates X=10; (6) P 1 updates X=0; (7) P 2 reads X.

Assume both the caches are initially flushed (empty) and implement direct mapping.

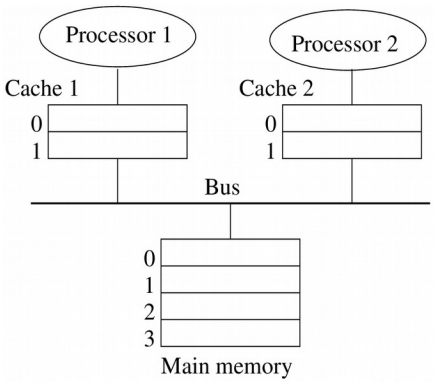

Figure yy

a) Define Write-Invalidate protocol.
(i) Identify the events - (read/write) hit/miss that occurred for the sequence of operations (1) to (7) in a Write-Invalidate protocol.
(ii) Show the value of X at main memory (M), Cache 1 and Cache 2 after each operation. 10

b) Consider the system of Figure yy realizes write-through policy. To maintain cache coherence it follows snoopy protocol based on the Write-Invalidate policy. Consider the following sequence of memory access events, where bold face numbers are for writes and the remaining are for read

Processor 1 0**0**101**1**20
Processor 2 0**1**010**2**23
Time step 12345678

(i) Define write-through policy.
(ii) Show the traces of reference by the processors 1 and 2 in the caches; and find the number of hits in cache 1 and 2. 7.5

2a(i) Indicate the basic features of an ERCW shared memory SIMD computer. A table 'tt1' contains n elements. Estimate the worst case search time to find the elements x and y in tt1 considering ERCW SIMD computer.

(ii) Show interconnection of an SIMD machine with 4 PEs (PE 0 to PE 3), using shuffle-exchange interconnection network. Show how PE 2 and PE 3 can transfer the data items to PE 1. 10

b) Draw the structure of 3x4 crossbar switch. Define its function. Show the interconnection of a 3^2x4^2 delta network. 7.5

3a(i) Draw a data flow graph showing the computations of

```
if a<b then a*b
  else a - b
endif.
```

(ii) Describe in brief the static model of Data Flow machine with 4 PEs (processing elements) in processing section and 16 instruction cell blocks in memory section. 12

b) Explain the case of out-of-order exceptions. How it is handled in instruction pipeline? 5.5

4a) Let consider execution of the program segment:

I 1 : R 1 ←Memory(A)
I 2 : R 2 ←R 2 + R 1
I 3 : R 3 ←R 3 + R 4
I 4 : R 4 ←R 4 * R 5
I 5 : R 6 ← ¬R 6
I 6 : R 6 ←R 6 * R 7

In the program segment, there are possibilities of RAW between I_x and I_y, WAR between I_a and I_b, and the WAW between I_i and I_j.

(i) Define RAW and WAR.
(ii) Find I_x, I_y, I_a, I_b, I_i and I_j.
(iii) Allocate additional physical registers (register renaming) to remove WAR and WAW; and show the modified program segment. 7.5

b(i) What is loop unrolling in ILP?
(ii) Consider the following loop

```
for i = 1 to n with increment 2 do
  f ();
```

Unroll the loop by inserting 3 copies of the body f() and find the number of loop iterations is reduced, for (i) $n = 999$; (ii) $n = 1000$. 10

5a(i) Define superscalar, superpipelined and superscalar-superpipelined processing.

(ii) State the key features of in-order issue, in-order-completion; in-order issue, out-of-order-completion; and out-of-order issue, out-of-order-completion superscalar schemes. 10

b) Distinguish between UMA and NUMA system. 7.5