30/11/16

Indian Institute of Engineering Science and Technology, Shibpur
Dual-Degree (BTech-MTech) 5th Semester Examinations, 2016

Subject: Computer Architecture and Organization II — Paper: CS-502
Time: 3 hours — Full marks: 70

Answer any five

1a) Define CPI. In a 16-stage pipeline computer MC, 4 bubbles (stall cycles) must be inserted for a conditional branch instruction and a cache miss causes the pipeline to stall for 25 cycles. Compute effective CPI for MC if the branch instructions constitute 15% of all instructions executed and 2% of all instructions encounter a cache miss when accessing the data memory. 8

b) What do you mean by loop unrolling in ILP? Consider the following loop

for $i = 1$ *to* n *with increment* 1 *do*
  $f()$;

Unroll the loop by inserting 4 copies of the body $f()$ for
i) $n = 1000$,
ii) $n = 1002$. 6

2a) Consider the following code segment

load R1, M(R2)
sub R1, R1, R3
add R4, R4, R5
or R6, R1, R7

Show dependencies of the instructions in the code segment and then explain how data speculation can be used to increase parallelism in execution. 8

b) Show how loop interchange technique can reduce the cache miss rate for the following loop

for $j = 1$ *to* 100 *with increment* 1
  for $i = 1$ *to* 10 *with increment* 1
    A[i][j] = B[j][1] * B[j+1][1]; 6

3a) A program consists of two nested loops, with only single branch instruction at the end of each loop. The outer loop is executed 100 times and the inner loop 200 times. Determine the accuracy of following branch prediction strategies while executing the nested loop. 8
i) Always predict taken.
ii) Always predict not taken.
iii) Use 1-bit of history (history for each loop is initialized to "taken").

b) Define register renaming in superscalar processing. Consider the following program segment

I1: R 1 ← M(X)
I2: M(Y) ← R 1
I3: R 1 ← R 2 × R 3
I4: R 1 ← R 4 + R 5

Show how renaming of registers can be done to exploit parallelism among the instructions while executed in out-of-order issue, out-of-order completion superscalar processor. 6

4a) Describe snoopy cache coherence protocol, based on the write-invalidate policy, for a system

with write-back cache. 8

b) Define false sharing miss. Consider the bus-based shared memory of Figure 1. The words X1 and X2 are in the block B. The block B is initially in the caches (Cs) of processors P1 and P2. For following sequence of events, identify each miss as true sharing miss or false sharing miss. Assume the system follows write-invalidate cache coherence scheme. 6

1. P2 updates X1, 2. P2 reads X2, 3. P1 reads X2,
4. P2 updates X1, 5. P1 updates X2, and 6. P2 reads X2.

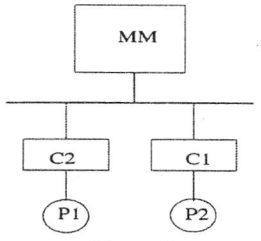

Figure 1

5a) Define 'miss penalty' in a cache/memory system. Describe how sub-block placement and early restart strategies can be effective in reducing cache miss penalty. 8

b) Define hit time in cache based system. Explain the role of pseudo-associative cache in reducing hit time. 6

6a) Distinguish SIMD and MISD machine. Show interconnection of an SIMD machine with 8 PEs (PE 0 to PE 7), using shuffle exchange interconnection network. A data item X is in PE1 and to be communicated to other PEs. Find the PEs with X if the shuffle interconnection function is executed 3 times. 8

b) Describe in brief the static model of Data Flow machine architecture with 8 processing elements, in processing section, and 64 instruction cell blocks in memory section. 6

7a) Define function of 2x2 crossbar switch. Show the interconnection of $2^3 \times 2^3$ delta network. 8
b) Describe, in brief, the model of NUCA based chip multiprocessors (CMPs). 6

8. Write short notes on the following
a) MESI protocol. 8
b) Code motion and compensation codes. 6