QUIZ-CACHE-2021-2

Total points 10/10

The respondent's email (**510519109.abhirup@students.iiests.ac.in**) was recorded on submission of this form.

✓ A program in execution with 200 blocks if needs all its blocks during execution, encounters 2/2

- ○ 100 compulsory misses
- ○ Unlimited compulsory misses
- ○ Unknown number of compulsory misses
- ◉ 200 compulsory misses ✓

✓ The hit time in pseudo-associative cache is almost same as that of 2/2

- ○ 4-way associative cache based system
- ◉ Direct-mapped cache based system ✓
- ○ 8-way associative cache based system
- ○ A fully associative cache based system

✓ Higher associativity of cache reduces 2/2

- ○ Capacity misses
- ○ Both compulsory and capacity misses
- ○ Compulsory misses
- ◉ Conflict misses ✓

✓ Consider instruction stream in an I-cache (for a program) is I1, I2, I3, I4, I5, I6, I7, I8, I9, I10. Let assume two instructions per block. That is, B1(I1, I2), B2(I3, I4), B3(I5, I6), B4(I7, I8) and B5(I9, I10). While executing the program trace contains I1, I2, I4, I7, I8, I10. That is, the blocks in the trace cache are 2/2

- ○ B1, B2, B3, B4
- ○ B1, B3, B4, B5
- ◉ B1, B2, B4, B5 ✓
- ○ B1, B2, B3, B5

✓ In cache design, early restart and critical word first are effective when block size is very large. Its main target is to reduce 2/2

- ○ Miss rate
- ○ Hit ratio
- ◉ Miss penalty ✓
- ○ Hit time