Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 5th Semester Examinations, 2021

Computer Architecture and Organization II (CS-3103)

Full marks: 50 Time: 1 hour 30 minutes

Answer any four

1. Consider the bus-based shared memory (main memory) system with two processors - Processor 1 (P1) and Processor 2 (P2), shown in Figure yy. Assume X in memory was originally set to 20 and then following operations were performed in the order given:
(1) P 1 reads X; (2) P 2 reads X; (3) P 2 updates X=5; (4) P 2 reads X;
(5) P 1 updates X=20; (6) P 2 reads X.

Assume both the caches are initially flushed (empty) and implement direct mapping.

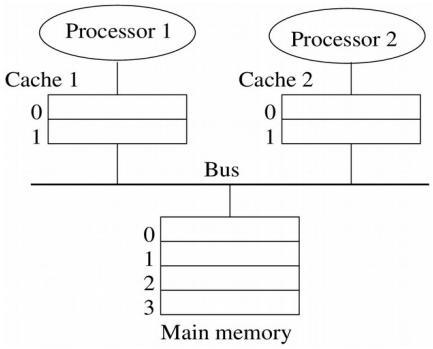


Figure yy

i) Define Write-Invalidate and Write-Update protocol in cache coherence.
ii) Identify the events - (read/write) hit/miss that occurred for the sequence of operations (1) to (6) and the value of X at main memory, Cache 1 and Cache 2 after each operation in Write-Invalidate and Write-Update protocol. 12.5

2. Define branch *delay slot* and *predict taken/predict not-taken* branch prediction scheme. Follow execution of the program segment

```
        Add  R1, R2, R3
        Branch L if R2=0
        Or R4, R5, R6
   L:  Sub R7, R8, R9
```

in a 4-stage (IF, ID, OF, EX) pipeline.

i) Identify the branch delay slot.
ii) Assuming *stall-on-branch* and no *delay slot*, what speed-up is achieved on execution of this code if branch outcome is determined at ID stage. Show the snapshot of pipeline execution.
iii) Modify the original program segment by moving an instruction to the delay slot. Evaluate performance of "predict taken" scheme on modified program segment. 12.5

3. Define EREW/CREW/ERCW/CRCW SIMD m/c with N processing elements. Find time to replace elements *x* from a table of *n* elements by 100 in such SIMD computers. 12.5

4. Define in-order issue in-order-completion, in-order issue out-of-order-completion, and out-of-order issue out-of-order-completion superscalar schemes. Show the architecture of a superscalar processor that can fetch and decode three instructions at a time. It has 2 writeback pipeline stage (WB1, WB2) and 3 functional units (FUs) (one FU requires 2 pipeline stages and 1 stage for each of other FUs). The following are constraints on a six-instruction (I1 to I6) code fragment:

- I1 requires two cycles to execute.
- I3 and I4 conflict for the same functional unit.
- I5 depends on the value produced by I4.
- I5 and I6 conflict for a functional unit.

To guarantee in-order completion, when there is a conflict for a functional unit or when an FU requires more than one cycle to generate a result, issuing of instructions temporarily stalls. Find time to complete execution of the code fragment. State assumption if any. 12.5

5. What is compulsory/conflict/capacity miss? If cache size is increased (block size remaining constant), then clarify the impact on compulsory/conflict/capacity miss. Show how

(i) pseudo-associative cache and (ii) loop fusion

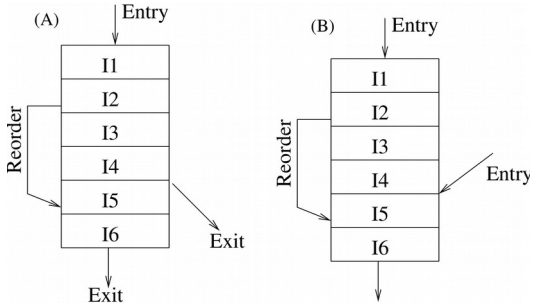
can reduce cache miss rate for the following program segment

```
.....
for  i= 1 to 1000 with increment 1 do
     C[i] = B[i] +A[i];
.............
for i= 1 to1000 with increment 1 do
        D[i] = B[j][1] * 2 x A[i];
.....…
```

12.5

6a) Define $0^{th}/1^{st}/2^{nd}$ order predictor in context-based value predictor. Let sequence of values of *x* is *a a a b b c d c a a a b b c a a a*. Find predicted value for *x*, in $0^{th}/1^{st}/2^{nd}$ order predictor. 6

b) Simple code motions are noted in (A) and (B). Show compensation codes for both A and B. 4



c) Draw a data flow graph and packaged unit of templates for F = a + 200*(a+b)/(a-b). 2.5