Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 5th Semester Examinations, 2022

Computer Architecture and Organization -II (CS-3103)

Full marks: 50 Time: 3 hours

Answer any five

1. Define the 1-bit and 2-bit prediction schemes. The series of branch outcomes stored in an 1-bit prediction buffer is 11001101 (1 represents taken branch and 0 is for un-taken branch).
(i) Identify the predictions at each branch instruction execution.
(ii) Find out mis-predictions. Assume predictor is initialized as 0. Mention assumptions taken.
(iii) If the 2-bit prediction is considered and the predictor is initialized with 10, then find the number of mis-predictions for the same branch outcome 11001101. 10

2. Define `structural hazard' and `data hazard' in a pipeline system.
(i) Identify the cases of possible structural and data hazards in a 4-stage instruction pipeline shown in Figure 1.
(ii) Show how pipeline bubbles can effectively be used to avoid the structural hazard in the machine with only one memory port.
(iii) Show how data forwarding can be used to avoid data hazard in the machine. 10

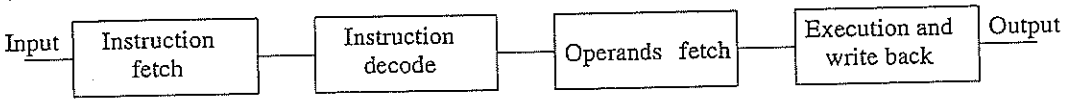

Figure 1

3a) A program consists of two nested loops, with only single branch instruction at the end of each loop. The outer loop is executed 100 times and the inner loop 200 times. Determine the accuracies of (i) Always predict taken, and (ii) Always predict not taken prediction strategies. 5

b) What do you mean by `exceptions'? Explain a case of out-of-order exceptions and the methodology for handling it in the instruction pipeline of Figure 1. 5

4a) Define compulsory cache miss. A program accesses each element of an 1024X1024 matrix 8 times in each course of its execution. If the data cache can accommodate 256 matrix elements and 16 matrix elements per block/page, then how many compulsory data cache misses are caused by this program's execution? 5

b) Show how loop interchange technique can reduce cache miss rate for the following nested loop

```
for (i = 1; i<101; i++)
    for (j = 1; j<4; j++)
        A[j][i] = B[i][1] * B[i+1][1];
```

Mention the assumptions taken. 5

5a) Describe in brief directory based protocol (with full directory) to ensure cache-coherence in a multi-processor system. Figure 2 shows a directory based cache system. Find out the number of bits in Directory A and B for- i) Full directory, ii) Limited directory, and iii) Chained directory. 5

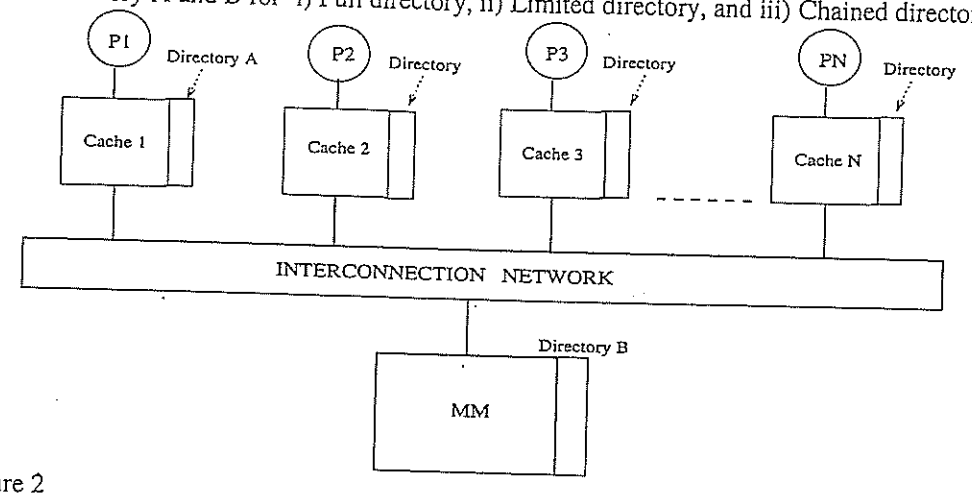

Figure 2

b) Describe the write-invalidate policy, implemented to enforce the cache coherence in a multiprocessor system. Evaluate performance of invalidation scheme in each of the following access patterns to variable V

i) Repeat a number of times: processor P1updates V and other 100 processors read the new value.
ii) Repeat a number of times: P1 updates V 100 times, then processor P5 only reads V. 5

6a) Define 1st and 2nd order predictor in context-based value predictor (CVP). Let sequence of values for a variable x is 1 1 1 2 2 3 4 3 1 1 1 2 2 3 1 1 1. Find the predicted value for x, in 1st and 2nd order predictor. 5

b) Define memory-wall in today's computation architectures. Introduce Near-memory Processing (NMP), Processing-in-Memory (PIM) and In-memory Computing (IMC) to address the issue of memory-wall. 5

7. Write short notes on the following

a) Uniform and Non-Uniform Memory Access system 3
b) Static and Dynamic Data Flow machine 3
c) CREW and ERCW Shared Memory SIMD m/c 4