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INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY, SHIBPUR
B.Tech. (CS) 5^{th} SEMESTER FINAL EXAMINATION 2019

MICROPROCESSOR BASED SYSTEMS (CS 503)

Full Marks: 70 Time: 3 Hours

Use a single answer script. Assume 8085A processor and its assembly language; if not specified. Two marks are reserved in each group for short and meaningful answers.

GROUP A : Answer any three questions from this group

1. a) The following program segment gets an interrupt request during the execution through RST 6.5 interrupt input line.

```
        ORG 2000H
        LXI SP, 0000H ; opcode of LXI SP is 31H
HERE:   JMP HERE      ; opcode of JMP is 0C3H
```

   If the CPU executes the ISR then what will be the start address of the ISR and the return address stored in the stack? Also, find the stack location(s) to store the return address.

   b) What are the *assembly time*, *load time*, and *run time* operations for the program given in 1 a). Explain with reason. [6+5]

2. a) Write a subroutine to multiply two 8-bit numbers available in B and C registers. Result should be returned through HL pair register.

   b) Write a subroutine that generates a delay using two loops (one nested inside the other). The 16-bit delay value is to be provided through B (upper byte of the delay value) and C (lower byte of the delay value) registers. Calculate the maximum delay possible using this sub-routine for a clock speed of 3 MHz. Assume, that the average execution time of any instruction is 4-T. [5+6]

3. a) Using a suitable diagram explain *bus contention*. What is a *wait state* and why is it provided? Draw the OF machine cycle with two *wait states*.

   b) Draw the timing diagram of the machine cycles (showing the content of the address and data buses in each cycle) needed to execute the CALL instruction in the following program segment.

```
        ORG     2000H
SAFEVAL EQU     8000H
DELAY   EQU     8500H
        LXI     SP, SAFEVAL
        CALL    DELAY; opcode for CALL is 0CDH
```

   [(2+2+2)+5]

4. a) Draw the ARM data flow model? Why is a 16-bit thumb instruction set provided? What happens to the value stored in r0 (=0) and r5(=0AH) if we execute the following ADD instruction.

```
ADD r0, r1, LSL #5
```

   b) Why conditional execution of arithmetic and logic instructions have been incorporated in ARM? Show the reduction in code size with aN example for computing GCD; i) in 8085A assembly and ii) ARM assembly. The GCD algorithm is *while* $(a! = b)$ *if* $(a > b)$ $a- = b$; *else* $b- = a$; $[(3 \times 2) + 5]$

5. a) A 3 to 8 decoder has 3 input lines (I_2, I_1, and I_0), 3 enable lines ($\overline{E_1}$, $\overline{E_2}$ and E_3) and 8 output lines ($\overline{O_0}, \overline{O_1} \ldots \overline{O_7}$). Show how this decoder can be used to detect the 7 different machine cycles (Opcode fetch to Bus idle).

   b) The devices that are to be interfaced with an 8085A CPU for a small system are one EPROM (1513 locations × 8-bit); one RAM (509 locations × 8-bit), one input Port (1 location × 8-bit) and one output Port (1 location × 8-bit). No fold-back in any form is permitted. Show the possible decoding arrangement. The memory map is also to be shown. [4 + 7]

GROUP B : Answer any three questions from this group

6. a) Draw the processor programming model of 8086. For the instructions given below find out the exact physical locations in memory used for reading or writing for the instructions marked with '*' in the comments.

```
mydata segment
var_0 dw 10 dup (?)
var_ 1 dw 1
mydata ends
mystack segment
dw 100 dup(0)
stack_top label word
mystack ends
mycode segment
start: mov ax, 1234H
mov bp, ax
mov bx, 4567H
mov sp, 98ABH
mov si, 0CDEFH
mov ax, var_1[bx][si] ; *
mov [bp][si], bx ; *
push ax ; *
.
.
mycode ends
```

Assume that the code, data and stack segment registers are pointing to the beginning of the segments, namely, mycode, mydata and mystack, respectively.

b) State with a suitable diagram the mechanism to compute the address of an ISR in X86 when interrupted through the INTR line. In an X86 based computer two X86 assembly language programs with the same code are executed. They operate on the same data array (16-bit, 40,000 element array) for implementing the same algorithm. While one program is taking 1 unit time the other takes 2 unit. What could be the reason(s) for this difference in execution times? [(3+4)+4]

7. a) What are the specialities of a micro-controller in comparison with a general purpose processor? What could be the implication of a short stack space implemented utilising 16 bytes of Data-memory space in MCS48 series micro-controllers?

b) Convert 4-bit decimal to 4-bit Gray code using a standard table driven code conversion technique. Write two sub-routines to accomplish the task; i) using 8085A; and ii) MCS-48 assembly languages, respectively. [(3+2)+6]

8. a) Compare RISC and CISC features. A 32 bit fixed length format is used in Berkeley RISC I architecture and only three different addressing modes are made available. Show the format of those three addressing modes with suitable instructions.

b) The DMA is done to transfer a block of data from Memory or I/O to Memory or I/O without the intervention of the CPU to save time. Compute the time required to transfer a 4 KB block from location X to location Y for a programmed data transfer in an 8085A based system. Assume any instruction takes 6T time. Compare the same if in the same system a DMA controller does a single byte transfer in 2T states. [(3+3)+5]

9. a) Write a subroutine PACK that packs the nibbles stored in B (b3 ...b0) and C (b3 ...b0) and returns the packed byte through Accumulator. B (b3 ... b0) and C (b3 ...b0) in higher and lower nibbles of A, respectively.

b) Write a subroutine UNPACK that unpacks the byte available in Accumulator (A) and stores the higher nibble of A in B (b3 ...b0) and lower nibble in C (b3 ...b0), respectively. [5+6]

10. Write short notes on – (i) Use of ROM as a decoder; (ii) Little endian and Big-endian systems; and (iii) Common data directives used in assembly language. [4+3+4]