30/4/17

Indian Institute of Engineering Science and Technology, Shibpur

Five year Dual Degree (BTech-MTech) 5th Semester Examinations, 2017

Subject: Computer Architecture and Organization II
Time: 3 hours

Paper: CS-502
Full marks: 70

Answer any four

1a) Describe method of broadcasting a message x in EREW and CRCW SIMD computer. Estimate the worst case search time to find the element x from a table of N elements in (i) EREW; (ii) CRCW SIMD computer. 10

b) How a data flow machine differs from control flow machine? Describe, in brief, the static model of data flow machine architecture with 32 processing elements and 256 cell blocks in memory section. 7.5

2a) Define MESI protocol. Explain when in MESI,
i) the cached copy of a block B is allowed to be modified?
ii) the cached copy of a block B can change its state from I to E on read miss for block B? 10

b) What is `victim cache'? Define cache `conflict miss'. Describe how introduction of a victim cache can reduce the conflict misses in a system. 7.5

3a) Define write-invalidate and write-through schemes for cache coherence. The following steps describe the values of X in cache 1 of processor P1, cache 2 of processor P2, and main memory (MM), of a multiprocessor system, after different activities in write-invalidate scheme for maintaining cache coherence. The cache write policy is the write-back and X is in main memory block BX.

Activity	X at cache 1	X at cache 2	X at MM
1. Initial state	20	-	20
2. P2 reads X	A	B	C
3. P1 writes X=0	D	E	F

Find A, B, C, D, E and F. 10

b) What is false sharing cache miss? `False sharing miss normally occurs in a system realizing the large block size and write-invalidate scheme for cache coherence' – Explain. 7.5

4a) Define `control hazard' in a pipeline system. Describe the `predict taken' and `predict not-taken' schemes. Evaluate the performance of these two in reducing pipeline branch penalties. 10

b) Define RAW, WAR, and WAW data hazards. Consider the following code sequence:
ADD R0, R1, R2 (R0 is the destination register)
MOVE R2, R0 (R2 is the destination register)
Identify the possible data hazards. 7.5

Pg 1/2

5a) Consider the following loop

```
for i = 1 to n with increment 2 do
    f ();
```

Unroll the loop by inserting 4 copies of the body f () for (i) n = 104; (ii) n = 103. 5

b) Take the following example program segments (i) and (ii)

```
(i) for i = 1 to 100 do
      X[i] = X[i] * Y[i];
    for i = 1 to 100 do
      Y[i] = X[i] * X[i];

(ii) for i = 1 to 100 do
       begin
         X[i] = X[i] * Y[i];
         Y[i] = X[i] * X[i];
       end
```

Compute the total number of cache misses during execution of (i) and (ii). Assume each element of X and Y forms a memory block and the cache can accommodate one element of X and one element of Y at a time. 5

c) Describe, in brief, the loop interchange technique to reduce cache miss rate. 7.5

6a) State key features of *in-order-issue in-order-completion, in-order-issue out-of-order-completion, and out-of-order issue out-of-order-completion* superscalar schemes. 5

b) Describe directory based protocol (with fullmap directory) to ensure cache-coherence in a multi-processor system. 7

c) What is `delta' network? Compute the number of 4x3 elementary switches in a 4^3x3^3 delta network. 5.5

7. Write short notes on the following

a) UCA and NUCA 10

b) Data speculation to increase parallelism in execution 7.5