Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 5th Semester Examinations, November 2023

Computer Architecture and Organization -II (CS-3103)

Full marks: 50 Time: 3 hours

Answer any five

1a) Define delta-network. Construct the 8x8 delta-network with 2x2 elementary switches. There is an *nxm* delta-network. How many stages and switches per stage are there in the *nxm* delta-network? State assumptions taken and any relation between *n* and *m*. 5

b) Define Stride value predictor (SVP) and 2nd order predictor in context-based value predictor (CVP). Let sequence of values loaded to *x* in different time steps is 1, 2, 3, 4, 1, 2, 3, 1, 2, 3, 4. Find number of mis-speculations in SVP and value predicted for *x* in SVP and 2nd order CVP. 5

2a) What are the RAW and WAR in data-hazard? Consider a pipelined processor with 4 stages: Instruction Fetch (IF), Instruction Decode/Operand Fetch (ID), Execute (EX) and Write Back (WB). IF, ID and WB stages take 1 clock cycle to complete the operation. In EX stage, number of clock cycles needed for ADD (+)/SUB (-) instruction is 1 and for MUL (*) instruction it is 3. The data forwarding is used in this processor. Find cases of RAW and WAR, and show execution of following sequence of instructions in the pipelined processor in different clock cycles. 5

I1: R6 <--- R0 + R2
I2: R3 <--- R1* R6
I3: R4 <--- R5 - R4

b) Define 'predict taken' and 'predict not-taken' schemes, used to address control hazard. Consider the program segment: I1, I2, I3, I4, I5, I6, I7, I8, I9, ... I1 is a conditional branch instruction - JUMP to I5 IF C. Show execution of the program segment in a 4-stage (IF, ID, OF and EX) pipelined processor when (i) predict taken, (ii) predict not-taken is followed in different clock cycles. Assume that the status of condition C can be known in OF stage of I1. 5

3a) A program consists of two nested loops, with only single branch instruction at the end of each loop. The outer loop is executed 100 times and the inner loop 200 times. Determine the accuracy of (i) Always predict taken, and (ii) Always predict not taken prediction strategies. 5

b) What do you mean by `exceptions'? Explain a case of out-of-order exceptions and the methodology for handling it in the instruction pipeline. 5

4a) Take following program segment

```
for (i = 1; i<100; i++)
   A[i] = A[i] * B[i];
for (j = 1; j<100; j++)
   B[j] = A[j] * A[j];
```

Each A[i]/B[i] forms a block. If the program segment is executed in a system with only two cache frames (blocks), one for A[i]s and the other for B[i]s, then compute total number of cache misses during execution. Perform loop fusion and then compute number of such misses. 5

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b) Define false sharing miss. Consider bus-based shared memory (M) system consisting of two processors P1 and P2. Let assume that words X1 and X2 are in the same block B. Block B is in the caches C1 and C2 of P1 and P2 at time step 0. For following sequence of events, identify each miss as a true sharing miss, a false sharing miss, or a hit in a Write-Invalidate protocol:

P1 writes X1, P1 reads X2, P2 reads X2, P1 writes X1, P2 writes X2, and P1 reads X2.

5a) Define 4-state MESI protocol. Consider a bus based shared memory system consisting of two processors P1 and P2 with caches Cache1 and Cache2. Cache1/Cache2 can fit only one block at any given time. The shared memory in divided into three blocks A, B, C and contains shared variables X in A, Y in B, and Z in C respectively. Each block can be in any one of the MESI protocol states. The variables in shared memory are initialized as X=1, Y=2, and Z=3; but caches are empty. The system follows write-invalidate scheme. The following events are occurred

(1) P1 reads X, (2) P2 reads X, (3) P2 updates X=X+5, (4) P1 reads Y,
(5) P2 reads X, (6) P1 updates X=X-20

Show contents of caches and memory after each event. Mention clearly assumptions taken. 5

b) Define code motion in trace scheduling. Consider the simple code motions (reorder) noted in Figure 1(A) and (B)

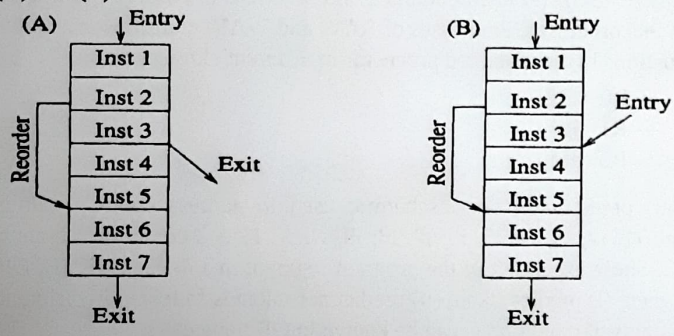

Figure 1

Find compensation at the side Exit of Figure 1(A) and side Entry at Figure 1(B). 5

6a) Indicate basic features of an ERCW shared memory SIMD computer. Describe method of broadcasting a message in such an SIMD computer. Find time complexity of broadcasting. 5

b) Show the organization (interconnection only) of an SIMD machine with 16 PEs (PE0 to PE15), using perfect shuffle interconnection network. If shuffle interconnection function is executed 2 times, in which PE the data item *x* is located? The *x* originally was in PE6. If perfect shuffle SIMD machine is of 64 PEs and the shuffle interconnection function is executed 5 times, in which PE the data item can be located that originally was in PE31. 5

7. Write short notes on the following

a) Near-memory Processing, Processing-in-Memory and In-memory Computing 4
b) True gate, False gate, Merge gate and Switch in DFG 3
c) Early restart and critical world first in reducing cache miss penalty 3

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