3/12/18

Indian Institute of Engineering Science and Technology, Shibpur
Five year Dual Degree (BTech-MTech) 5th Semester Examinations, 2018

Subject: Computer Architecture and Organization II — Paper: CS-502
Time: 3 hours — Full marks: 70

Answer all questions. All the questions except Q4 are of MCQ type.
There may be more than one choice, given against an MCQ type question, are correct.
Choose all the correct choices. Then show computation/give justification of your answer.

1. Answer any 10. Each carries 2 marks. 20

a) Comparing the time T1 taken for execution of a single instruction on a pipelined CPU with time T2 taken on a non-pipelined but identical CPU, it can be commented that the relation between T1 and T2 may be

(A) T1 < T2, (B) T1 = 2*T2, (C) T1 = 3*T2, (D) T1 = 4*T2

b) CPI of two pipelined base scalar processors (P1 and P2), P1with 4-stage instruction pipeline and the P2 with 8-stage instruction pipeline are

(A) 1 and 2, (B) 1 and ½, (C) ½ and 1, (D) 1 and 1.

c) The hit time in pseudo-associative cache is almost same as that of

(A) A fully associative cache based system, (B) 4-way associative cache based system,
(C) 8-way associative cache based system, (D) Direct-mapped cache based system.

d) In 4-state MESI protocol, if the state of a cached block B in processor P*i* is "Exclusive" after P*i* has read-hit on B, then what will be the state of the cached data block B in P*i* after P*i* writes B?

(A) Shared, (B) Exclusive, (C) Modified, (D) Invalid.

e) A program is having 200 blocks. It needs all the blocks during execution. The cache follows associative mapping. The cache size is of 4 blocks. The execution of the program encounters

(A) Unlimited compulsory misses, (B) 100 compulsory misses,
(C) 200 compulsory misses, (D) unknown number of compulsory misses.

f) Merging of arrays

(A) reduces capacity and conflict miss, (B) reduces compulsory and conflict miss,
(C) reduces capacity and compulsory miss, (D) reduces compulsory, capacity and conflict miss.

g) False sharing cache miss normally occurs in a system realizing the

(A) large block size and write-invalidate scheme, (B) large block size and write-update scheme,
(C) small block size &write-invalidate scheme, (D) small block size and write-update scheme.

h) Higher associativity of cache reduces

(A) Conflict misses, (B) Compulsory misses, (C) Capacity misses,
(D) Both compulsory and capacity misses.

i) In the pipeline execution of following code sequence

ADD R0, R1, R2; (R0 = R1+R2)
MOVE R2, R0; (R2 = R0)

the type of possible data hazards are

(A) RAW and WAR, (B) RAW and WAW, (C) WAR and WAW, (D) None.

j) The selection of candidate for branch delay slot from

(A) The target is preferred when there is high probability that the branch will be taken,
(B) The not-taken zone of branch is preferred when probability of untaken branch is very high,
(C) The instructions appear before the branch instruction in original program is the best choice.

k) Let consider an SIMD computer with 8 processing elements (PE0 to PE7), realizing shuffle-exchange network. The number of shuffle/exchange operation needed to transfer an information from PE2 to PE5 is

(A) 1, (B) 2, (C) 3, (D) 8.

l) Based on the instruction issue policy, the superscalar processors are categorized as:

(A)In-order issue, in-order-completion superscalar computer,
(B)In-order issue, out-of-order-completion superscalar computer,
(C)Out-of-order issue, in-order-completion superscalar computer,
(D)Out-of-order issue, out-of-order-completion superscalar computer.

Which one of the above 4 is never considered.

2. Answer any 10. Each carries 3 marks. 30

a) The series of branch outcomes stored in an 1-bit prediction buffer is 11111110 (1 represents taken branch and 0 is for un-taken branch). When the predictor is initialized as 0 then the number of mis-predictions is - (A) 8, (B) 7, (C) 2, (D) 1.

b) In the following loop

```
for i= 1 to 100 with increment 2
begin
  A[i] = A[i] * B[i];     .....(1)
  B[i+1] = C[i] * D[i];   .....(2)
end
```

(A) There is no loop-carried dependence, (B) There is loop-carried dependence from (2) and (1)
(C) There is a loop-carried dependence from (1) and (2),
(D) There is loop-carried dependence from (2) and (1) and from (1) to (2)

c) The following are the four instructions in sequence

I1: A = B + C; I2: C = A * B; I3: D = A + C; I4: A = B * C.

How many unique comparisons (between register sources and destinations) are necessary to find all of the RAW dependence. Assume that all instructions have one register destination and two register sources. (A) 3, (B) 6, (C) 12, (D) Can not be computed.

d) A cache access requires one clock cycle and a cache miss stalls the processor for five cycles, which of the following cache hit rates comes closest to achieve an average memory access of 2 cycles? (A) 75, (B) 80, (C) 83, (D) 86.

e) An EREW shared memory SIMD computer consists of two processing elements (PE1 and PE2). Its shared memory M stores x at location l. Both the PEs executes "add [l] + 5". The minimum time taken to finish this computation at the PEs is

(A) 1-unit, (B) 2-units, (C) 3-unit, (D) None of these.

f) In a 4^2X3^2 delta network, the number of 4^2X3^2 elementary switches required is

(A) 7, (B) 9, (C) 12, (D) 16

g) Consider the following loop

for i=0 to n with increment 1 do

$f()$;

When unrolled the loop by inserting 4 copies of the body $f()$; for (i) n = 104 and (ii) n = 103, then the number of loop iterations reduced in these cases to

(A) 26 and 25, (B) 26 and 26, (C) 26 and 28, (D) None of these.

h) Let the total number of memory references is = 10000 and the number of misses at L1 and L2 are 200 and 40 respectively. Then the miss rate_(local or global) at L1, missrate_local at L2 and missrate_global at L2 are

(A) 0.02, 0.02 & 0.02; (B) 0.02, 0.20 & 0.20; (C) 0.02, 0.004 & 0.20; (D) 0.02, 0.20 & 0.004

i) A multi-processor system with 2048-core processors implements "full-map" directory protocol for its cache system, in which directory contains a pointer to every cache. The memory block/ cache line size is 128 bytes. How many directory state bits are required to track which caches are sharing a given block of memory and what is the ratio of directory state bits to data bits?

(A) 11 and 7:11, (B) 256 and 2:1, (C) 2048 and 7:11, (D) 2048 and 2:1.

j) An 8KB direct mapped write-back cache is organized as multiple blocks, each of size 32-bytes. The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprising of 1 valid bit and 1 modified bit. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

(A) 4864 bits, (B) 6144 bits, (C) 6656 bits, (D) 5376 bits.

k) The following steps describe the values of X in cache 1, cache 2, and MM (of a multiprocessor system) after different activities in write-invalidate scheme. The cache write policy is write-back.

Activity	X at cache 1	X at cache 2	X at MM
1. Initial state	20	Invalid	20
2. P2 reads X	20	20	20
3. P1 writes X=0	X	Y	Z

The X, Y and Z in activity 3 are: (A) 0, 20, 20; (B) 0, 0, 20; (C) 0, 0, 0; (D) 0, Invalid, 20.

l) An EREW shared memory SIMD computer consists of two processing elements (PE1 and PE2). At time t the permissible access to a memory locations l and k is

(A) PE1 and PE2 read l, (B) PE1 reads l and PE2 reads k,

(C) PE1 reads l and PE2 writes to k, (D) Both (B) and (C) but not (A).

3. Answer any one. 4

a) Consider the bus-based shared memory shown in Fig. 1. Let assume that the words X1 and X2 are in the same block B. The block B is in the caches (Cs) of P1 and P2 at time step 0. For the following sequence of events, identify false sharing miss in a Write-Invalidate protocol.

Time step	Event	Bus activity (cache miss/hit false/true)
1.	P1 updates X1	
2.	P1 reads X2	
3.	P2 reads X2	
4.	P1 updates X1	
5.	P2 updates X2	
6.	P1 reads X2	

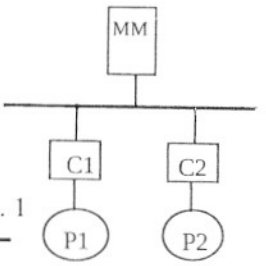

Fig. 1

(A) At time step 3, 5; (B) At time step 3, 5, 6; (C) At time step 2, 3, 5; (D) At time step 1, 4, 5.

b) A multi-processor system with 2048-core processors implements limited directory protocol for its cache system. It allows up to 8 cores to have a cached copy of a block. The memory block/ cache line size is 128 bytes. How many directory state bits are required to track which caches are sharing a given block of memory and what is the ratio of directory state bits to data bits?

(A) 256 and 2:1, (B) 2048 and 2:1, (C) 96 and 3:32, (D) 2048 and 3:32.

4. Write short notes on any two of the following 2x8 =16

a) Superscalar vs superpipelined processor.
b) VLIW execution for degree 3.
c) Dataflow machine.