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(2021CSB043)

Indian Institute of Engineering Science and Technology, Shibpur  
BTech (CST) 6<sup>th</sup> Semester Mid Semester Examination, February 2024

Subject: Computing-in-Memory Architecture (CS-3223)  
Full marks: 30

Time: 2 hours

Answer all

- ✓ 1a) Show the construction of  $n$ -channel depletion-type MOSFET. Apply proper drain-to-source voltage and sketch the flow of electrons for  $V_{GS} = 0V$ . 4
- b) Sketch a  $n$ -channel enhancement-type MOSFET with the proper biasing applied ( $V_{DS} > 0V$ ,  $V_{GS} > V_T$ ) and indicate the channel, the direction of electron flow, and the resulting depletion region. 4
- ✓ 2a) In CPU-centric von Neumann computing model, define power wall, memory wall and ILP walls. 4
- b) Introduce Near-memory Processing (NMP), Processing-in-Memory (PIM) and In-memory Computing (IMC). Identify the working set locations in such computing systems. 2
- ✓ 3 Show the ROC architecture (DRAM-based Processing with Reduced Operation Cycles) that can support bit-wise in-memory computing for basic logic operations including NOT, AND, and OR. Explain how  $A + B$  and  $A.B$  (each  $A/B$  is of 1-bit) can be realized in the ROC. 6
- ✓ 4a) Show the structure of 6T SRAM cell. Design a logic circuit that can perform In-SRAM logical AND and NOR operations. 5
- b) Define basic mechanism and the components of an ANN. Describe the ANN architecture of the binary radix design. 5