



Empowering Innovation with Generated Model for Virtual Silicon and DTCO

Hockchen 2023

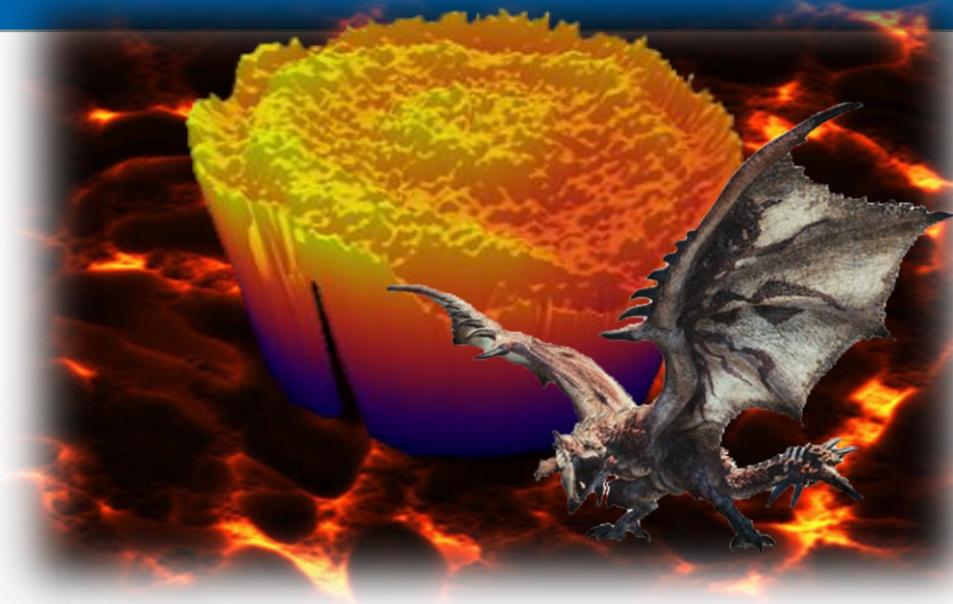
Background

■ Chip design challenges

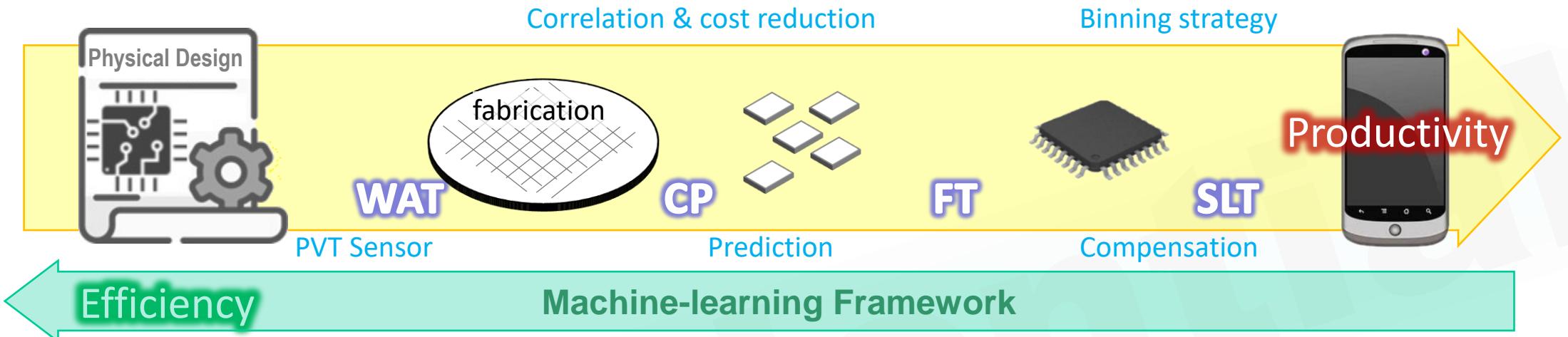
- Design margin (signoff method)
- Silicon and model mismatch
- Process and design co-optimization methods

■ Our contribution (opportunity)

- On-chip sensor IP and data analysis platform
- ML framework for design & production strategy
- Metric extraction & generated model for EDA industry

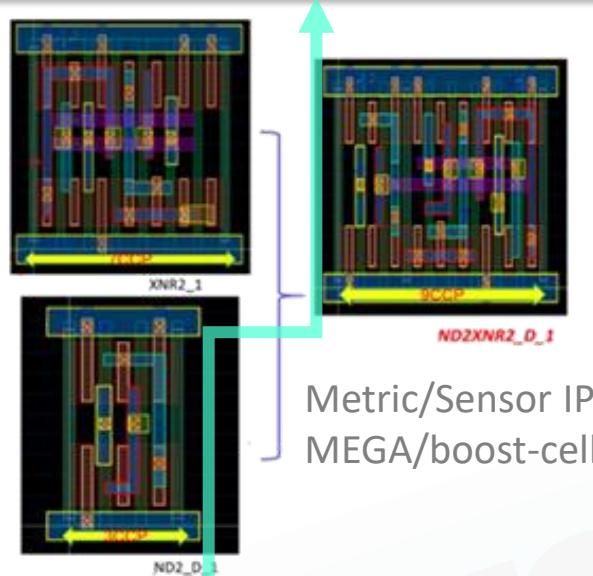


Productivity and Efficiency



Design for Efficiency

IP/Custom Cell



Voltage stacking

Ldi/dt

Custom Cell

Design Recipe (Margin)

Process Management

Ldi/dt

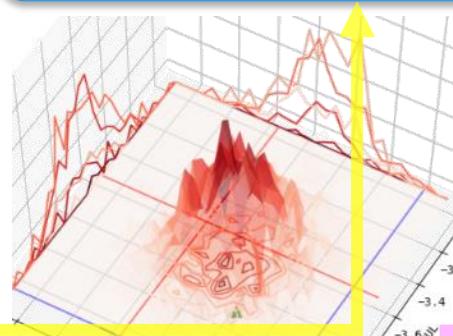
Library

Physical Design

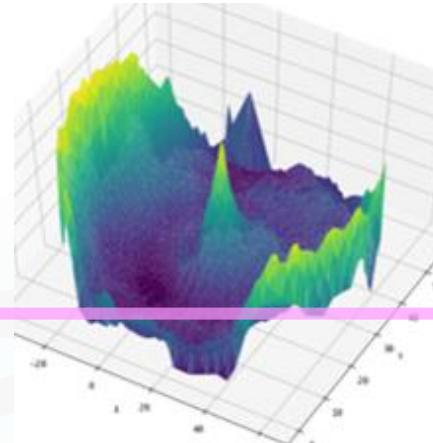
Process Variation

Energy Efficiency (J/T)

Design Methodology

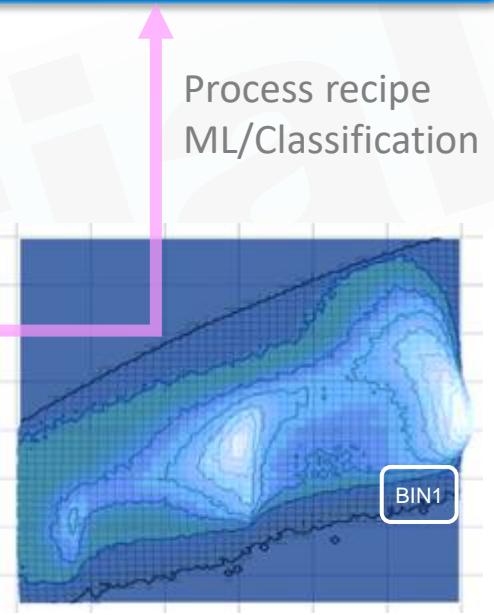


Data science/S2S
WAT/CP correlation



Uniformity/OCV
Design margin

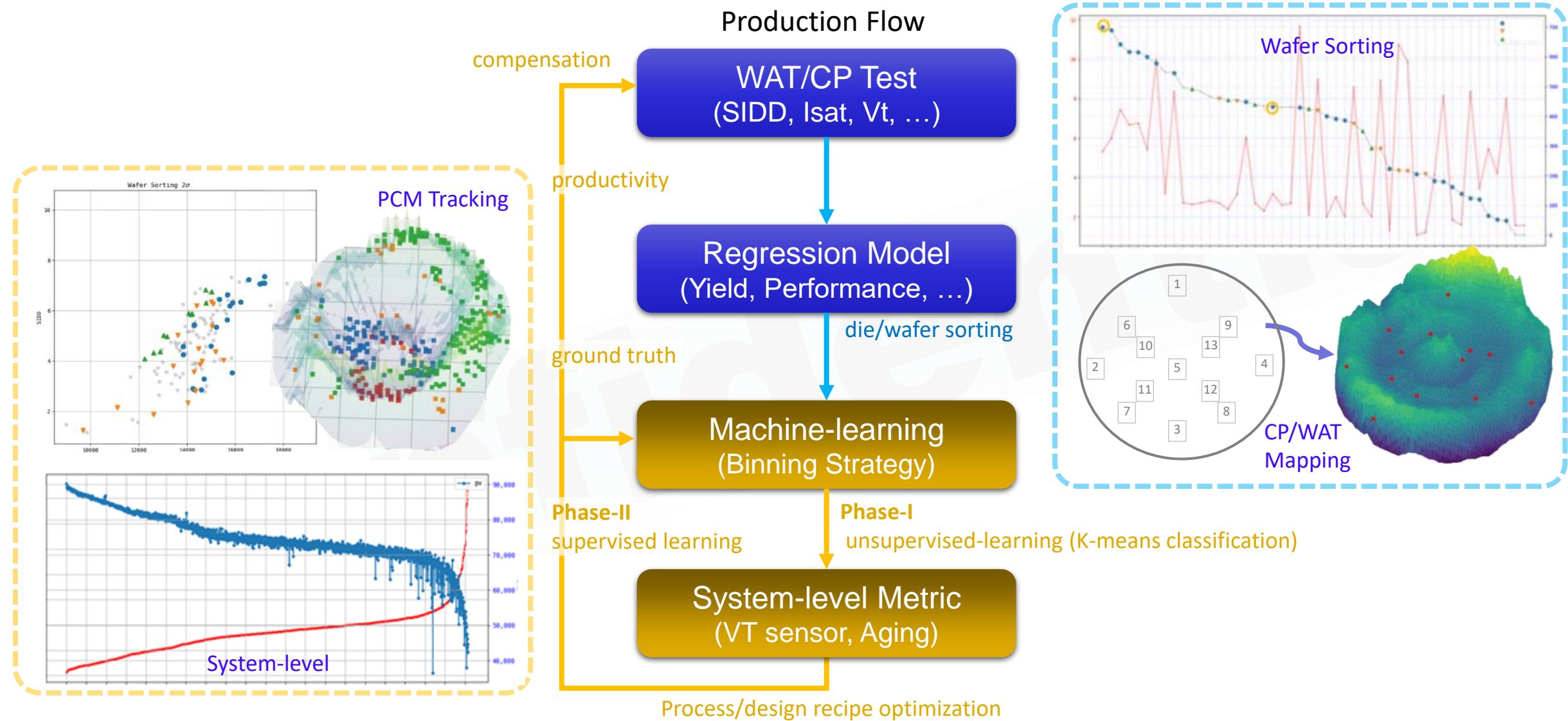
Binning Strategy



Process recipe
ML/Classification

Vmin reduction &
Supporting measures

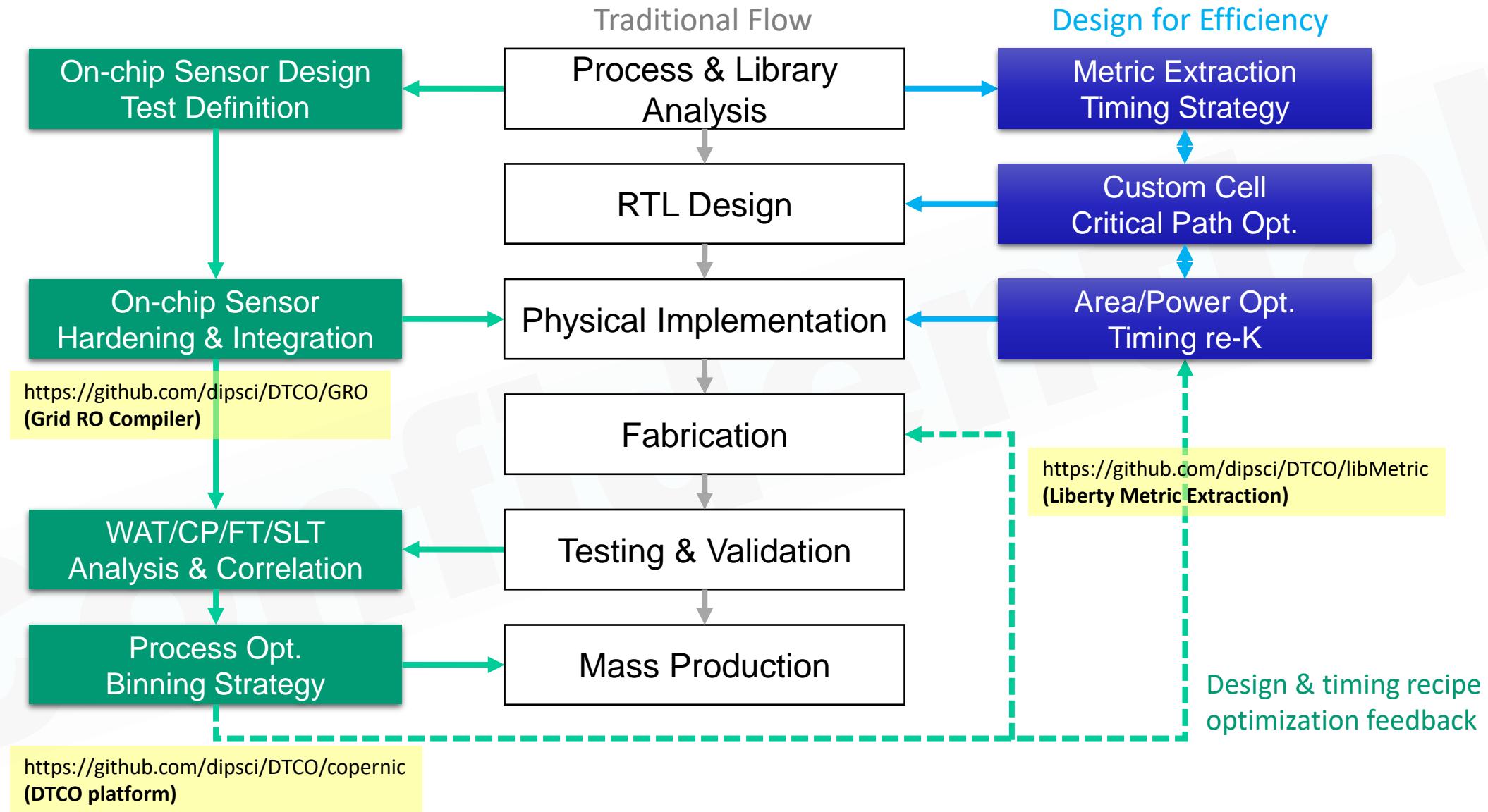
Binning Strategy Optimization



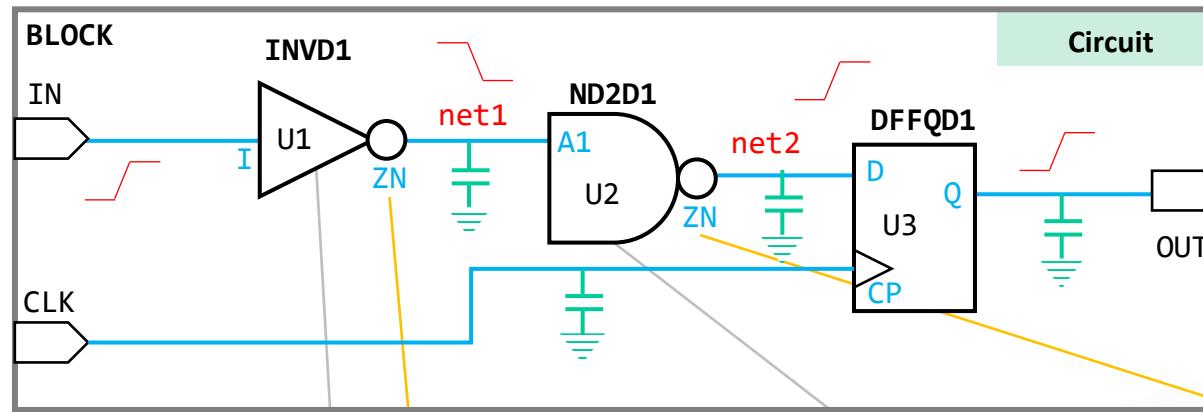
DTCO Platform

Python Package
% pip install DTCO

https://www.youtube.com/watch?v=QmqQt_fVaOA
(2021 NTU: Design for Efficiency)



Physical Design (Design Metric)



```
module BLOCK(IN, OUT, CLK);
    input IN, CLK;
    output OUT;
    INVD1 U1 ( .I(IN), .ZN(net1) );
    ND2D1 U2 ( .A1(net1), .ZN(net2) );
    DFFQD1 U3 ( .D(net2), .CP(CLK), .Q(OUT) );
endmodule
```

Verilog Model

Delay ('I,ZN,' , 'combinational', 'cell_fall')

```
Trans: [0.0032, 0.0079, 0.0173, 0.036 , 0.0735, 0.149, 0.3, 0.6]
Load: [0.0002, 0.0005, 0.0012 , 0.003, 0.005, 0.01, 0.02, 0.04]
Value:[[0.011, 0.016, 0.024, 0.041, 0.075, 0.143, 0.278, 0.53],
[0.014, 0.019, 0.028, 0.045, 0.079, 0.146, 0.281, 0.54],
[0.019, 0.025, 0.034, 0.052, 0.085, 0.153, 0.288, 0.55],
[0.028, 0.034, 0.045, 0.064, 0.099, 0.167, 0.302, 0.57],
[0.043, 0.051, 0.064, 0.085, 0.123, 0.194, 0.329, 0.61],
[0.068, 0.082, 0.097, 0.122, 0.166, 0.242, 0.383, 0.65],
[0.103, 0.125, 0.153, 0.189, 0.239, 0.326, 0.481, 0.76],
[0.153, 0.191, 0.239, 0.298, 0.371, 0.472, 0.648, 0.95]]
```

Trans ('A1,ZN,' , 'combinational', 'rise_transition')

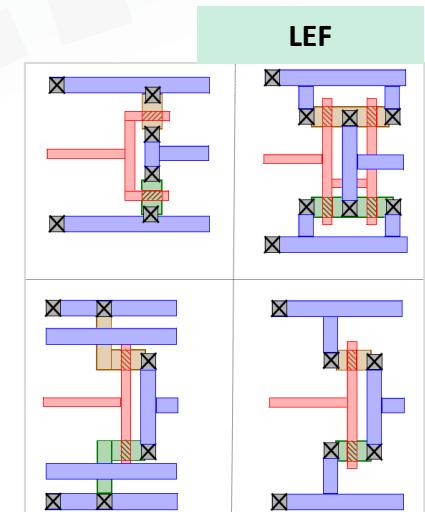
```
Trans: [0.0032, 0.0079, 0.0173, 0.036 , 0.0735, 0.149, 0.3, 0.6]
Load: [0.0002, 0.0004, 0.001, 0.002, 0.004, 0.007, 0.015, 0.03]
Value:[[0.015, 0.022, 0.035, 0.061, 0.111, 0.216, 0.427, 0.841],
[0.016, 0.022, 0.035, 0.061, 0.112, 0.217, 0.427, 0.842],
[0.018, 0.024, 0.037, 0.062, 0.113, 0.218, 0.426, 0.843],
[0.021, 0.028, 0.041, 0.066, 0.116, 0.218, 0.427, 0.844],
[0.025, 0.032, 0.047, 0.074, 0.124, 0.224, 0.429, 0.845],
[0.04 , 0.045, 0.056, 0.086, 0.141, 0.241, 0.441, 0.847],
[0.07 , 0.077, 0.088, 0.107, 0.163, 0.274, 0.475, 0.872],
[0.126, 0.138, 0.153, 0.176, 0.211, 0.318, 0.541, 0.944]]
```

Trans ('I,ZN,' , 'combinational', 'fall_transition')

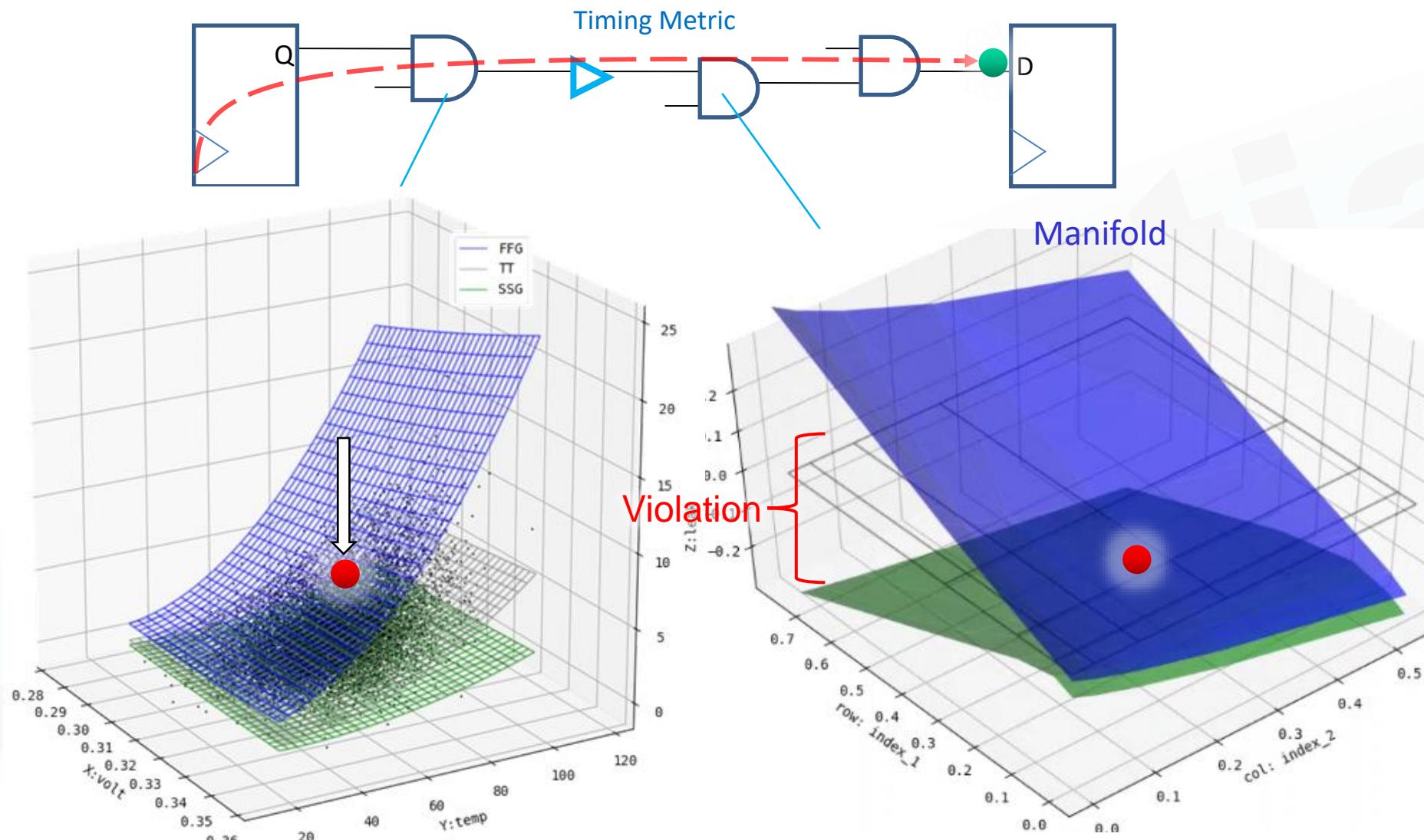
```
Trans: [0.0032, 0.0079, 0.0173, 0.036 , 0.0735, 0.149, 0.3, 0.6]
Load: [0.0002, 0.0005, 0.0012 , 0.003, 0.005, 0.01, 0.02, 0.04]
Value:[[0.010, 0.017, 0.032, 0.062, 0.121, 0.241, 0.472, 0.91],
[0.011, 0.018, 0.033, 0.062, 0.121, 0.242, 0.473, 0.92],
[0.012, 0.021, 0.034, 0.063, 0.121, 0.243, 0.474, 0.93],
[0.014, 0.023, 0.038, 0.067, 0.124, 0.244, 0.475, 0.94],
[0.021, 0.027, 0.044, 0.074, 0.131, 0.245, 0.476, 0.95],
[0.035, 0.043, 0.054, 0.086, 0.147, 0.261, 0.487, 0.96],
[0.063, 0.073, 0.087, 0.109, 0.172, 0.293, 0.521, 0.97],
[0.112, 0.129, 0.151, 0.178, 0.219, 0.337, 0.584, 1.04]]
```

Delay ('A1,ZN,' , 'combinational', 'cell_rise')

```
Trans: [0.0032, 0.0079, 0.0173, 0.036 , 0.0735, 0.149, 0.3, 0.6]
Load: [0.0002, 0.0004, 0.001, 0.002, 0.004, 0.007, 0.015, 0.03]
Value:[[0.016, 0.021, 0.027, 0.042, 0.071, 0.131, 0.249, 0.485],
[0.019, 0.023, 0.031, 0.045, 0.075, 0.134, 0.252, 0.489],
[0.025, 0.029, 0.037, 0.052, 0.082, 0.141, 0.259, 0.496],
[0.034, 0.039, 0.048, 0.065, 0.096, 0.155, 0.274, 0.511],
[0.051, 0.057, 0.068, 0.087, 0.121, 0.183, 0.303, 0.539],
[0.081, 0.091, 0.103, 0.125, 0.164, 0.233, 0.357, 0.596],
[0.127, 0.142, 0.164, 0.193, 0.239, 0.318, 0.456, 0.706],
[0.196, 0.222, 0.259, 0.309, 0.375, 0.466, 0.626, 0.903]]
```

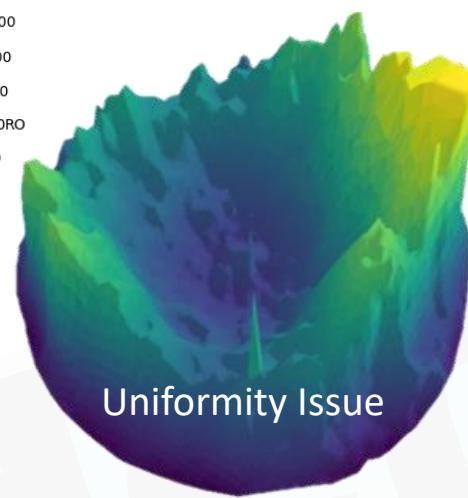
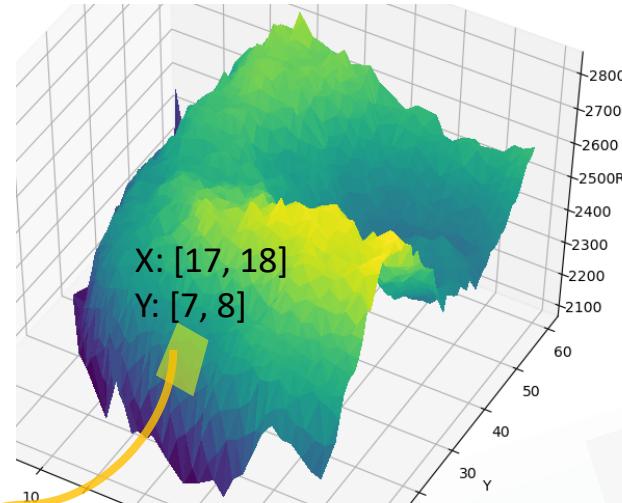
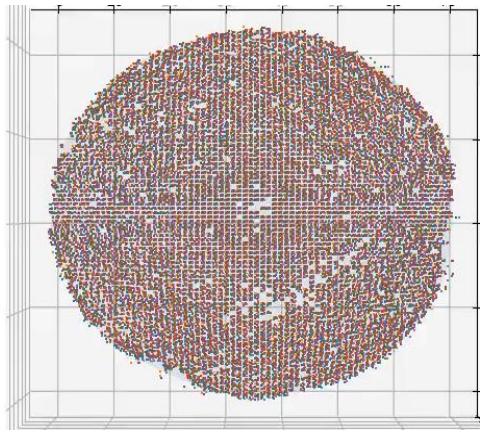


Metric Extraction & Optimization

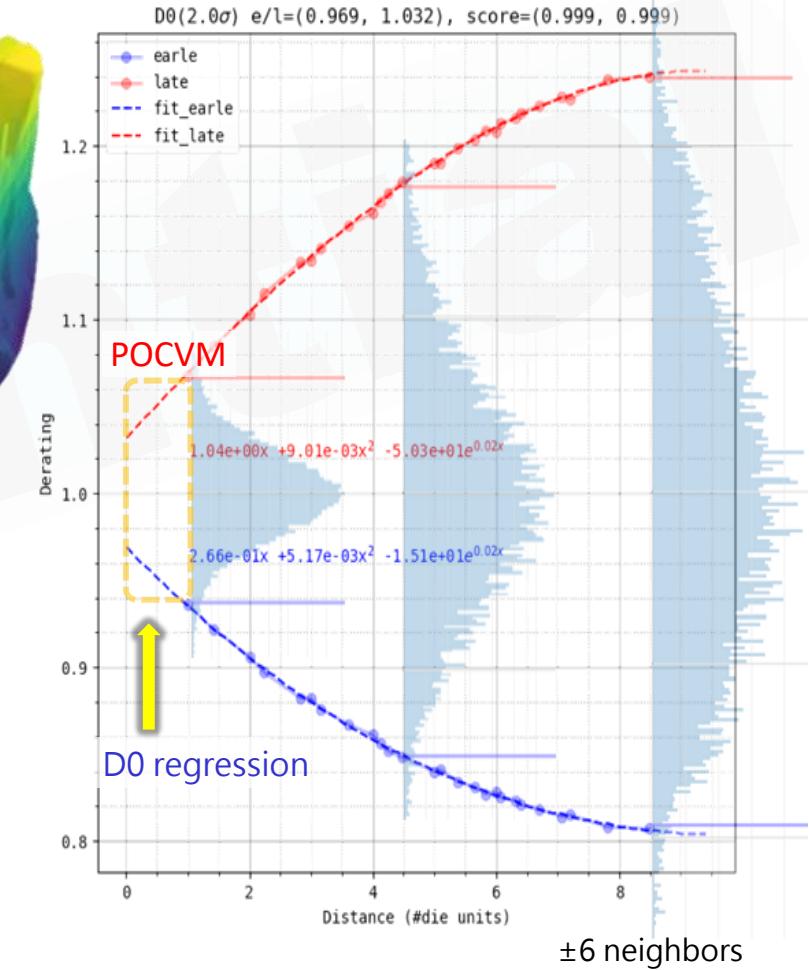


On-chip Sensor and Data Analysis

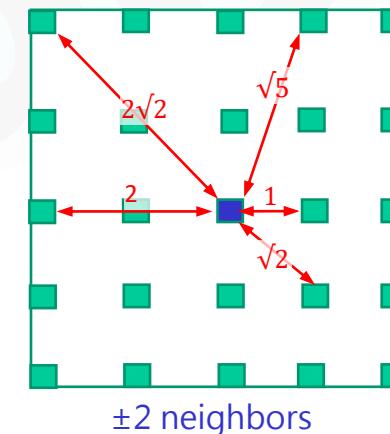
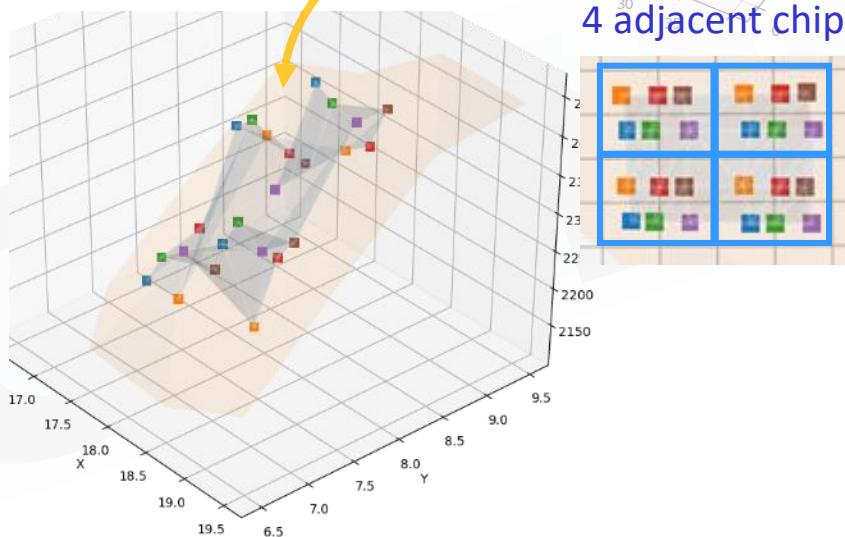
On-chip RO



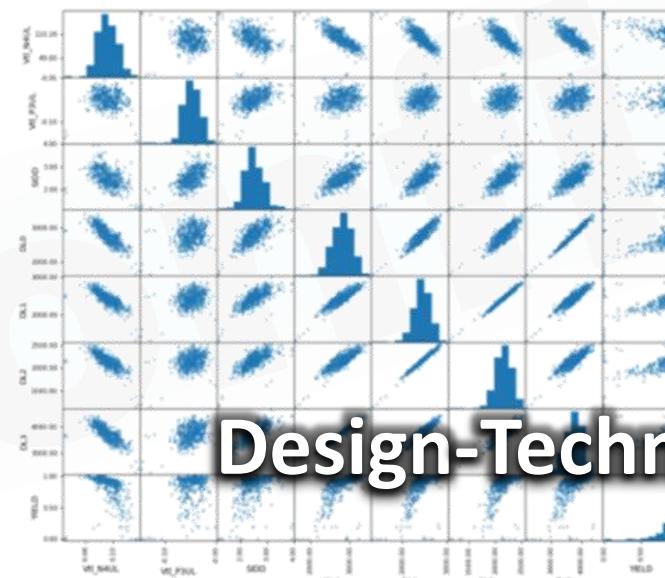
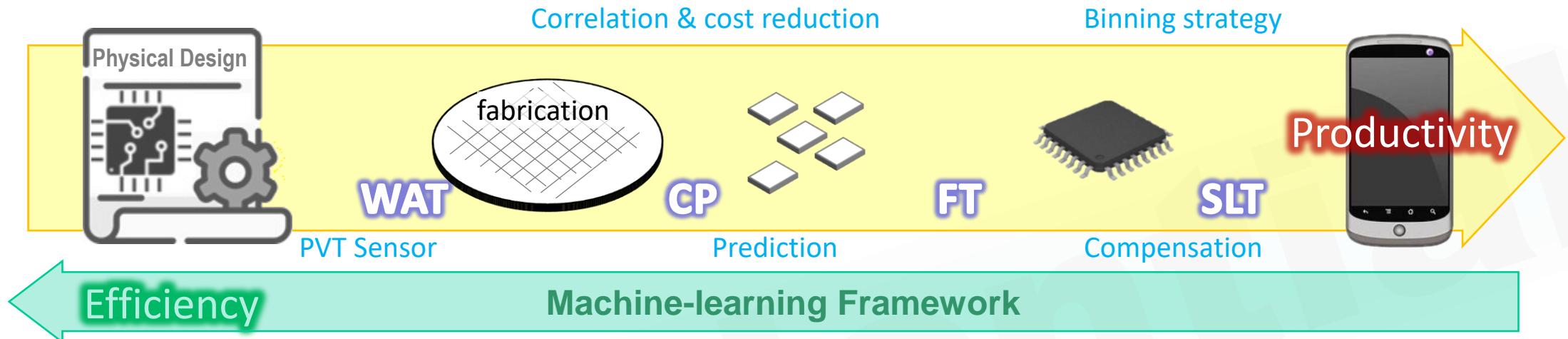
OCV regression



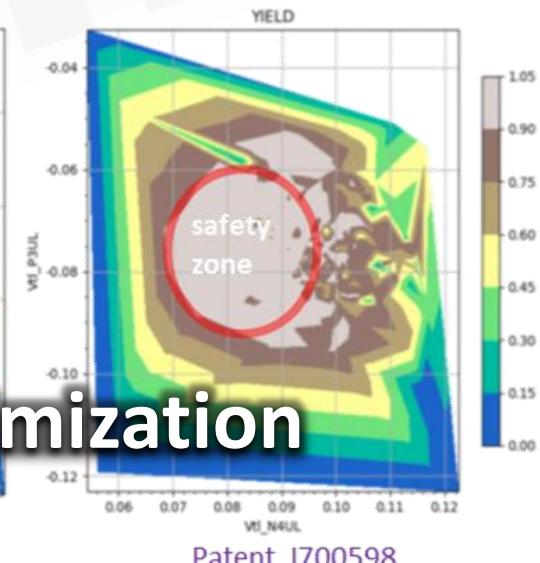
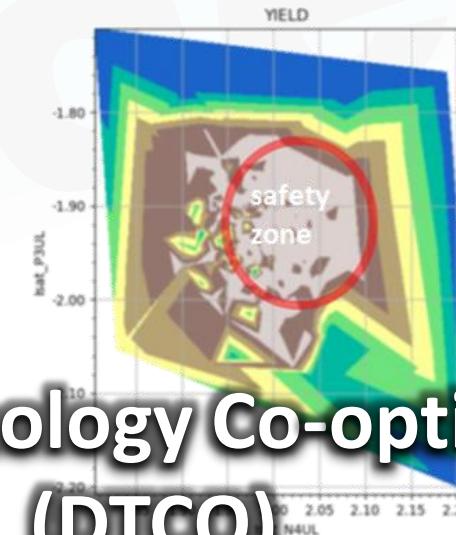
feature surface



Productivity and Efficiency

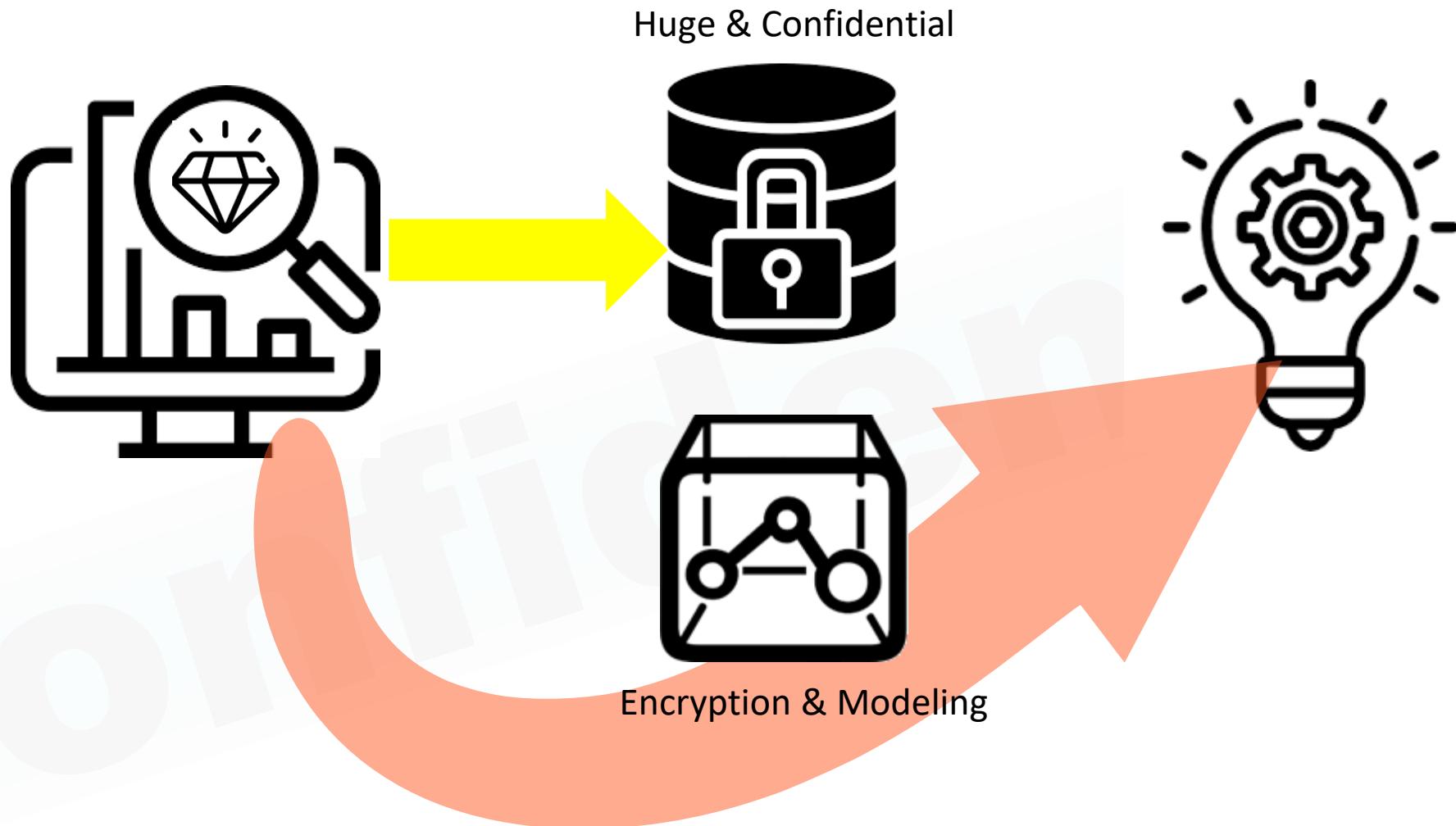


Design-Technology Co-optimization
(DTCO)

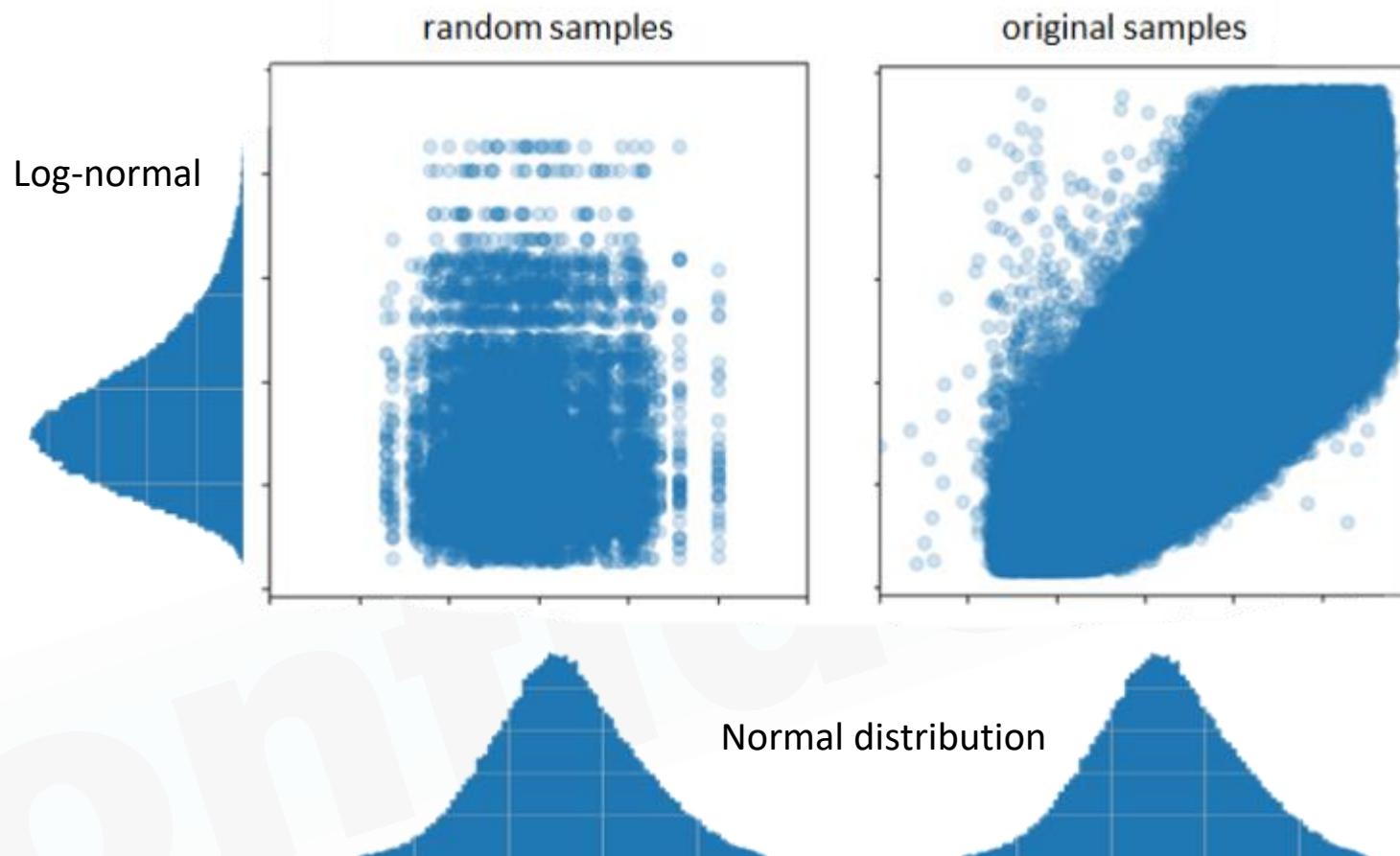


Patent, I700598

Data Acquisition Barriers

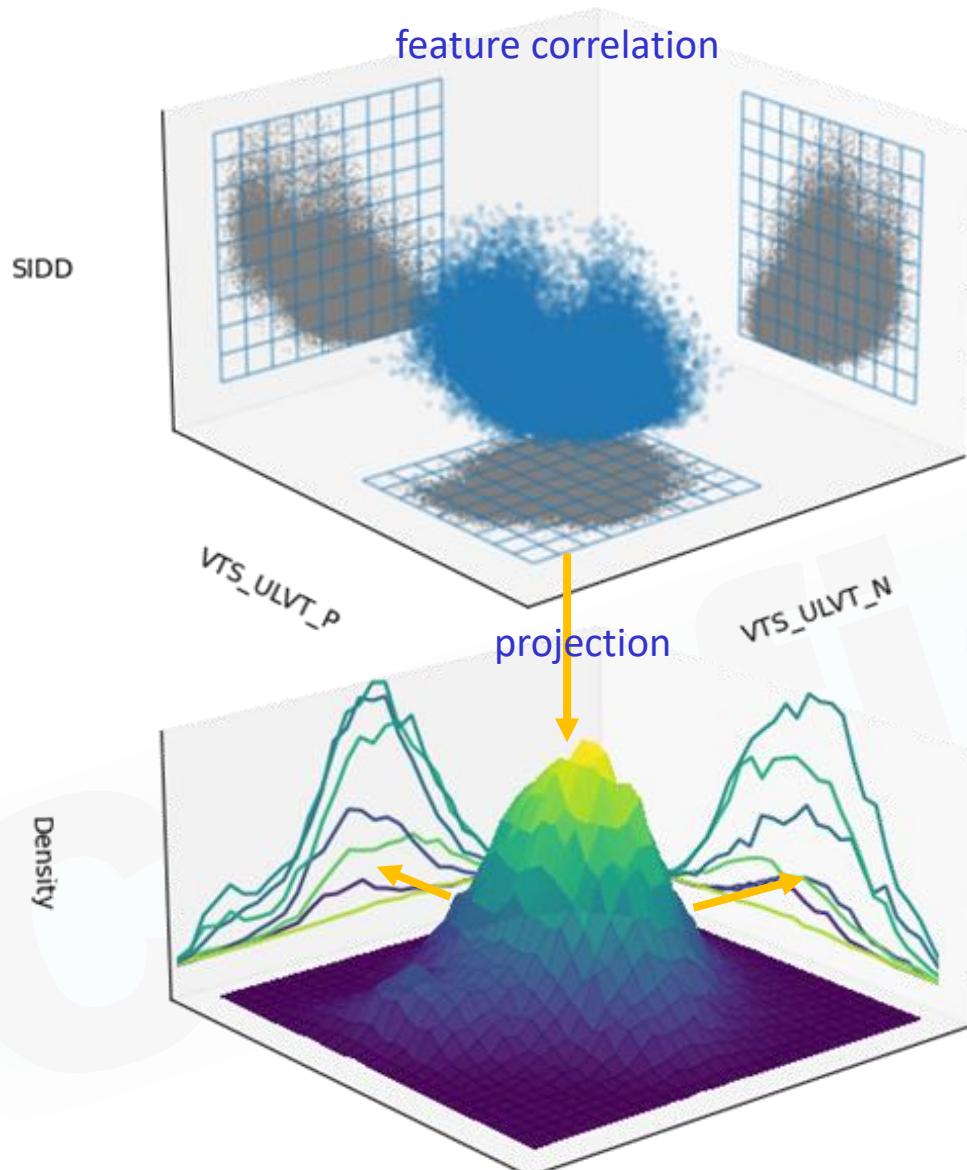


Multi-feature Data Modeling



Features can't be randomized individually; their distributions must match the parent set's as they are interdependent.

Feature Distribution and Correlation



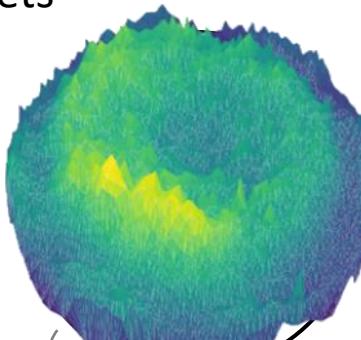
1. The probability distributions of features in each dimension follow the parent samples
2. The correlation distribution between any two features adheres to that of the parent samples
3. The correlation distribution among selected features in high-dimensional space conforms to the distribution observed in the parent samples

Dissipation of Feature Spatial Continuity

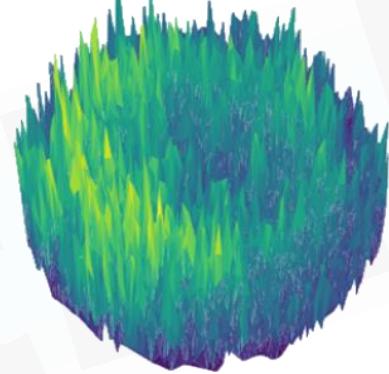
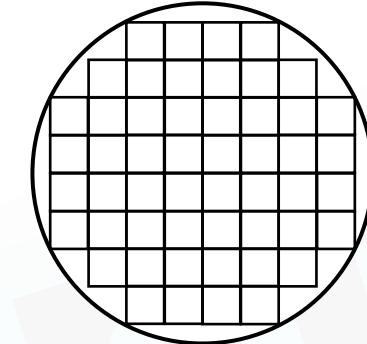
Random sample distributions
can match the parent sets

Wafer	X	Y	Feature1	Feature2	Feature3	...

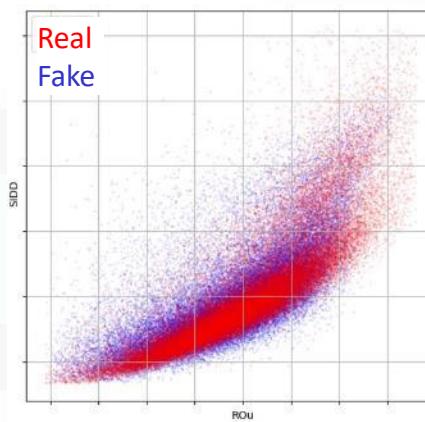
random sample generation
from a real dataset



Construct dataset by wafer coordinate



wafers
yield all features for each randomization



Feature 1

Feature 2

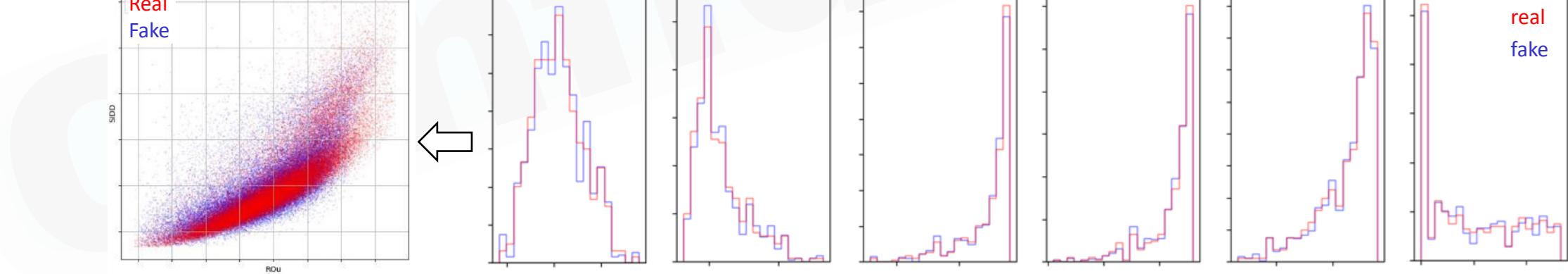
Feature 3

Feature 4

Feature 5

Feature 6

real
fake



Dataset Conversion

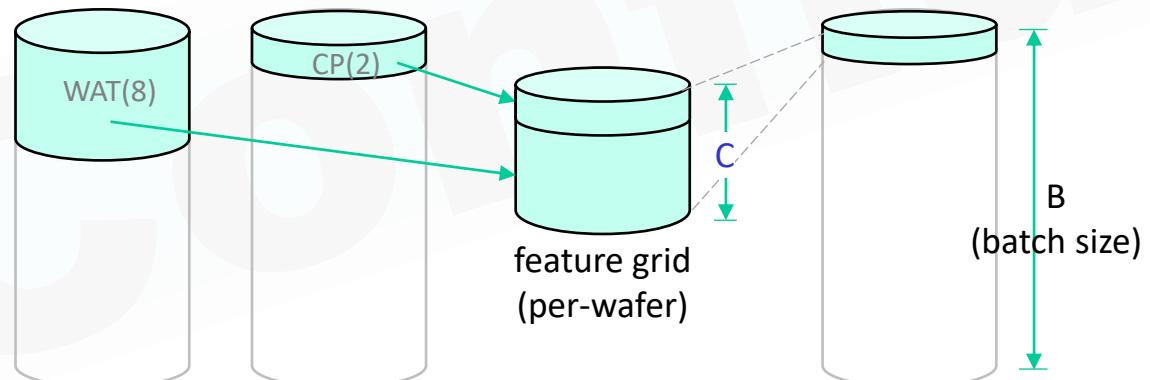
~10M samples

Test Features CP(2) + WAT(8)

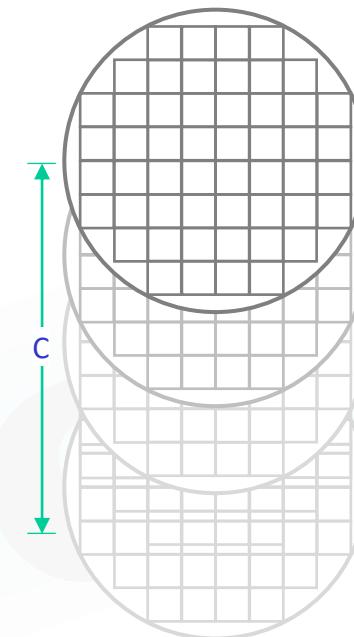
LWID	X	Y	CP-01	CP-02	WAT-01	WAT-02	WAT-03	...
LOT01_01	2	24	5	1421	10	5	8	
LOT01_01	6	25	3	3016	57	63	57	
LOT01_01	9	14	4	2733	22	53	59	
LOT01_01	11	29	4	2999	59	63	64	
LOT01_01	13	36	4	3047	62	63	63	

LOT21_01	53	56	3	2641	49	24	20	
LOT21_01	56	23	4	3121	41	60	64	
LOT21_01	58	40	5	3114	41	58	63	
LOT21_01	61	30	4	2880	36	57	63	
LOT21_01	65	32	3	2681	63	64	30	

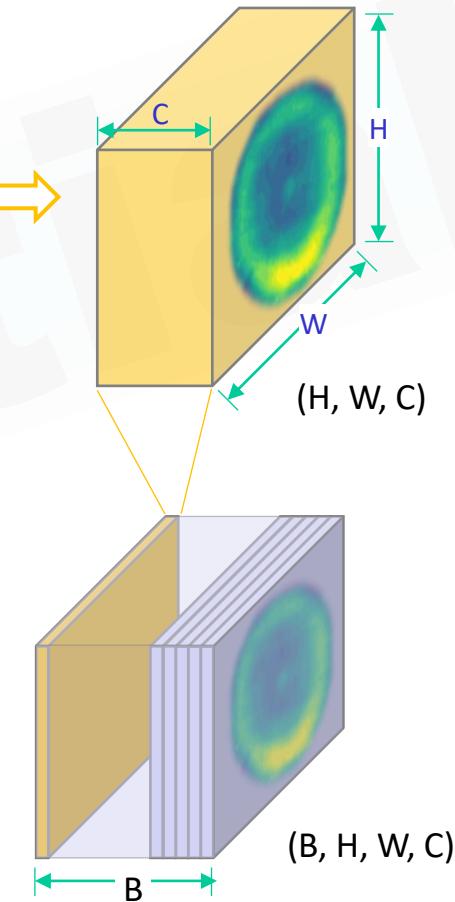
C (features)



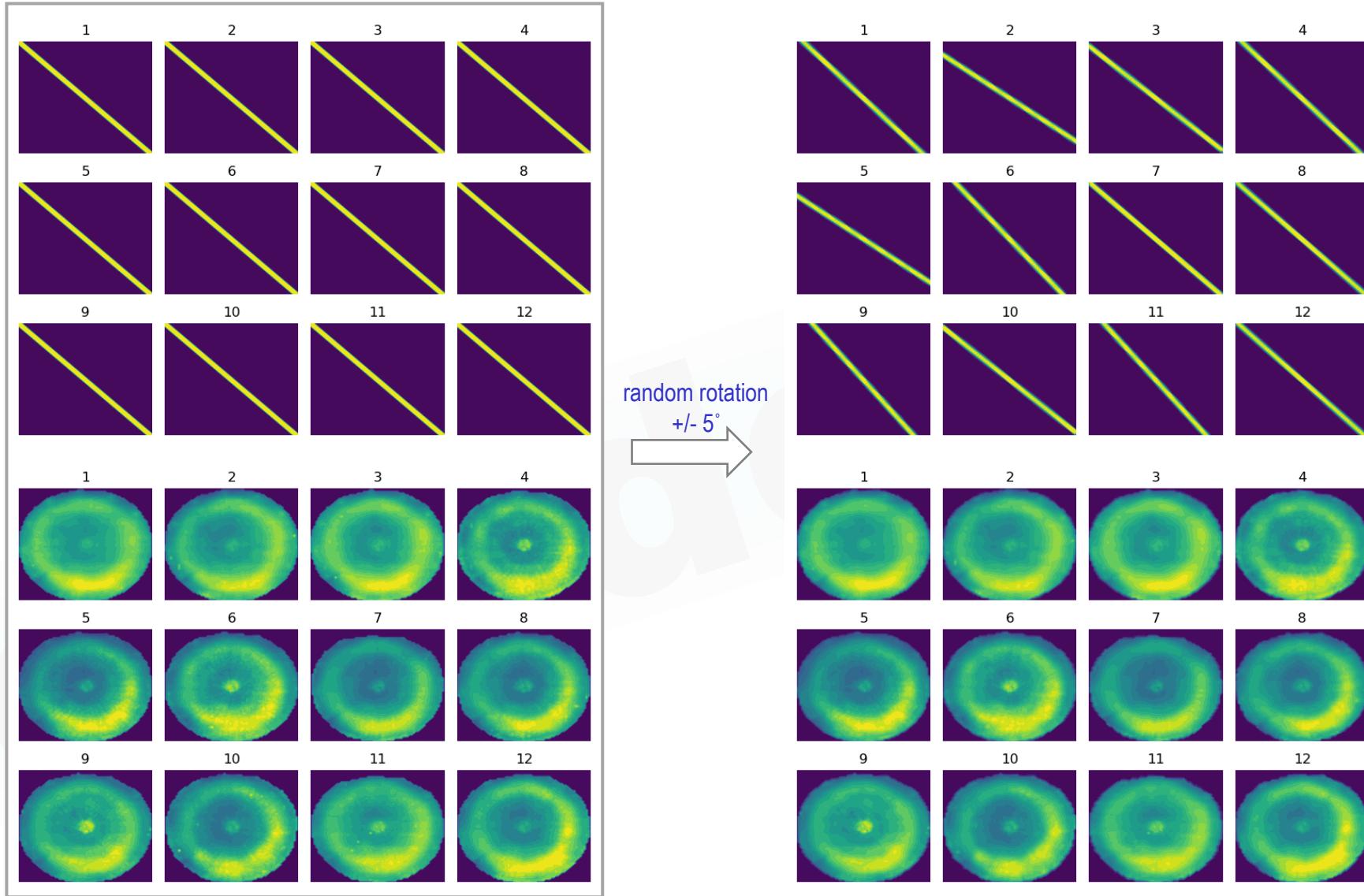
Feature grid (per wafer)



Dataset (per wafer)

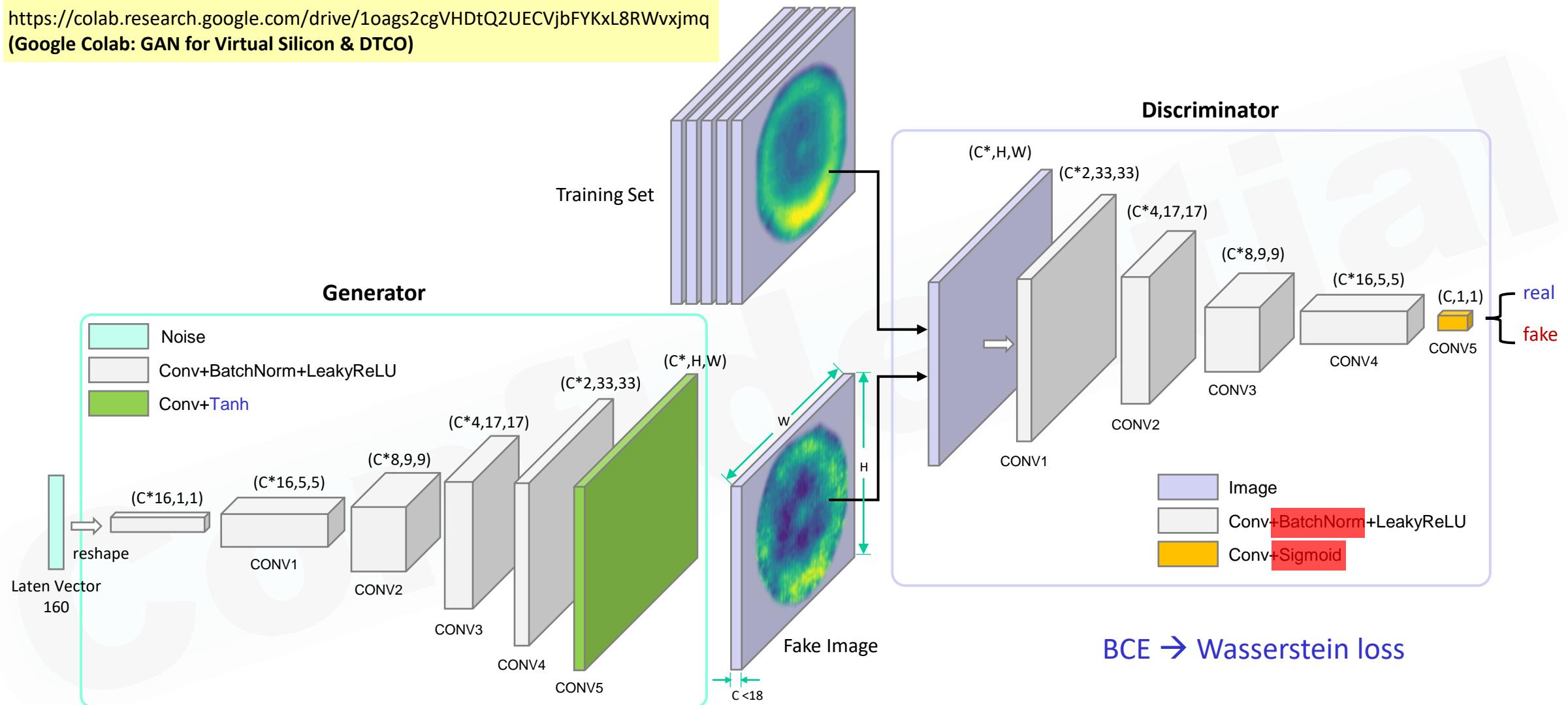


Data Augmentation

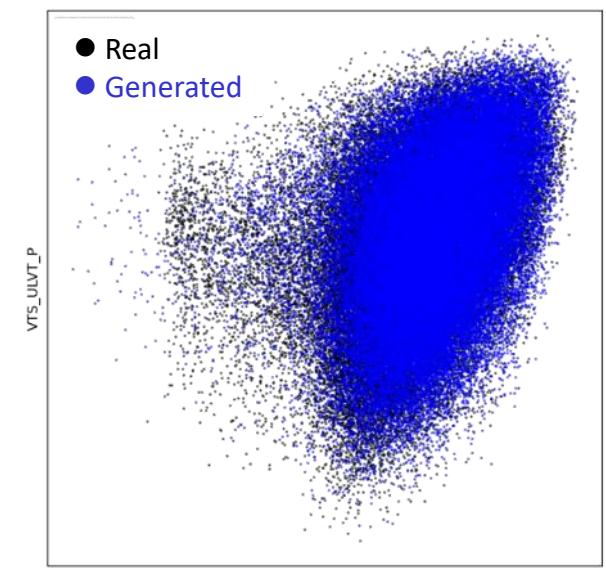
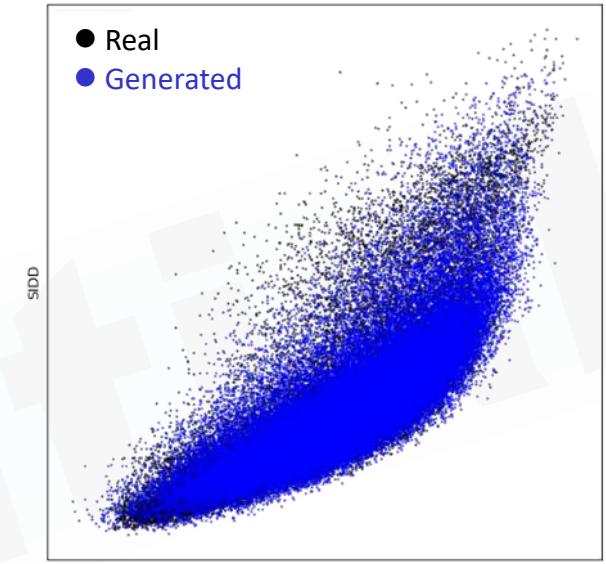
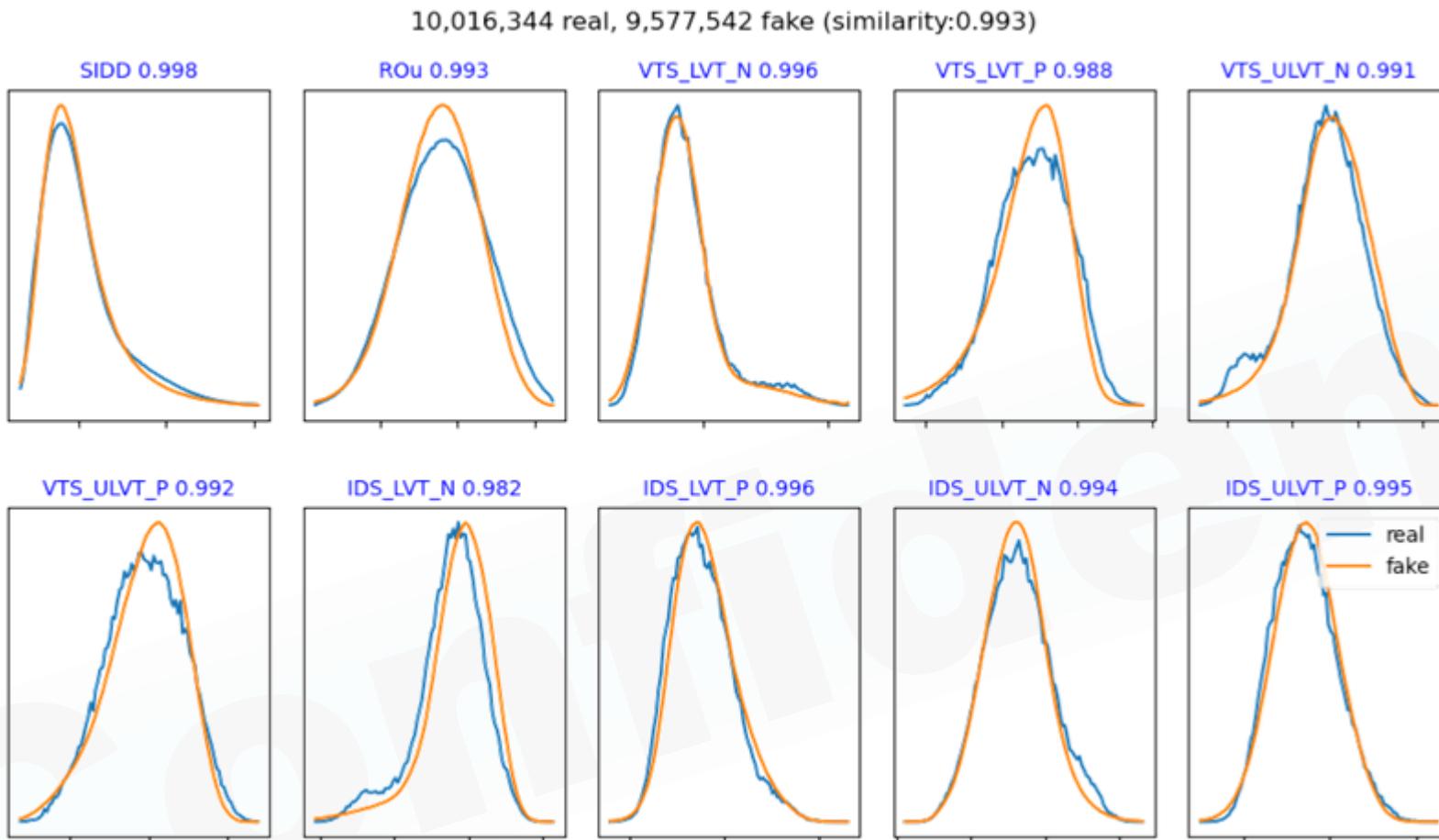


Simple GAN Modeling

<https://colab.research.google.com/drive/1oags2cgVHDtQ2UECVjbFYKxL8RWvxjmq>
(Google Colab: GAN for Virtual Silicon & DTCO)

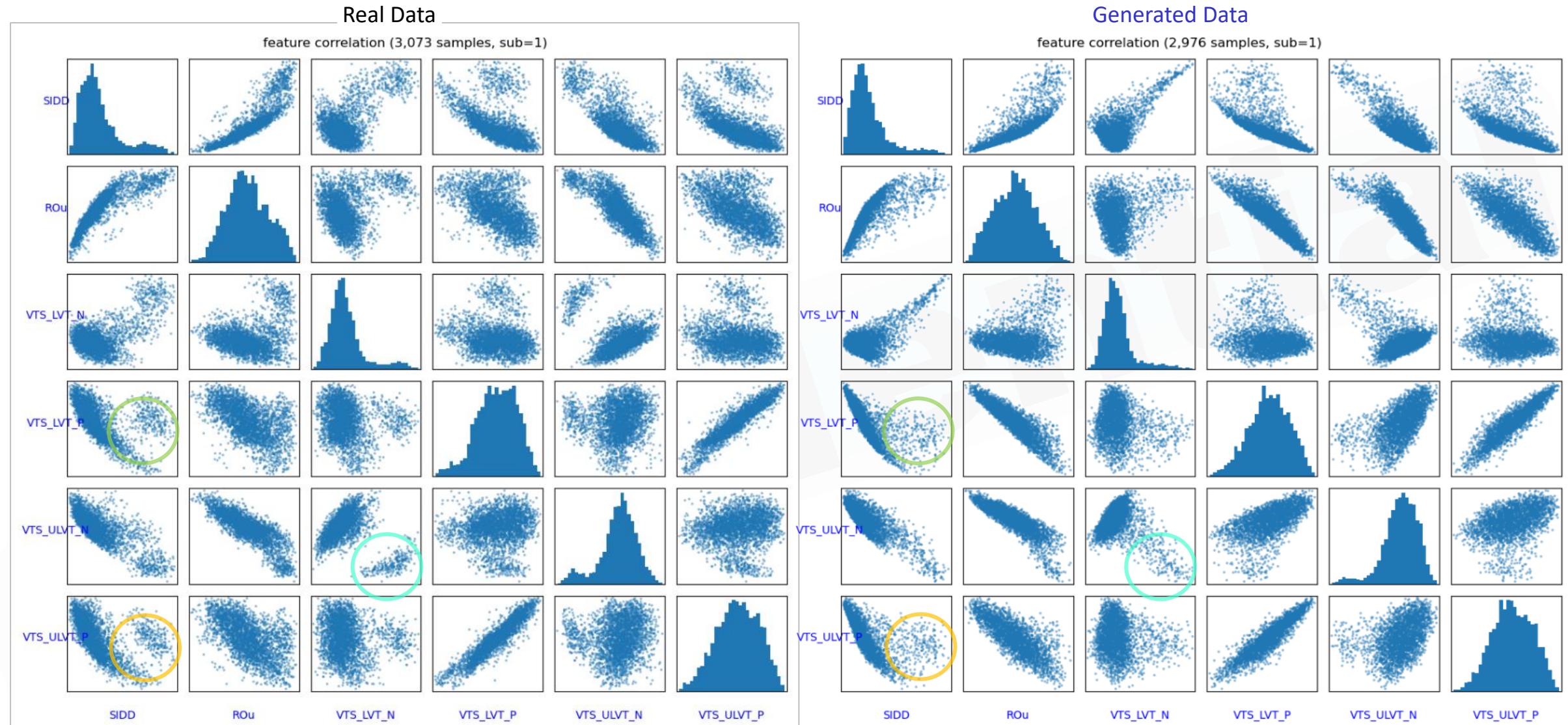


Feature Distribution Similarity



GAN: 1,000 epochs/~7hrs (NB)
WGAN: 1,000 epochs/~1.5hrs (NB)

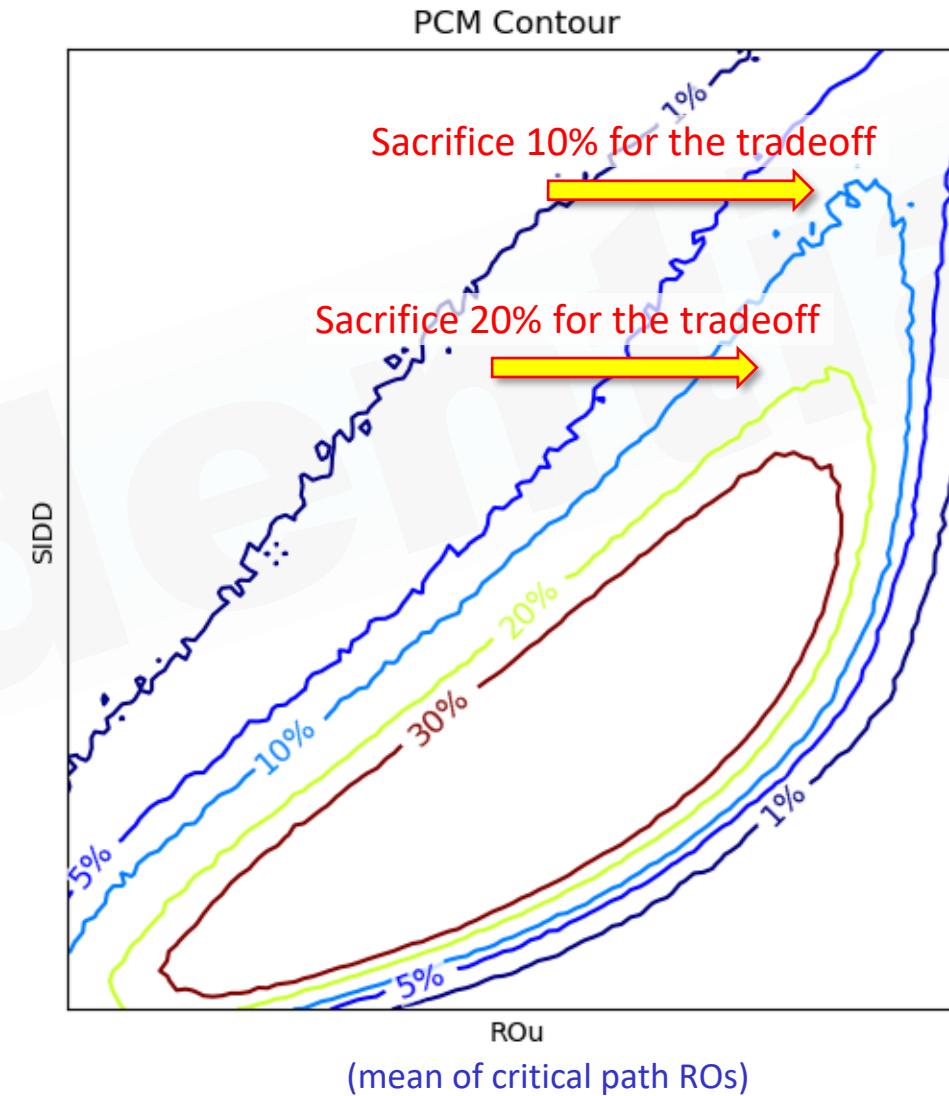
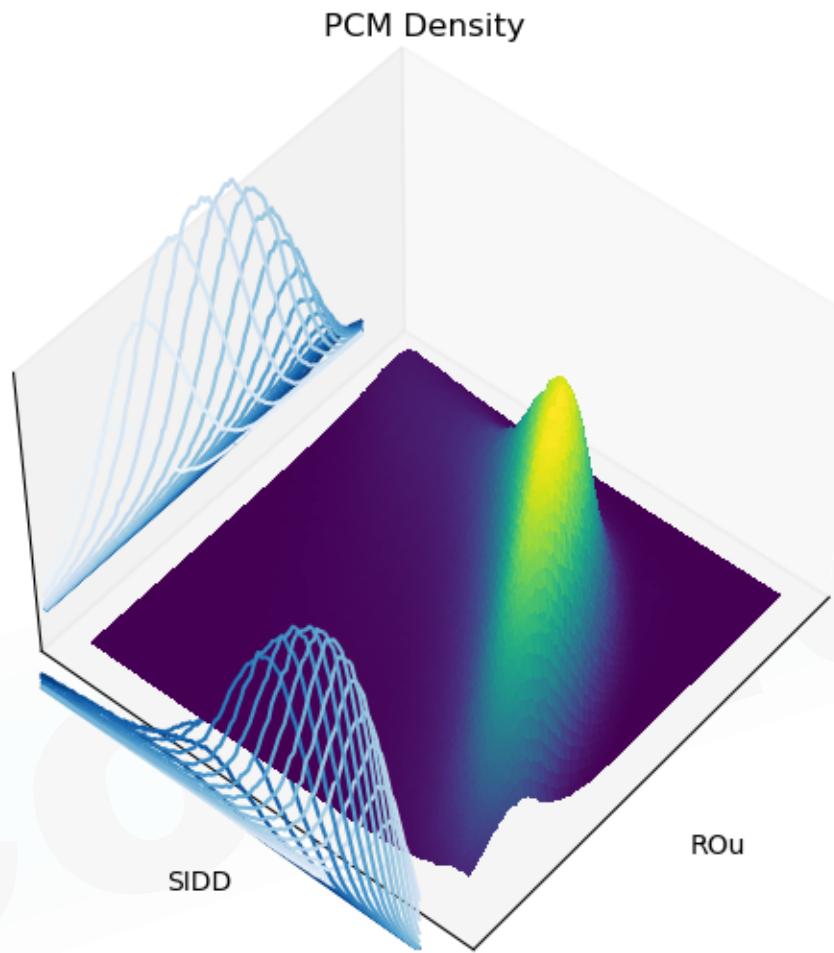
Feature Correlation



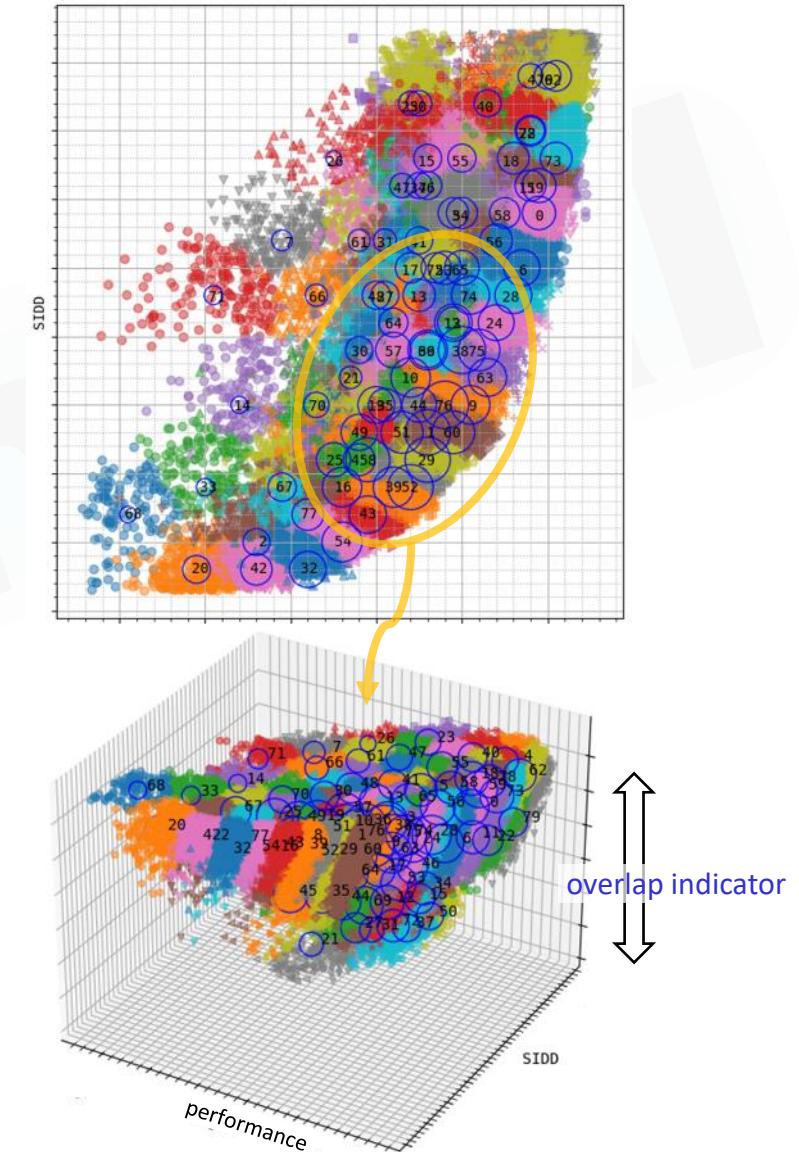
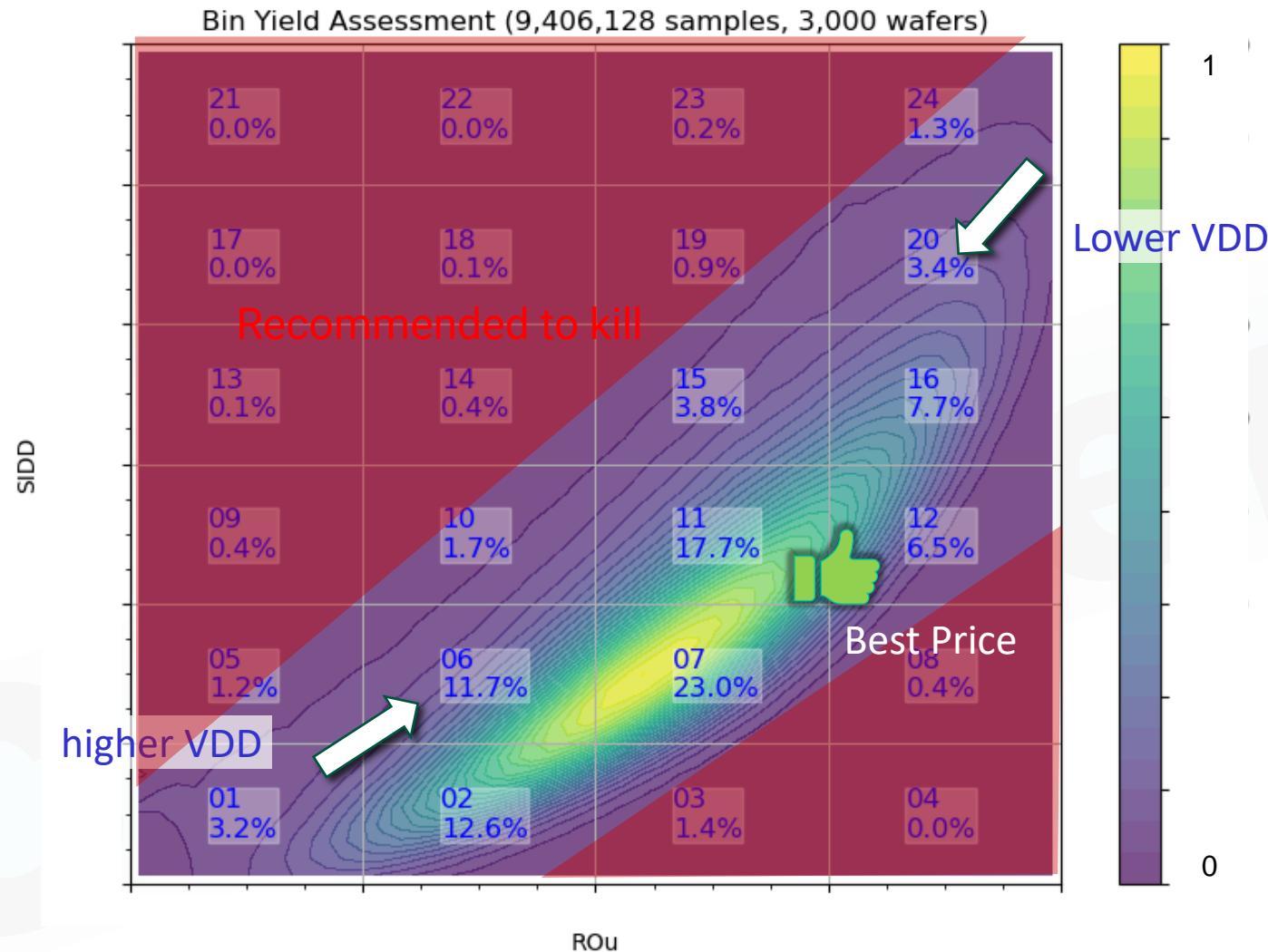
GAN seems to have learned the distribution of pilot wafers

Yield Assessment & Compromise

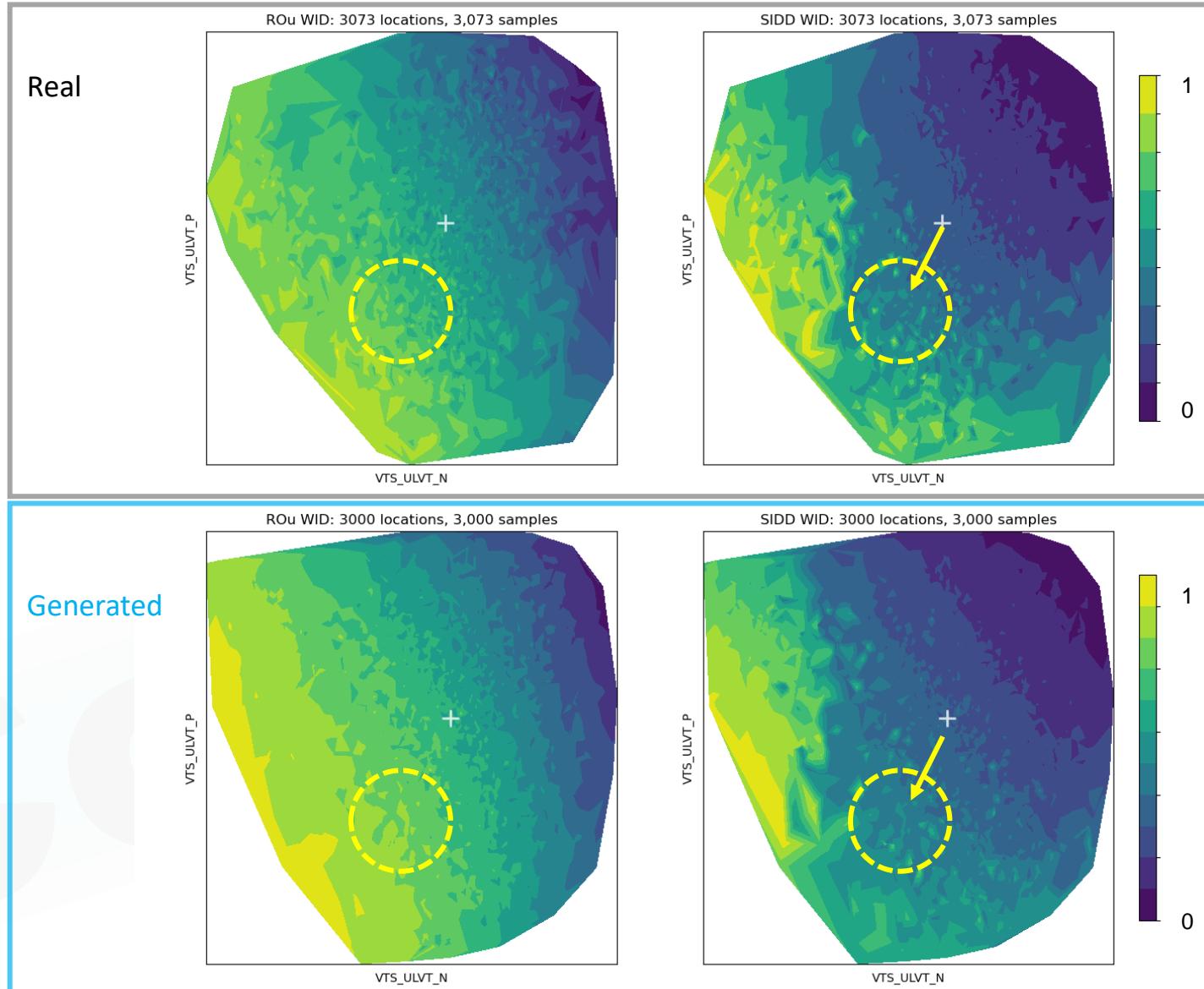
PCM 3D (2,976 wafers, 9,033,815 samples, sub:1)



Binning Assessment & Compensation

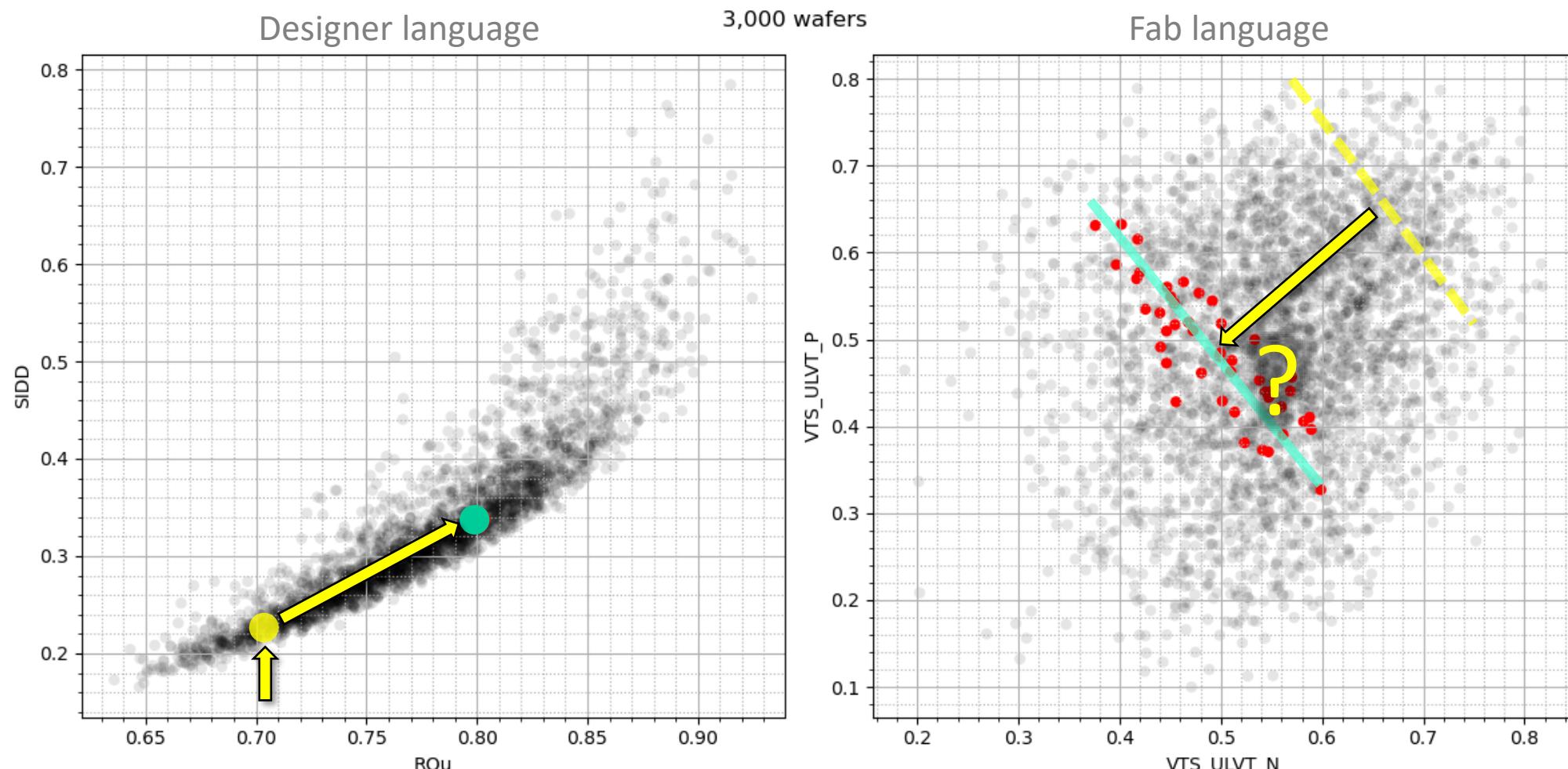


Process Recipe Optimization

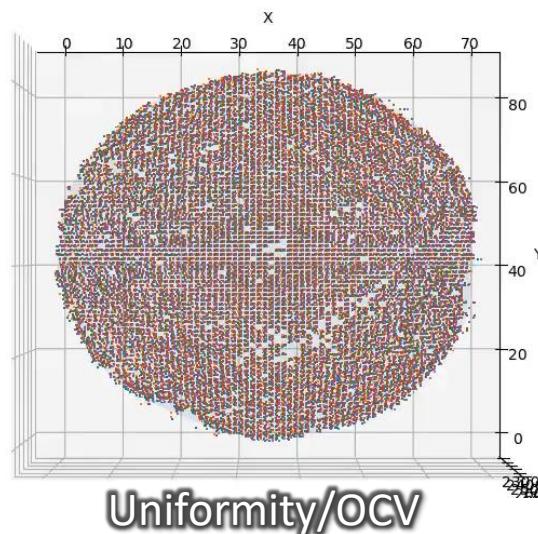


Guidance to maintain the same SIDD while improving the performance

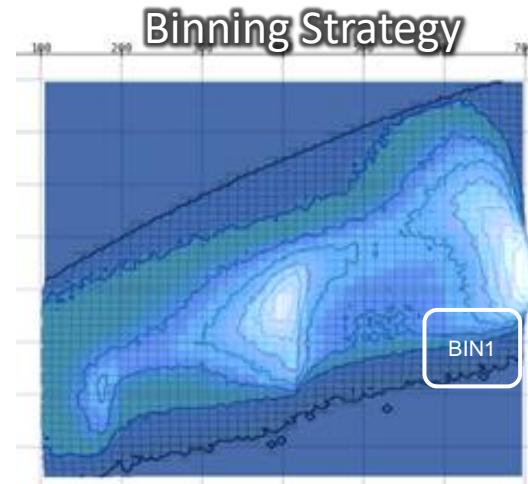
Process Tuning (Data Cross-probing)



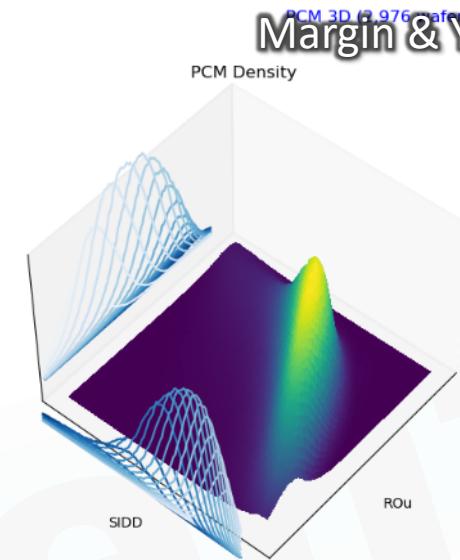
Empowering Innovation with Generated Model



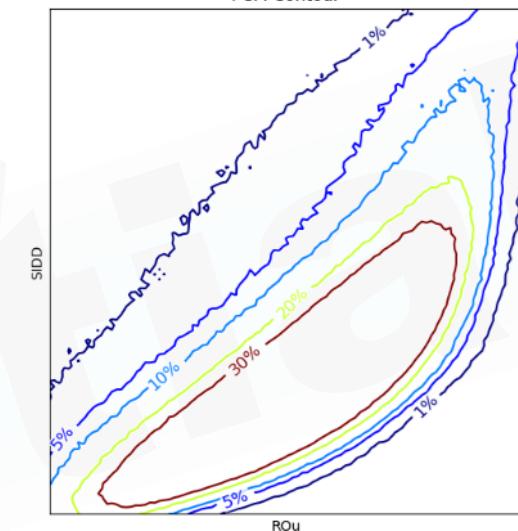
Uniformity/OCV



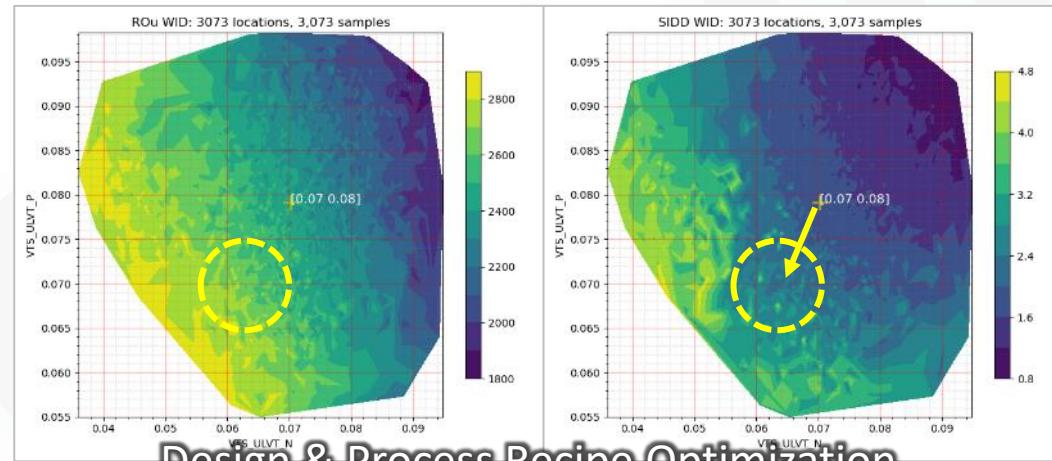
Binning Strategy



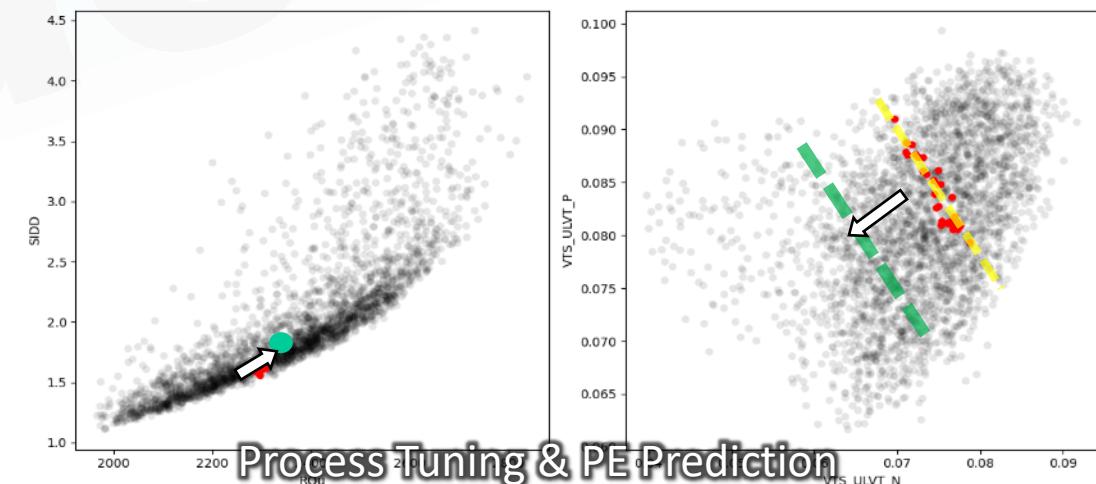
Margin & Yield Assessment



2,979 samples

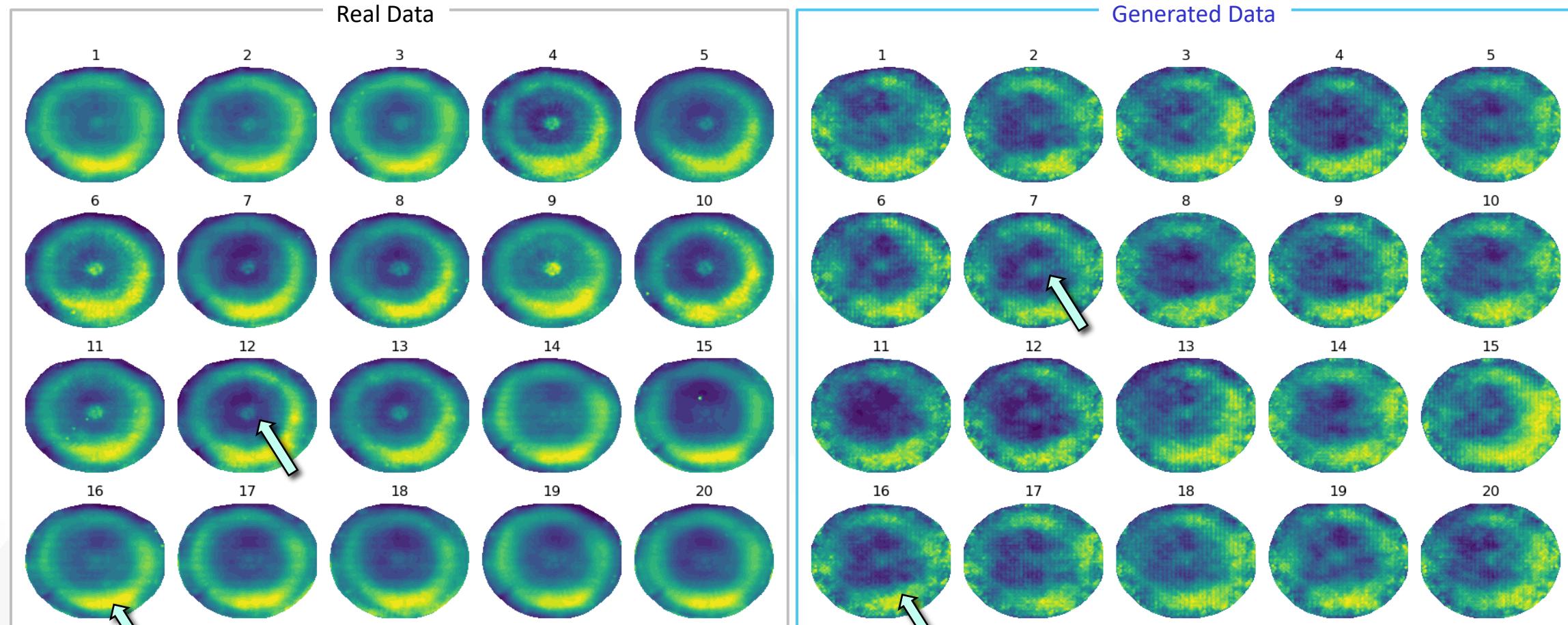


Design & Process Recipe Optimization



Process Tuning & PE Prediction

Smoothness Distortion



reproducibility
of
systematic defect

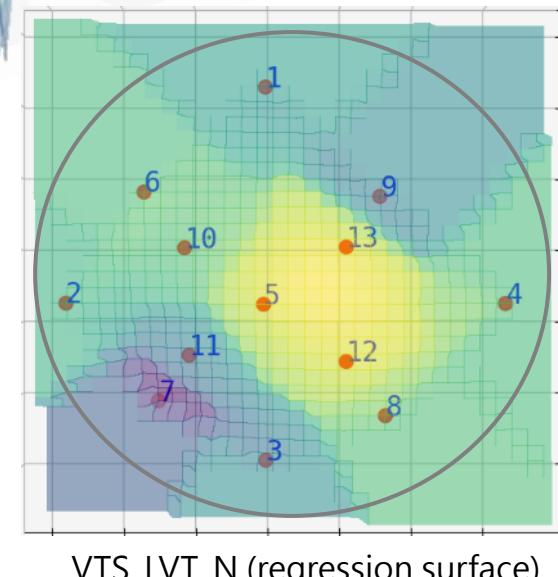
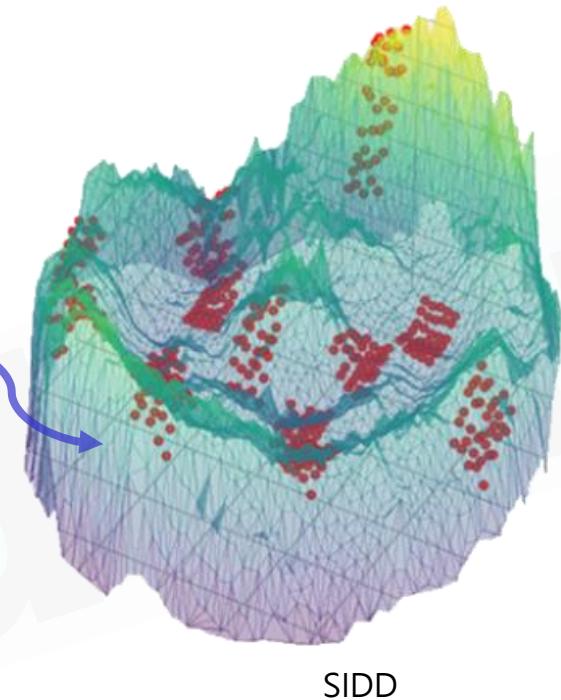
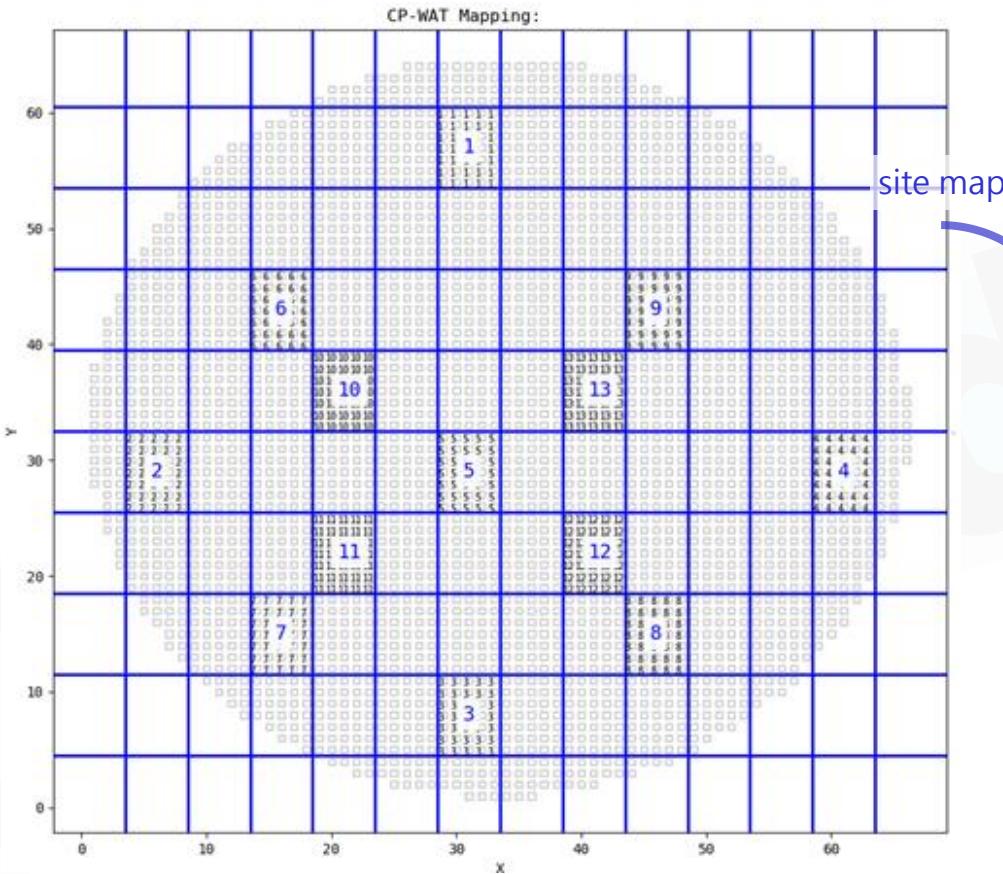


insufficient smoothness
of generated data



WAT Sampling Issue

- Insufficient data sampling
 - may lead to hasty generalization



Generated Model (Virtual Silicon)

■ Potential

- Data security, compression, and cross-domain delivery
- Application of design and process co-optimization strategies
- Development of emerging EDA tools

■ Room for improvement

- Feature dimension expansion
- Improvement in wafer-level feature smoothness
- Transformation between generative models