DAQ Trigger Top Module

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I. Overview

The overall structure of the “top” module is shown below in Fig. 1.

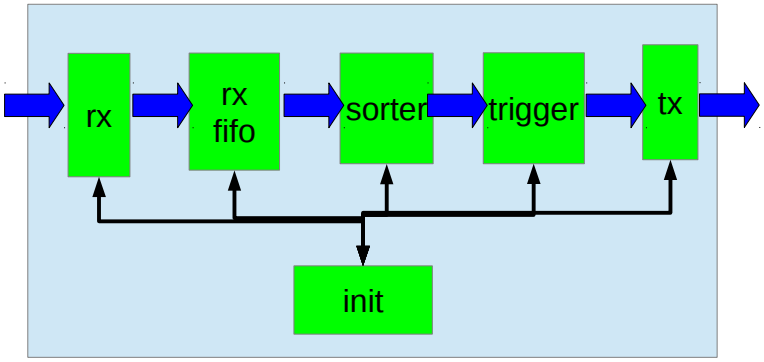

Figure 1: An overview of the design

The source files of the modules “rx” and “tx” are in the directory “Aurora/src”. These two modules are for the optical interface communication.

The source files of the module “rx_fifo” are in the directory “Xilinx_cores”.

The source files of the module “sorter” are in the directory “sorter/src”. This customizable sorter module is used to sort the data stream.

The source files of the module “trigger” are in the directory “trigger/src”. This module implements the trigger algorithm. Notice that only the “2ns” binned algorithm is implemented.

The source file of the module “init” is in the directory “Top/src”. This module is used to set the initial state of the whole design (e.g., after power up).

The directory “My_cores” includes the source files of some customizable library modules, e.g, a pipelined implementation of sorter and a synthesizable implementation of LUT.

The “trigger”, “sorter”, and “Aurora” directories include the source files, verification files and synthesis scripts for the trigger, sorter and Aurora modules.

The “sorter” and “trigger” modules are customizable and have several parameters.

II. Usage

1. To implement the design:

a. This design is developed on Linux. So, “/” rather “\” is used in directory hierarchy.

b. It is necessary that the “GMAKE” utility has been installed on your machine.

c. Make sure that the Xilinx ISE tools have been correctly installed and the binaries can be directly accessed. It is required that the environmental variables, e.g., PATH, have been set correctly.

d. Go to the directory “Top/syn/”, and then type “make physical_design”.

e. Wait for the process to finish. Check the file “top_route.twr” for timing report. The file “top_route.ncd” can be used to generate the “bit” file.

f. Typing “make clean” will remove all the generated files.

2. To simulate the design:

a. This design is developed on Linux, i.e., “/” rather “\” is used for directory hierarchy.

b. It is necessary that the “GMAKE” utility has been installed on your machine.

c. Make sure that the Xilinx ISE tools have been correctly installed and the binaries can be directly accessed. It is required that the environmental variables, e.g., PATH, have been set correctly.

d. Make sure that “perl” has been installed your machine.

e. Go to the directory “Top/sim”. Type “make OS_TYPE=*your_os_type* BASH_PATH=*your_bash_path* PERL_PATH=*your_perl_path* func_sim”. The “OS_TYPE” variable is used to find the Xilinx simulation libraries. For example, on my 64-bit machine, the OS_TYPE is “lin64”. For other supported OS type names, please refer to the Xilinx Simulation document.

f. Wait for the process to finish. To save time, only 20 patterns are used for simulation. Actually, if all the 5001 patterns are simulated, you may have to wait two days for the simulation to finish.

g. Typing “make clean” will remove all the generated files.