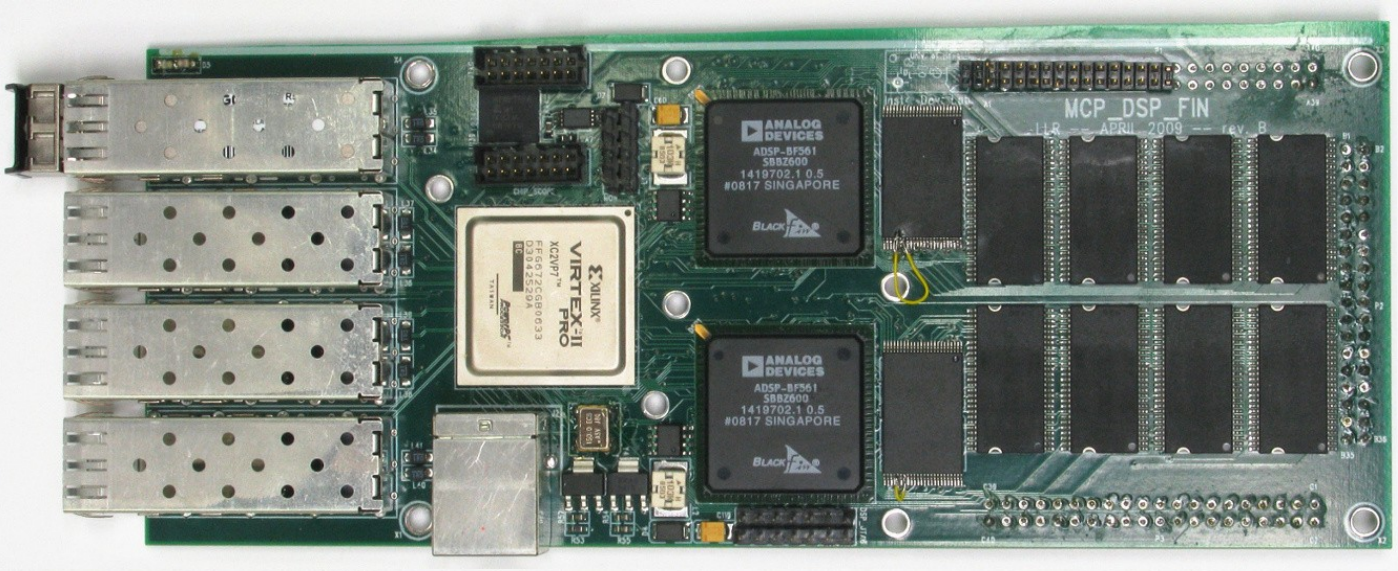
Data reduction in real-time with digital signal processing & DSP_FIN

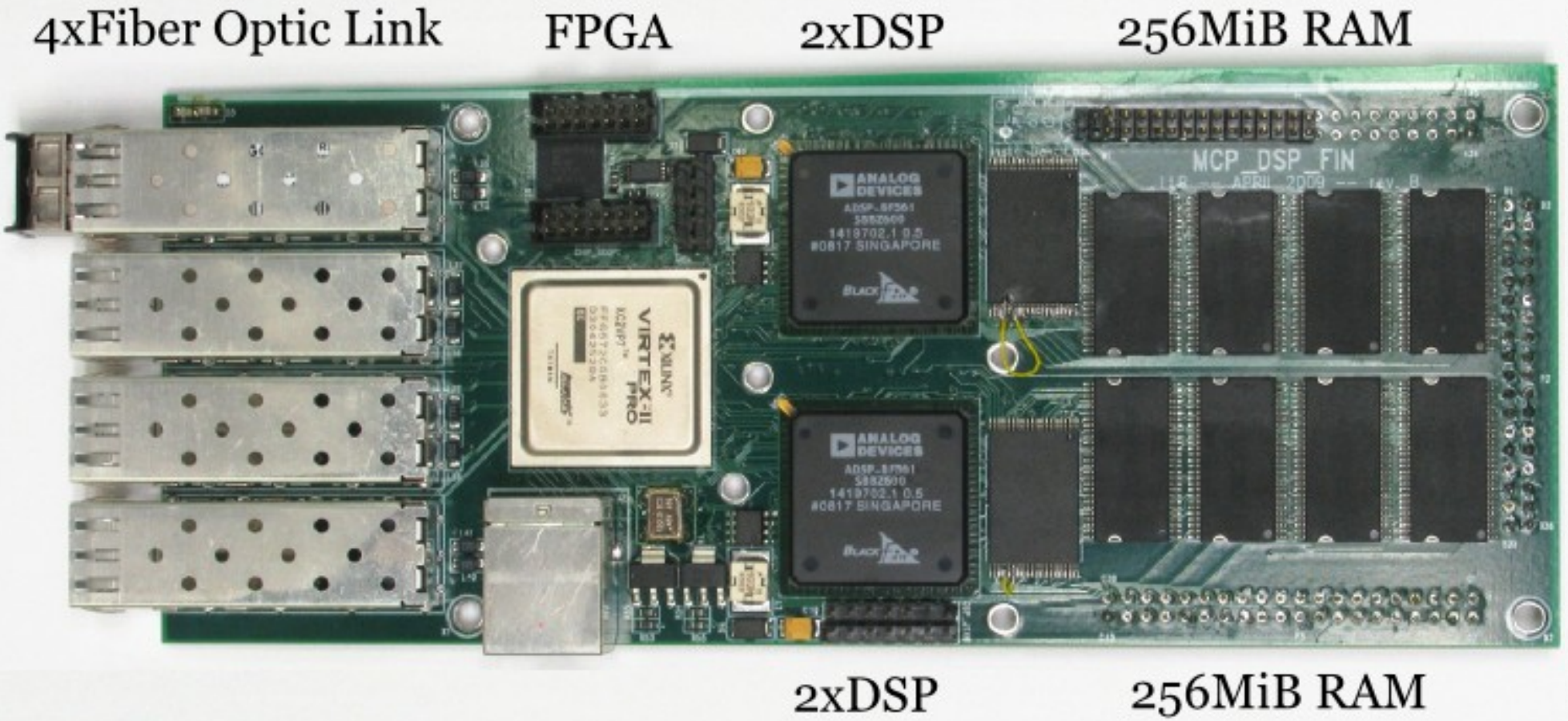
Local Collaborators:

Juaquin Anderson
Matt Andrew
Tom Browder
Michael Cooney
Xin Gao
James Kennedy
Luca Macchiarulo
Kurtis Nishimura
Louis Ridley
Jamal Rorie
Larry Ruckman
Gary Varner

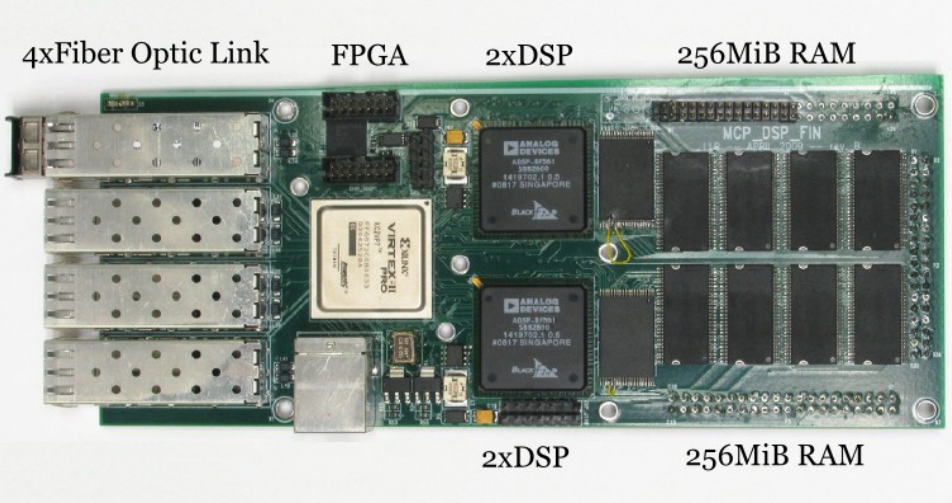


- 2010-01-25

DSP_FIN


4xFiber Optic Link
FPGA
2xDSP
256MiB RAM
MCP_DSP_FIN
ANALOG DEVICES
ADSP-BF561
1419702.1 0.5
#0817 SINGAPORE
XILINX
VIRTEX-II PRO
2xDSP
256MiB RAM

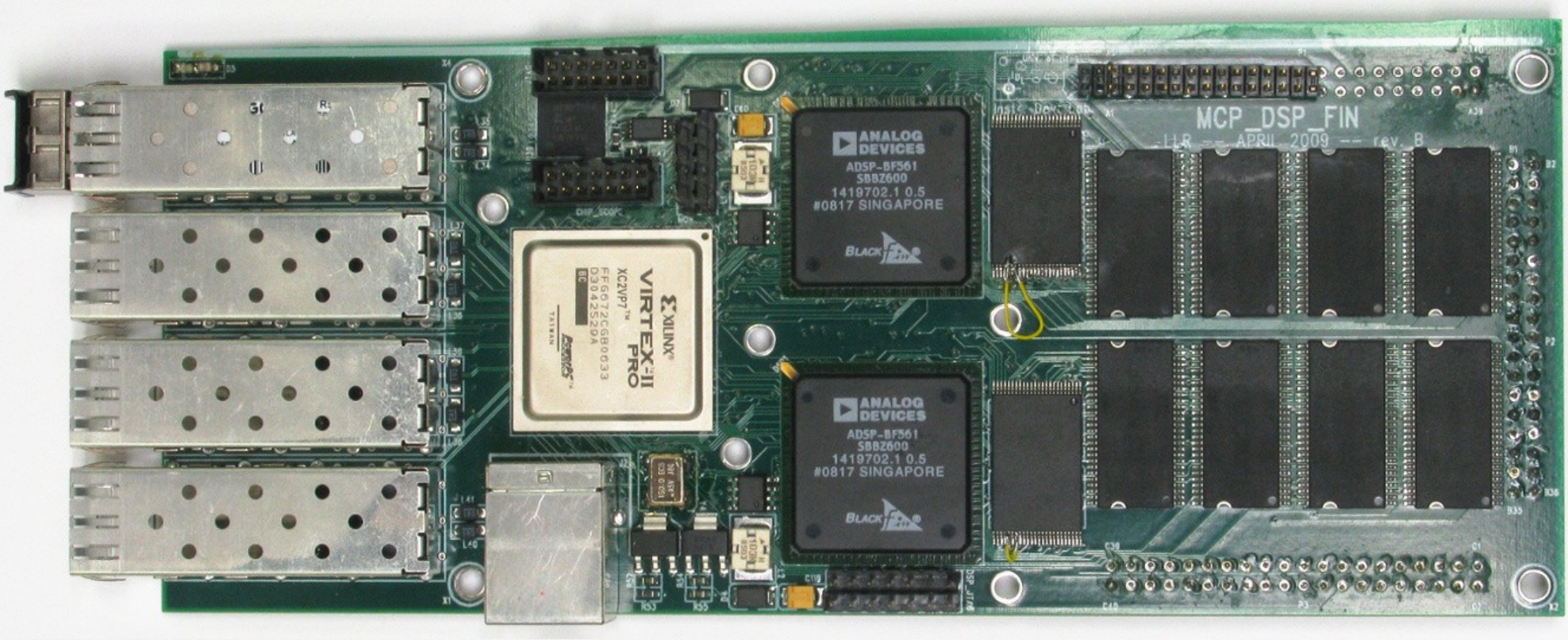
DSP_FIN



- DSP
  - Analog Devices Blackfin 561
    - dual-core
    - fixed-point
    - 600MHz (limited to 533MHz)
    - superscalar (when 16 bit)
    - assembly-language syntax very c-like
    - compiler accepts standard c/c++ code
- FPGA
  - Xilinx virtex 2 (revB) / virtex 4 (revC) / others
- DSP_FIN is useful for many different applications

DSP_FIN: particle ID

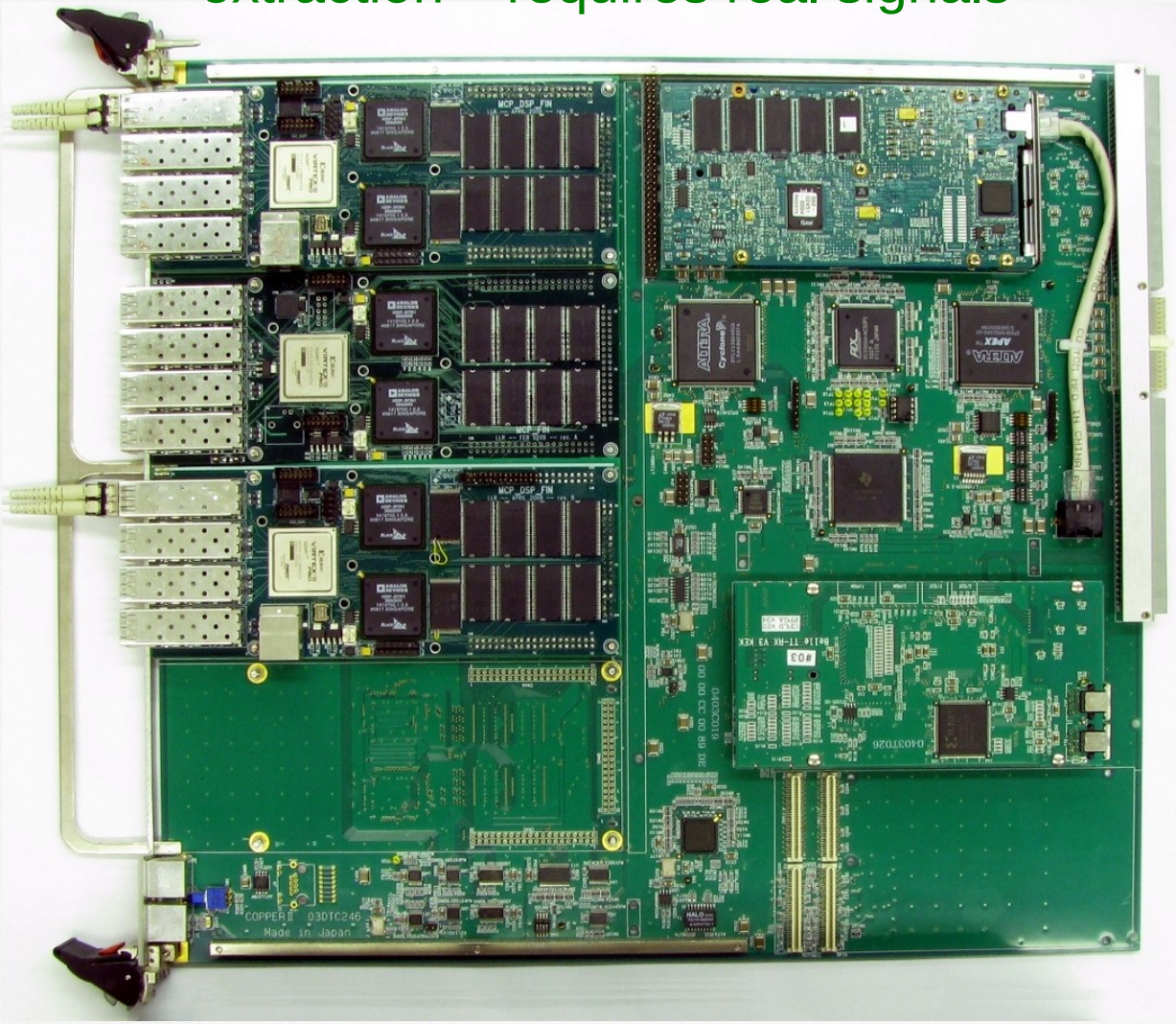
- each DSP core can process 60k waveforms/sec (measured)
- 30kHz L1 trigger rate and 2% occupancy:
  - each fiber brings in data from 64 PMT channels
  - each DSP FIN board can handle 256 PMT channels



DSP_FIN / COPPER: particle ID

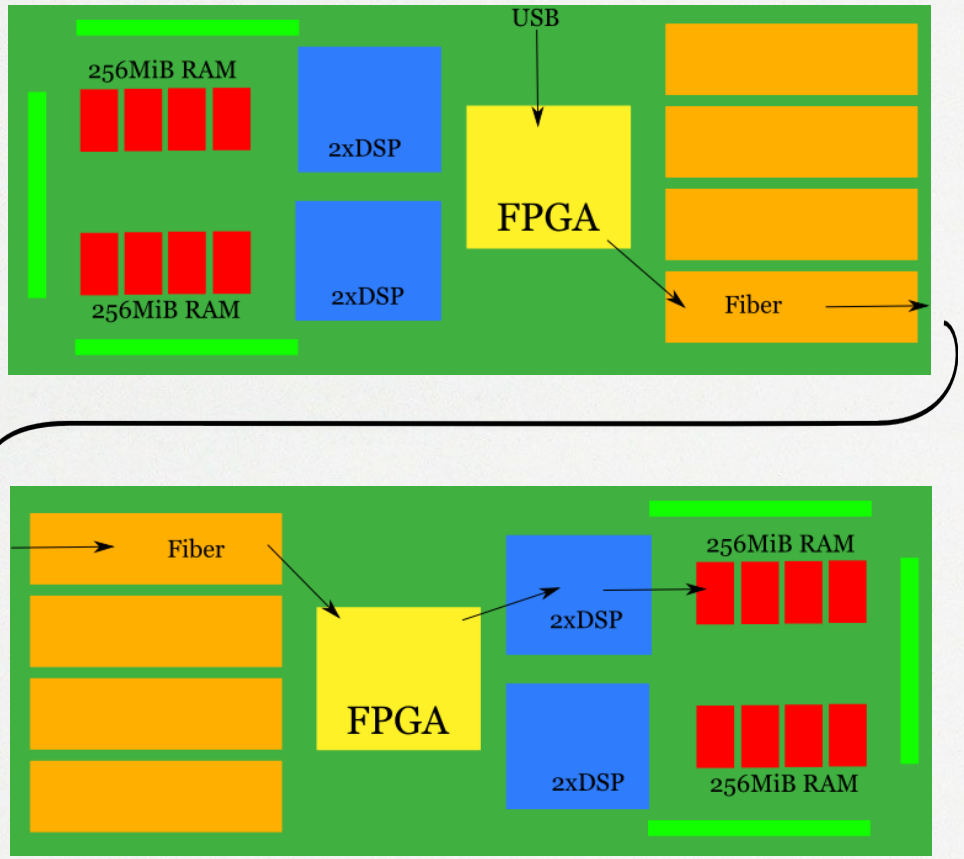
- each COPPER module can handle 1024 PMT channels (with 4 DSP_FIN boards per COPPER)
- need just 8 COPPER modules (with 32 DSP_FINs) to do all SL10 xTOP waveform processing in real time (8192 PMT channels)

Continuing studies of optimal signal extraction – requires real signals

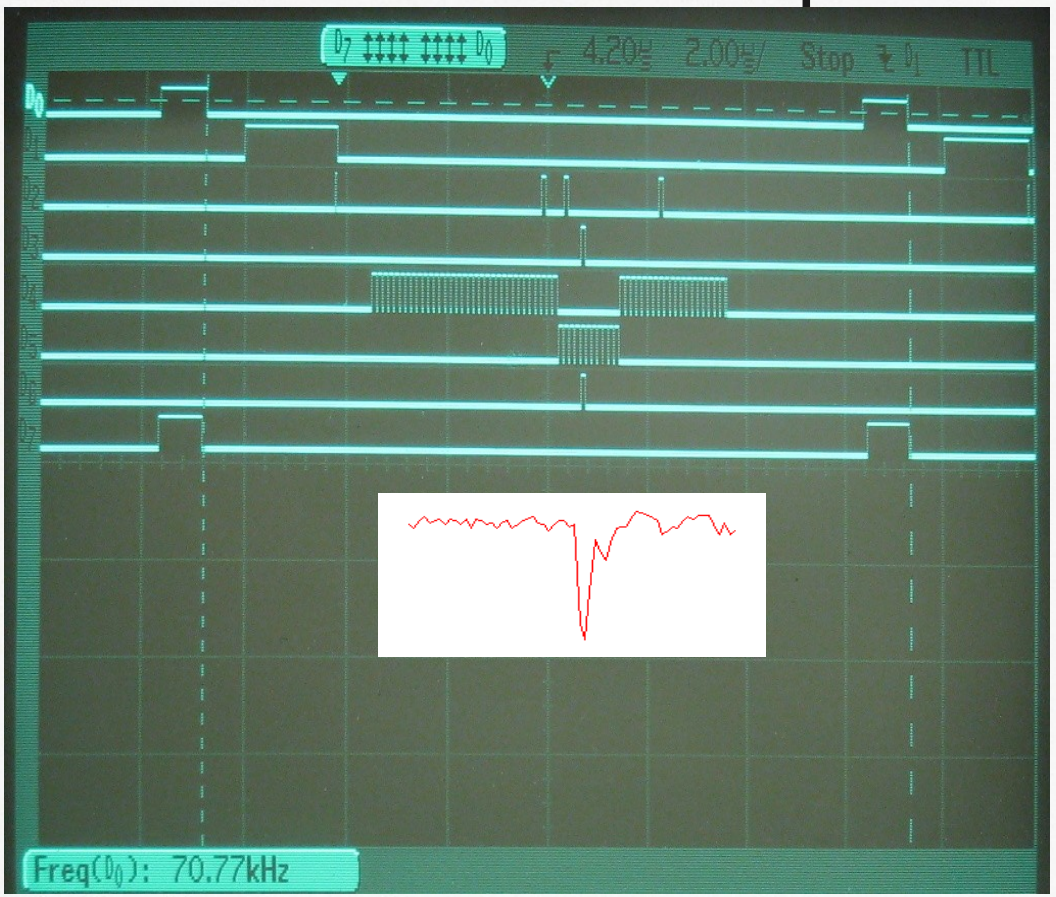


•DSP_FIN_revB “demo”

- USB → FPGA → fiber



- Fiber → FPGA → DSP → oscilloscope



•DSP_FIN_revC demo

- wxWidgets GUI → USB → FPGA → fiber
- fiber → FPGA → USB → wxWidgets GUI