Introduction

The LogiCORE™ IP GTP Transceiver Wizard automates the task of creating HDL wrappers to configure the high-speed serial GTP transceivers in the Spartan®-6 LXT FPGAs.

The menu-driven interface allows one or more GTP transceivers to be configured using pre-defined templates for popular industry standards, or from scratch, to support a wide variety of custom protocols. The Wizard produces a wrapper, an example design, and a testbench for rapid integration and verification of the serial interface with your custom function.

Features

- Creates customized HDL wrappers to configure Spartan-6 family GTP transceivers
- Users can configure Spartan-6 family GTP transceivers to conform to industry standard protocols using predefined templates, or tailor the templates for custom protocols
- Templates include support for the following specifications: CPRI™, DisplayPort, Gigabit Ethernet, HD-SDI, OBSAI, PCI EXPRESS® (PCIe®) generation I, Serial RapidIO, XAUI, Aurora 8B/10B, SATA 1.5 Gb/s, and SATA 3 Gb/s
- Automatically configures analog settings
- Each custom wrapper includes example design, testbench; and both implementation and simulation scripts
- Included at no additional charge with ISE® Design Suite software. Access the GUI for this Wizard from the ISE CORE Generator™ software

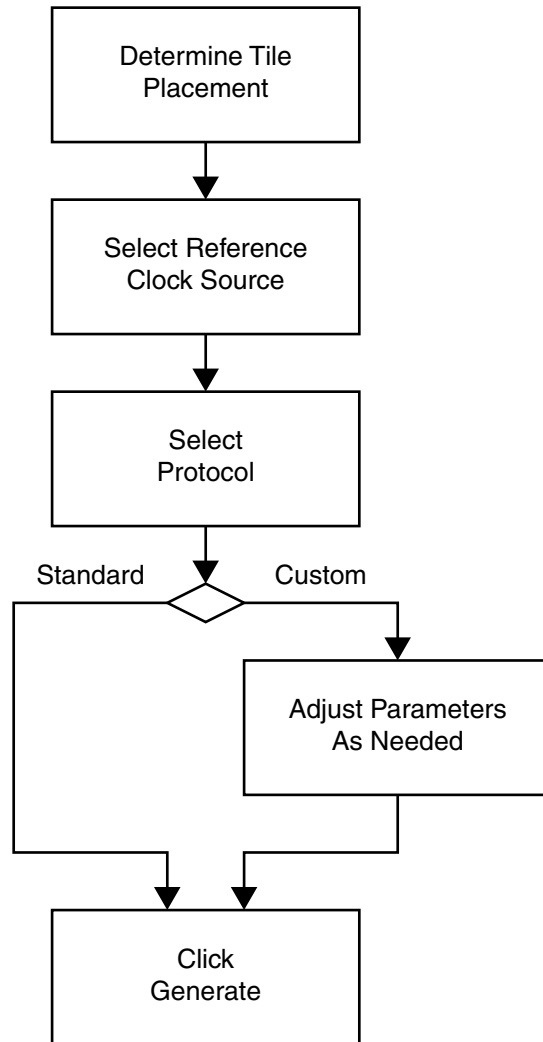| LogiCORE IP Facts Table					
Wizard Specifics					
Supported Device Family[1]	Spartan-6 LXT FPGAs [2]				
Supported User Interfaces	Not Applicable				
	Resources				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Config1	Not Applicable				
Provided with Wizard					
Documentation	Product Specification Getting Started Guide				
Design Files	Verilog and VHDL				
Example Design	Verilog and VHDL				
Testbench	Verilog and VHDL				
Constraints File	Synthesis Constraints File				
Simulation Model	Verilog and VHDL				
Tested Design Tools					
Design Entry Tools	CORE Generator™ tool				
Simulation	ISim 13.1 Mentor Graphics ModelSim 6.6d Cadence IES[3] 10.2 Synopsys VCS and VCS MX 2010.06				
Synthesis Tools	XST 13.1 Synopsys Synplify Pro D-2010.03				
Support					
Provided by Xilinx, Inc.					

Notes:

1. For a complete listing of supported devices, see the release notes for this Wizard.
2. For more information on the Spartan-6 devices, see the *Spartan-6 Family Overview* [Ref 1]
3. Cadence Incisive Enterprise Simulator (IES)

Functional Overview

Figure 1 outlines the steps required to configure GTP transceivers using the Wizard. Start the CORE Generator™ software and select the GTP Transceiver Wizard, then follow the chart to configure the transceivers and generate a wrapper that includes an accompanying example design.

- If you use an existing template with no changes, click Generate.
- If you are modifying a standard template or starting from scratch, proceed through the Wizard and adjust the settings as needed.

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Figure 1: **GTP Wizard Configuration Step**

See the *Spartan-6 FPGA GTP Transceivers User Guide* [Ref 3] for details on the various transceiver features and parameters available.

Structure of the Example Design and Testbench

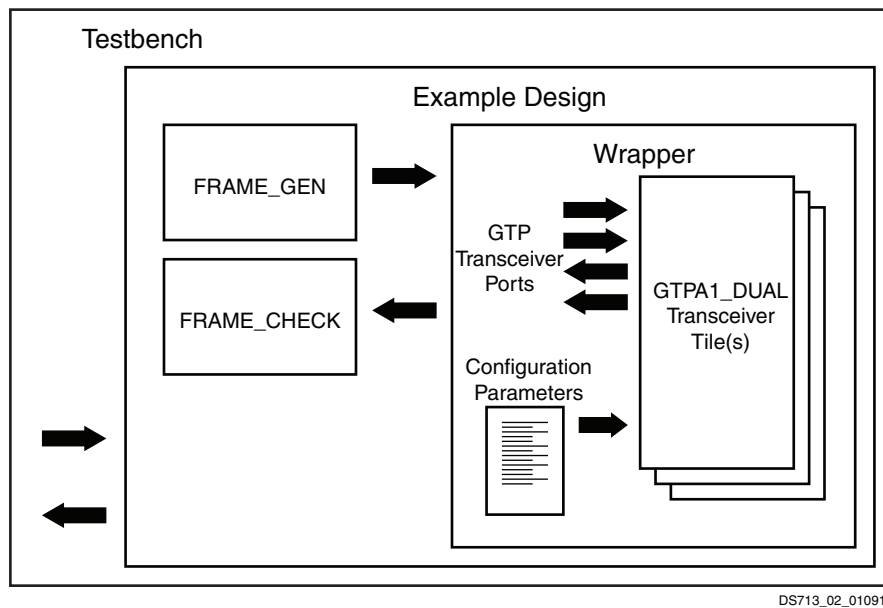Figure 2 illustrates the structure of the example design and testbench generated with the GTP wrapper.

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Figure 2: **Structure of the Example Design and Testbench**

The following files are provided to demonstrate how to simulate the configured transceiver:

1. GTP Wrapper, which includes:
    *   The specific gigabit transceiver configuration parameters set using the Wizard.
    *   GTPA1_DUAL Transceiver selected using the Wizard.
2. Example Design illustrating modules required to simulate the wrapper. The components are:
    *   FRAME_GEN Module: Generates a user-definable data stream for simulation analysis.
    *   FRAME_CHECK Module: Tests for correct transmission of data stream for simulation analysis.
3. Testbench: Top-level testbench demonstrating how to stimulate the design.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

The Spartan-6 FPGA GTP Transceiver Wizard is provided free of charge under the terms of the Xilinx End User License Agreement. The Wizard can be generated by the Xilinx® ISE CORE Generator software, which is a standard component of the Xilinx ISE Design Suite. This version of the Wizard can be generated using the ISE CORE Generator system v13.1. For more information, please visit the Architecture Wizards web page.

Information about additional Xilinx LogiCORE modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

References

1. DS160: *Spartan-6 Family Overview*
2. UG546: *LogiCORE IP Spartan-6 FPGA GTP Transceiver Wizard v1.9 Getting Started Guide* for a general overview of the wrapper creation procedure.
3. UG386: *Spartan-6 FPGA GTP Transceivers User Guide*

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
04/24/09	1.1	Initial Xilinx release.
06/24/09	1.2	Wizard v1.2 release.
09/16/09	1.3	Wizard v1.3 release.
12/02/09	1.4	Wizard v1.4 release.
04/19/10	1.5	Wizard v1.5 release. Added support for SATA 3 Gb/s. Added Ordering Information.
07/23/10	1.6	Wizard v1.6 release.
09/21/10	1.7	Wizard v1.7 release.
12/14/10	1.8	Wizard v1.8 release.
03/01/11	1.9	Wizard v1.9 release. Updated Wizard and tools versions. Added Wizard's availability and location in Features. Changed title of "Wrapper Overview" section to Structure of the Example Design and Testbench and replaced its text. Removed component numbers from and renamed Figure 2. Minor typographical corrections.

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