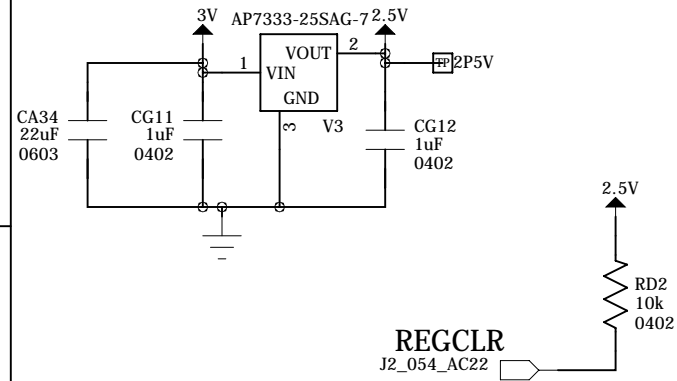


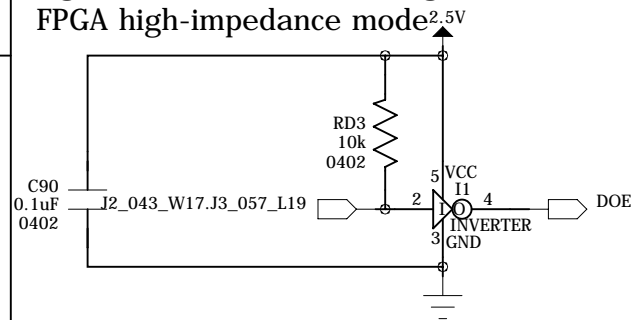
E

provides 2.5V for multiplexers, i2c eeprom,
i2c GPIOs and i2c temperature sensors



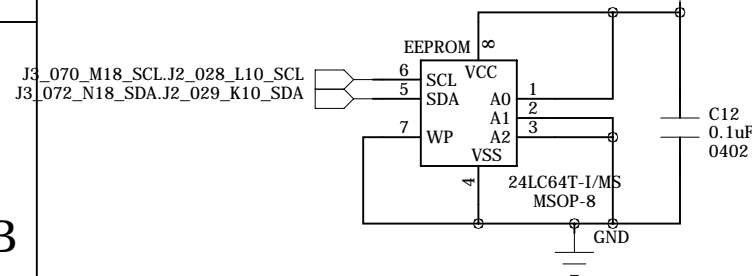
the pullup is so all the registers are cleared
(even when FPGA not present)

disables DOE by default
ensures all four DOE (active high)
signals are not driven during
FPGA high-impedance mode



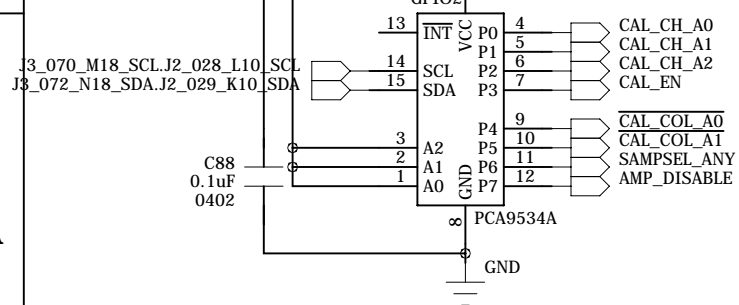
i2c eeprom for carrier identification

i2c address = 1010001

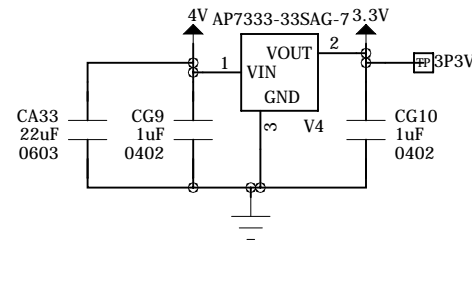


i2c GPIO to control calibration signal
amp_disable

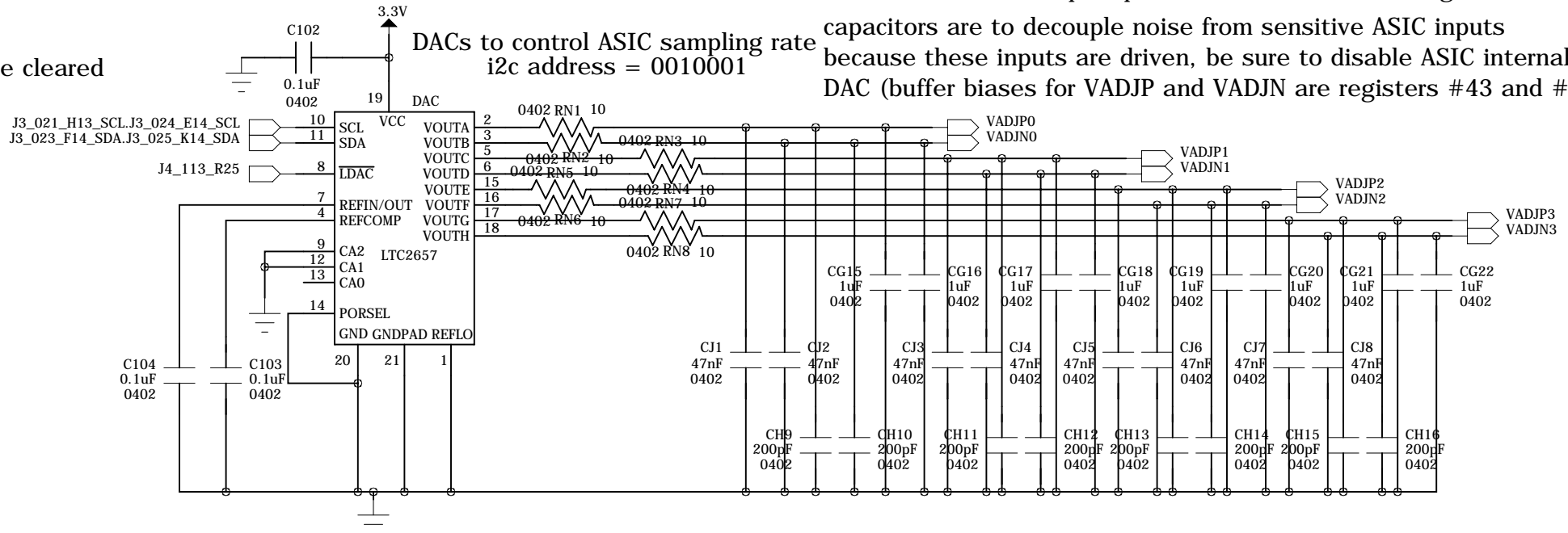
i2c address = 0111111



provides 3.3V for LTC2637 DACs

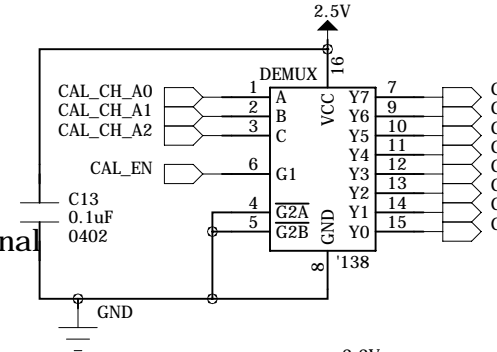


DACs to control ASIC sampling rate
i2c address = 0010001



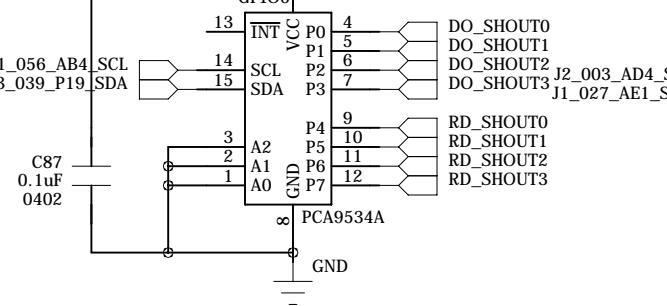
capacitors are to decouple noise from sensitive ASIC inputs
because these inputs are driven, be sure to disable ASIC internal
DAC (buffer biases for VADJP and VADJN are registers #43 and #45)

selects one channel out of 8 for calibration signal



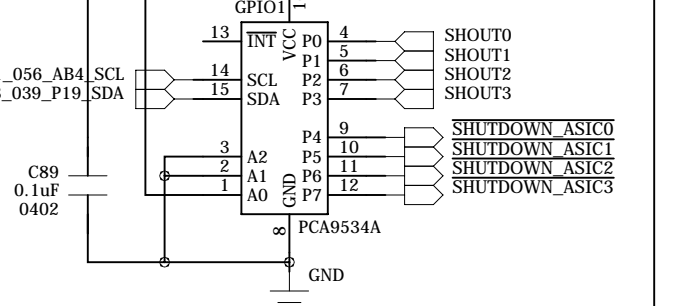
i2c GPIO to readback sample,
channel and window shift registers

i2c address = 0111000

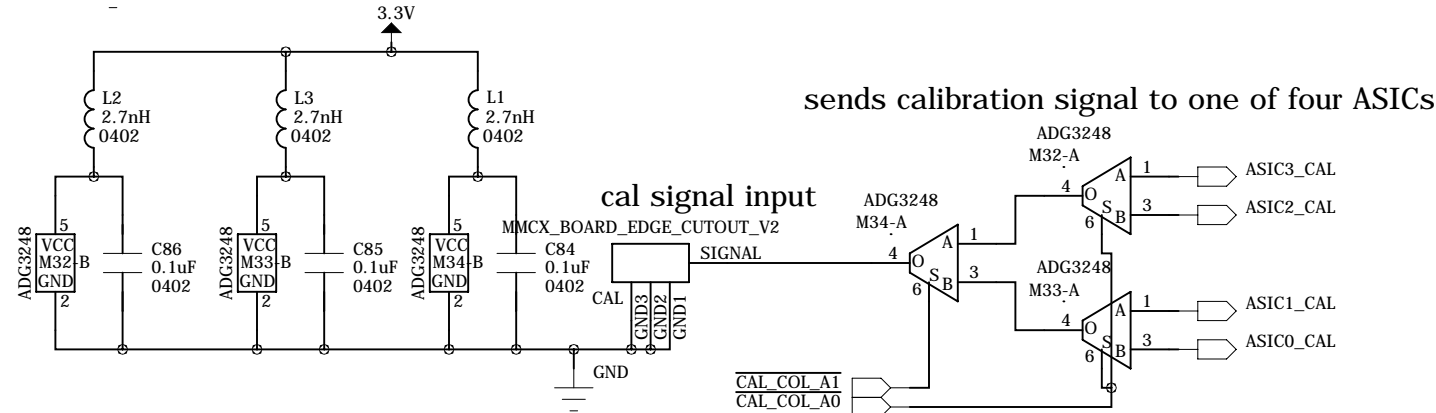


i2c GPIO to readback generic shift register

i2c address = 0111001



sends calibration signal to one of four ASICs



institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

title: carrier13
revision: D
IDLAB design #: IDL_13_047
circuit design: LJR, MZA, KAN, GSV, LM
PCB design: MZA, LJR

sheet #: 1 of 11
sheet description: POWER_CAL_I2C_FET_DAC_GPIO_EPROM
date last modified: 2013-12-31

D

C

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A

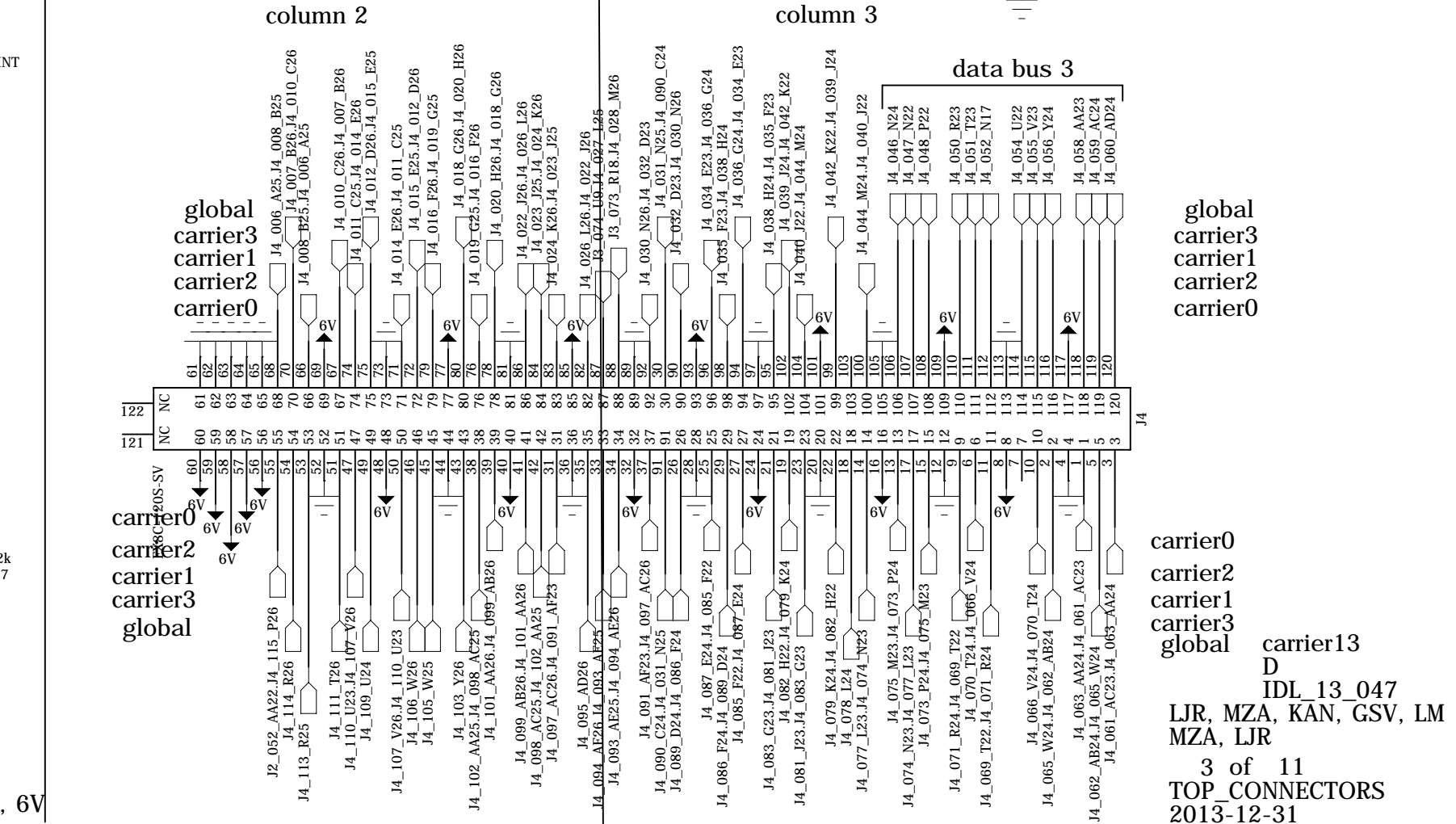
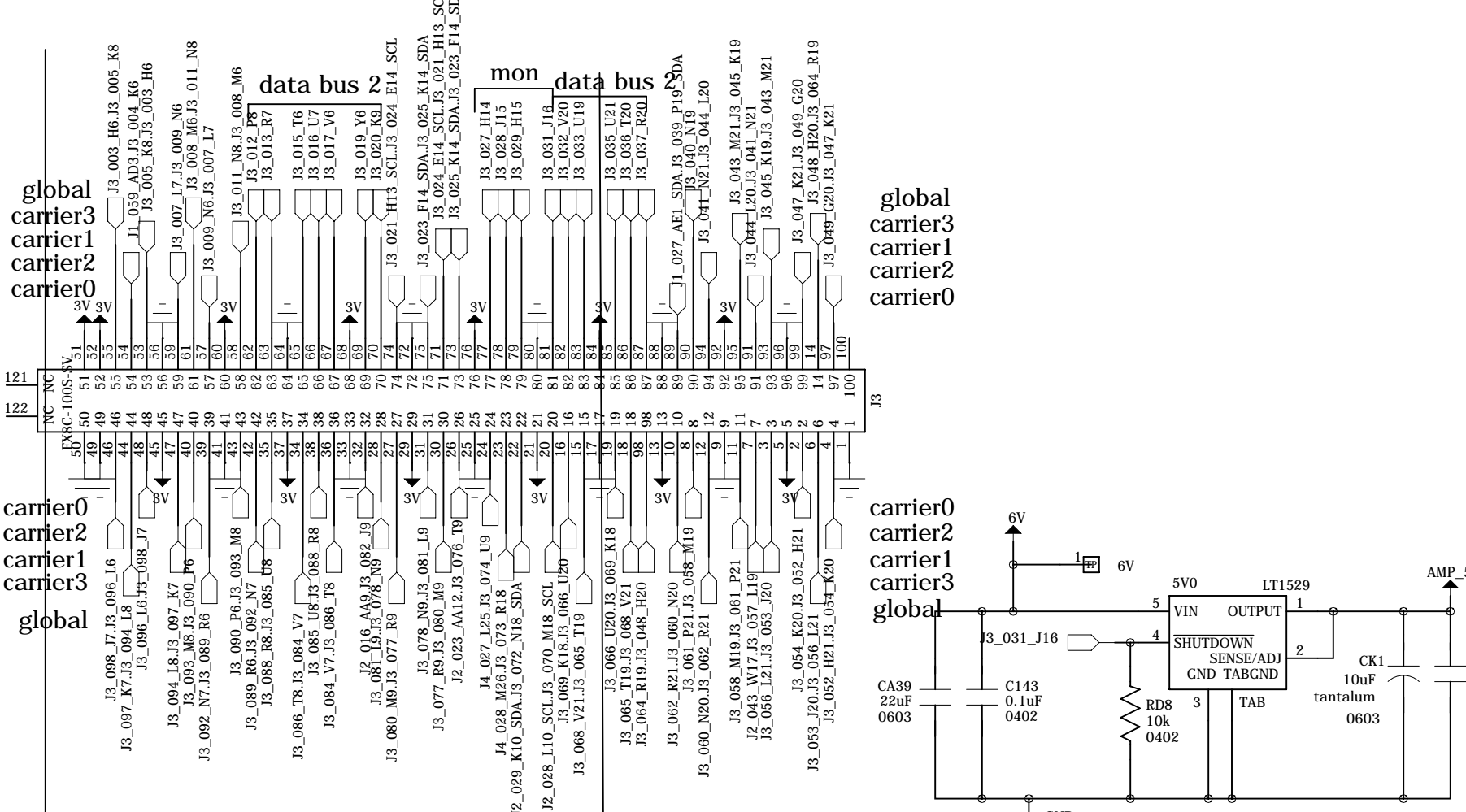
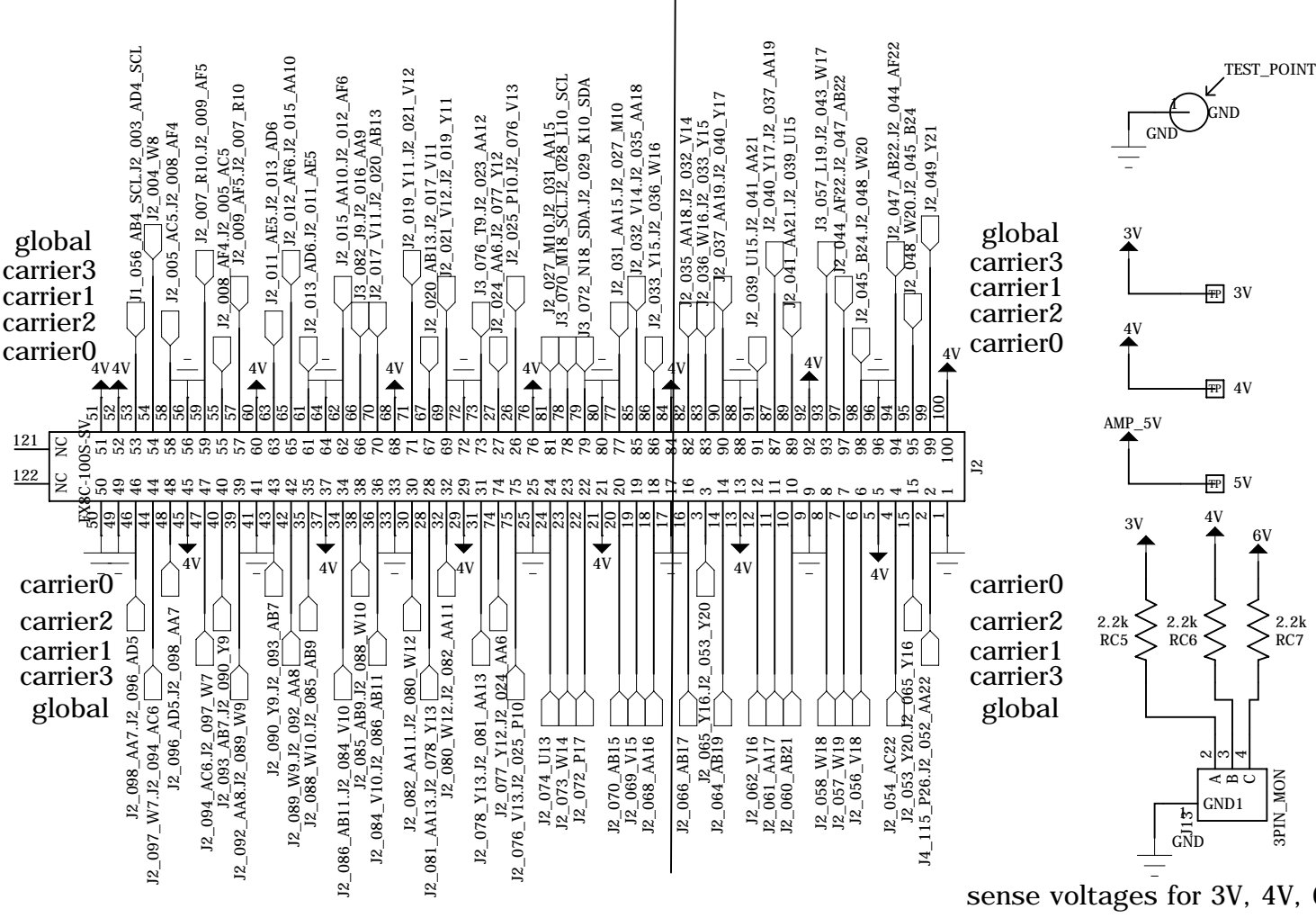
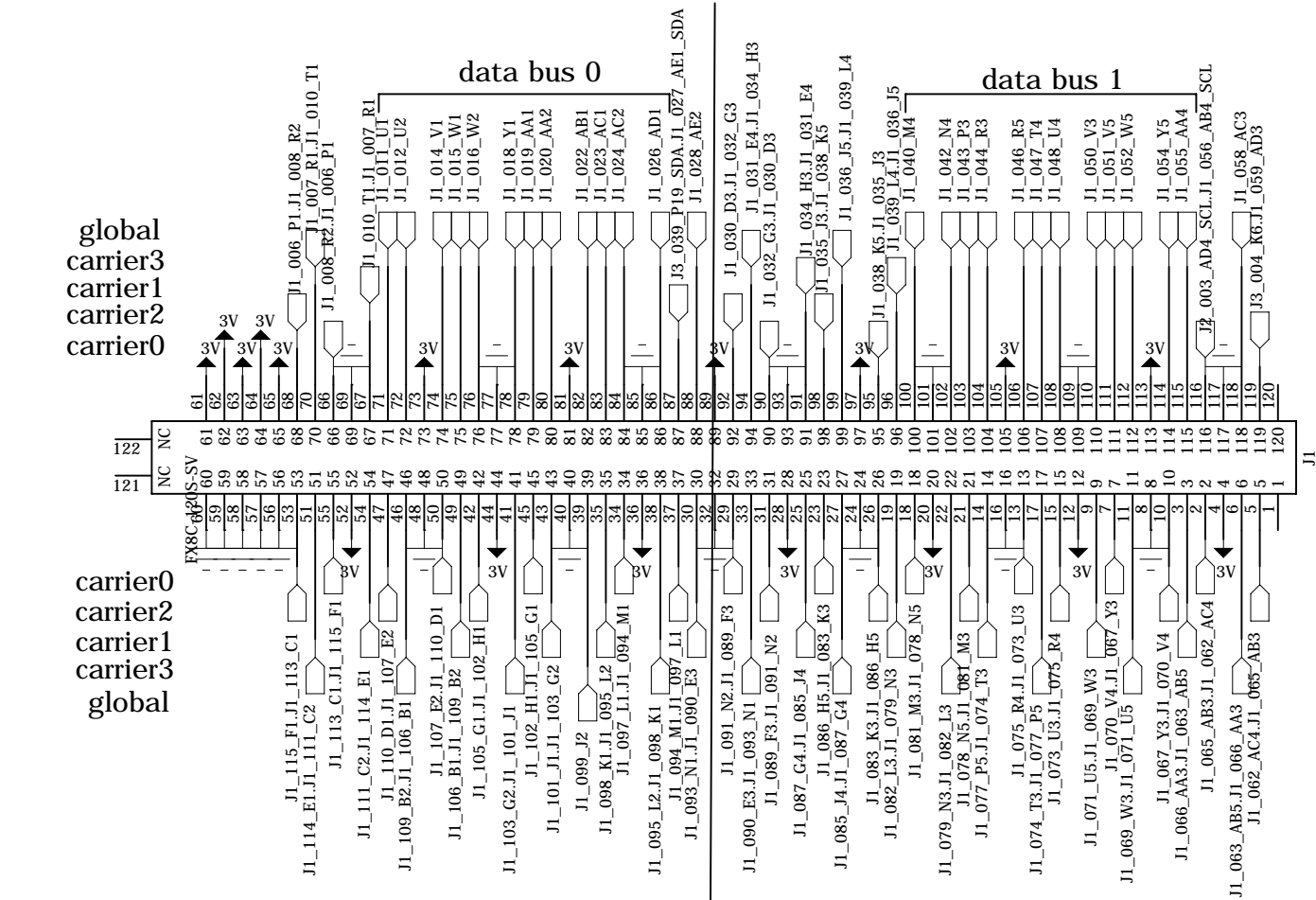
E

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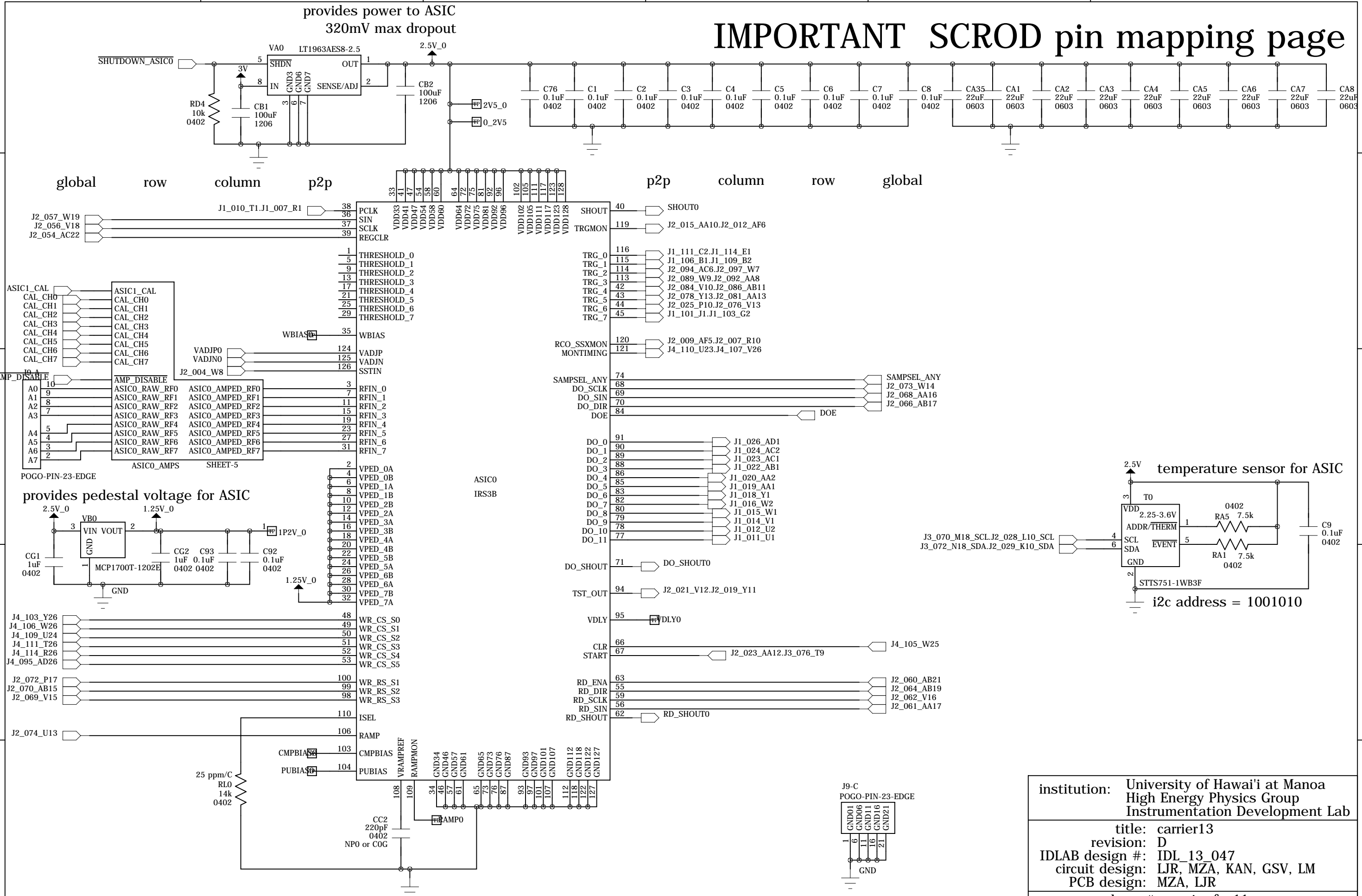
C

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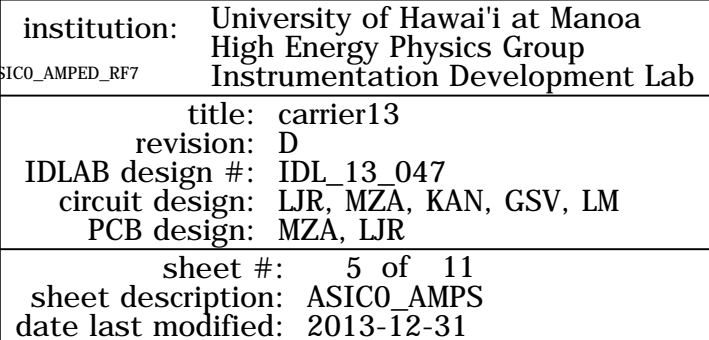
A



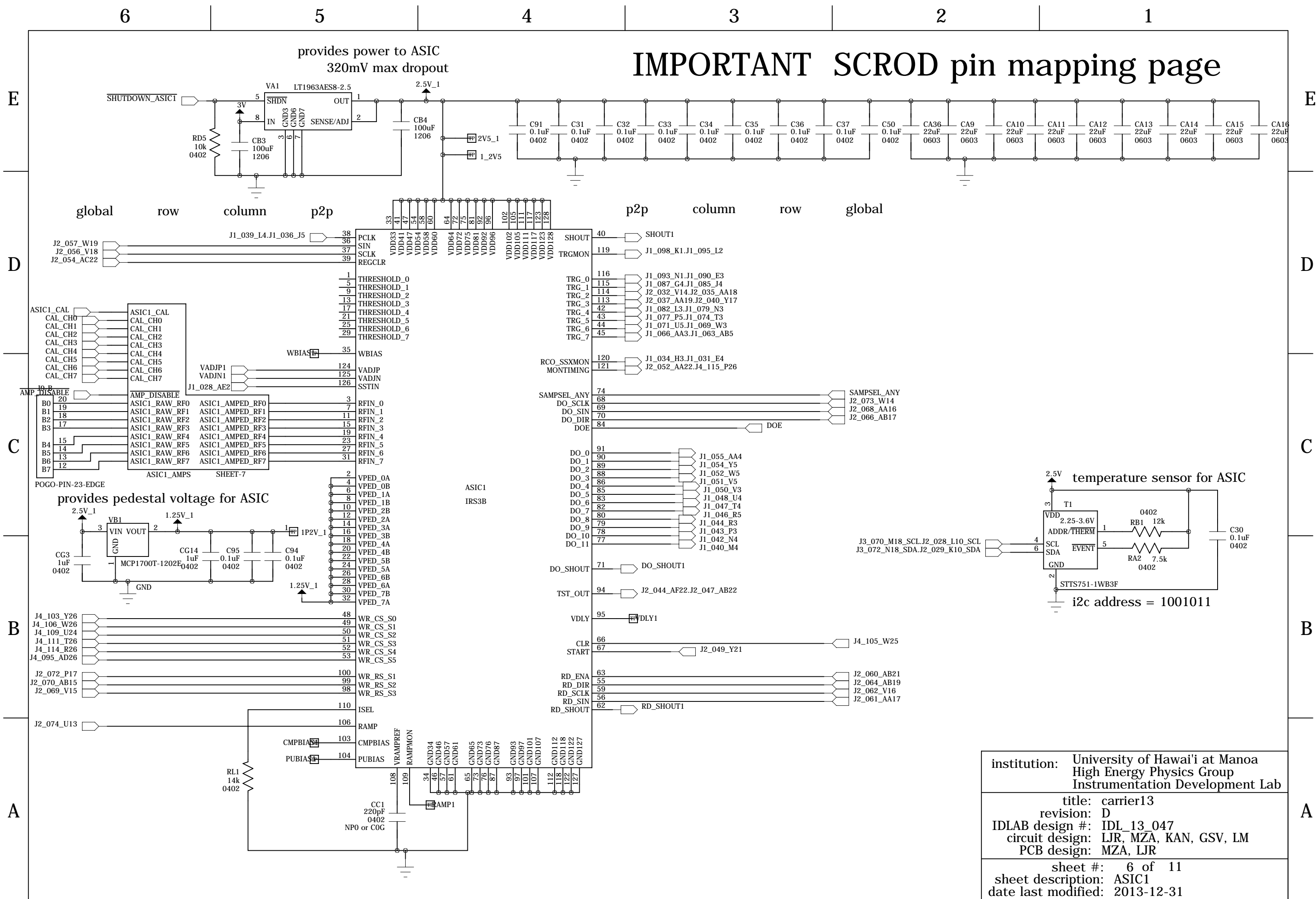
IMPORTANT SCROD pin mapping page



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier13
revision:	D
IDLAB design #:	IDL_13_047
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR
sheet #:	4 of 11
sheet description:	ASICO
date last modified:	2013-12-31



IMPORTANT SCROD pin mapping page



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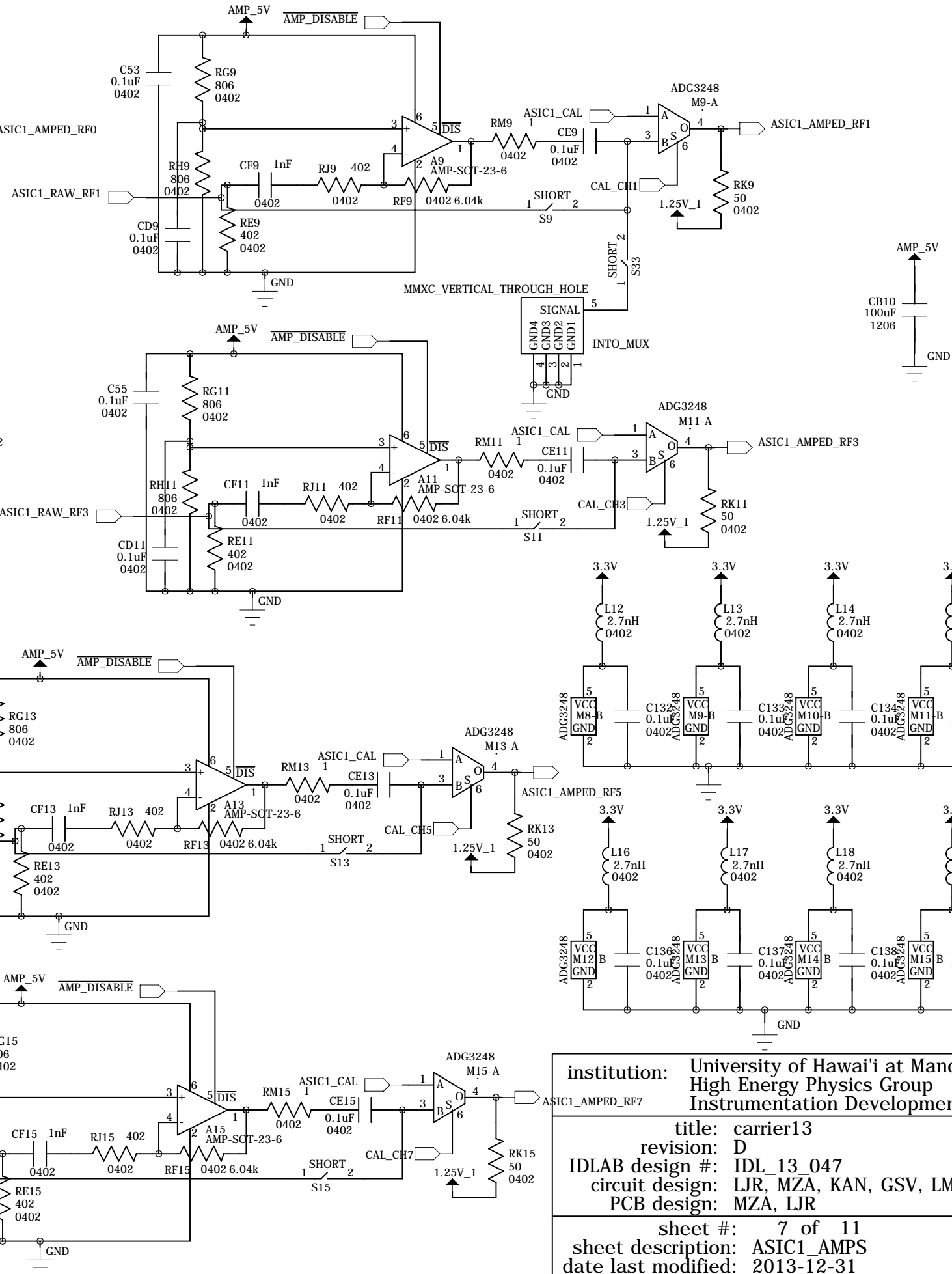
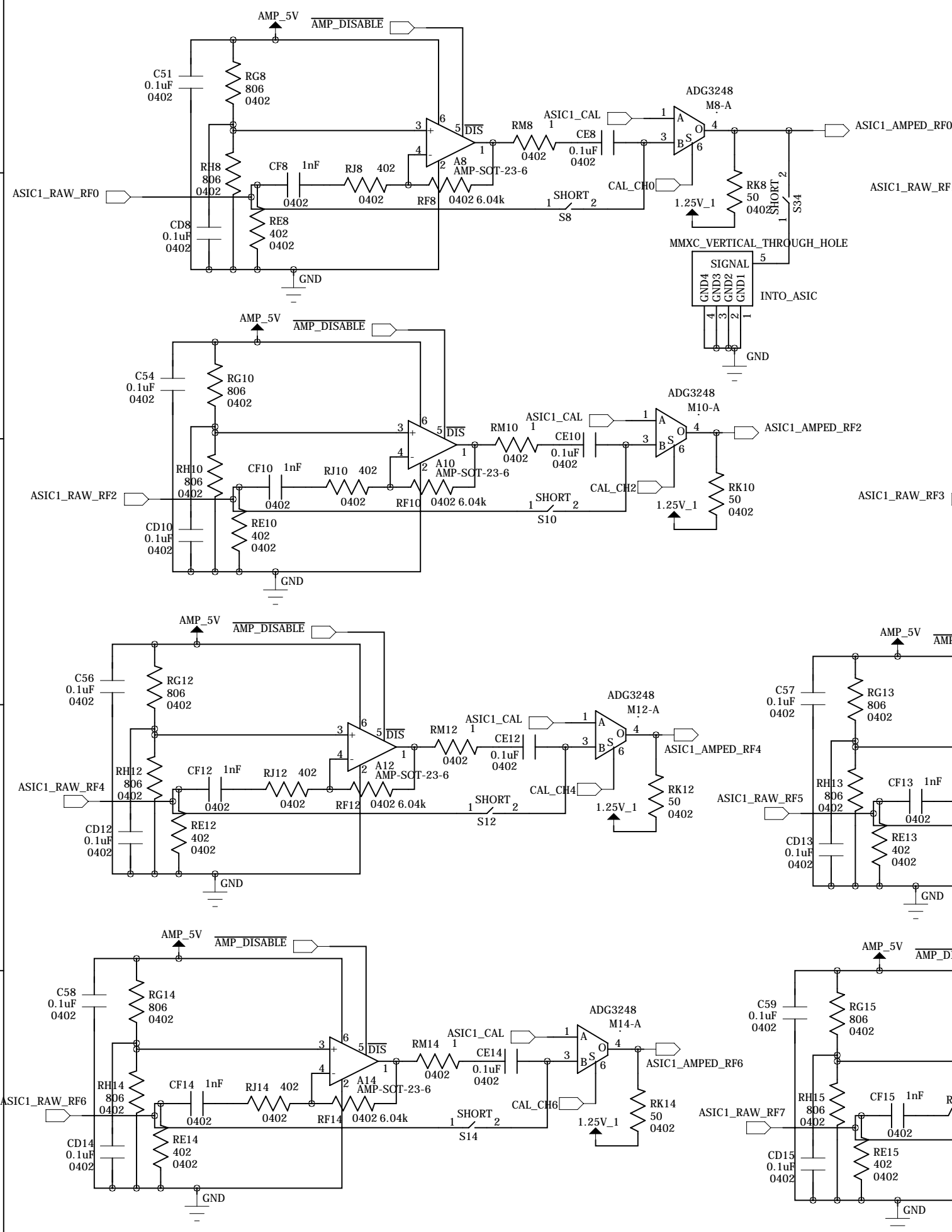
E

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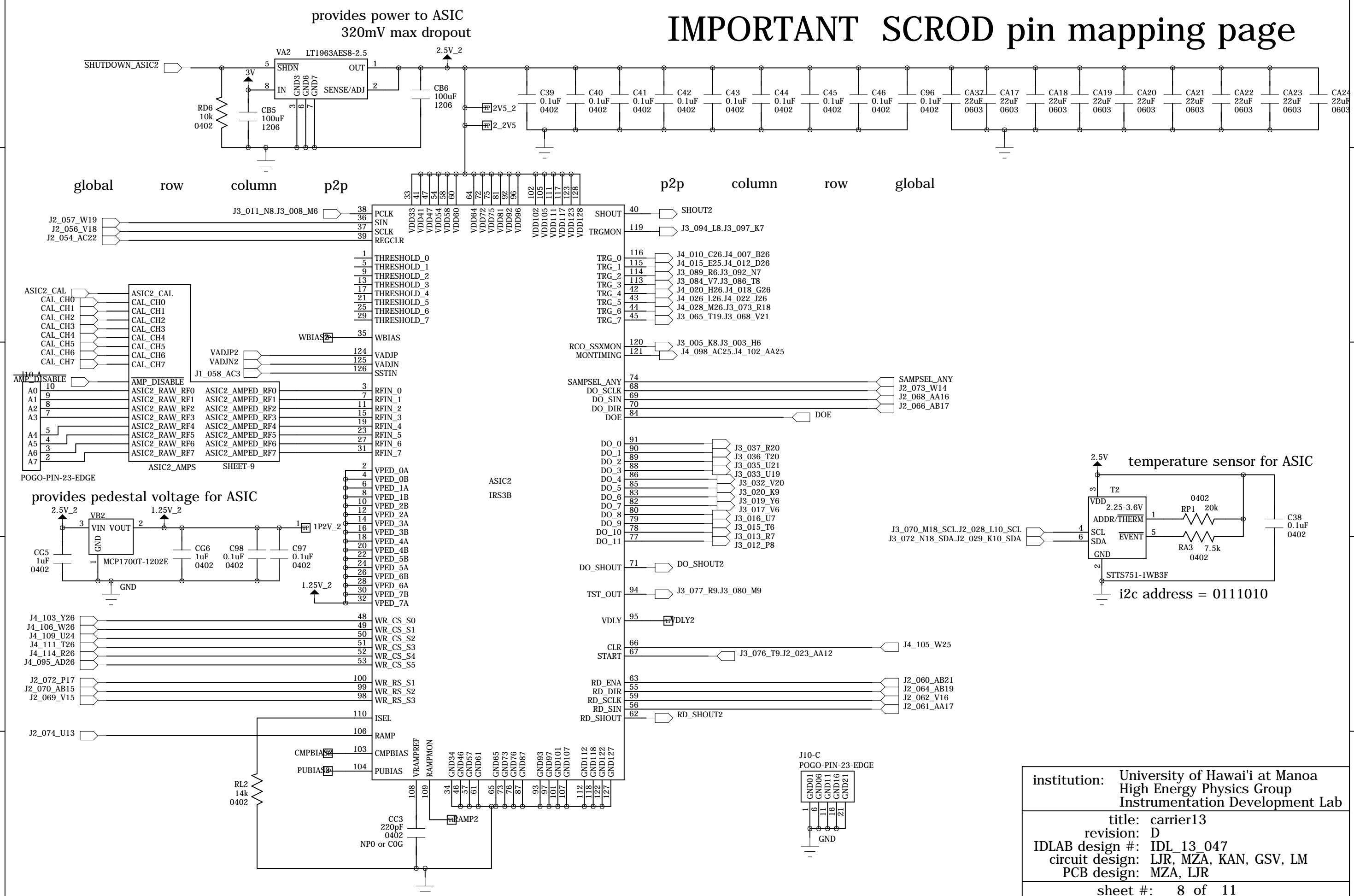


institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

title: carrier13
revision: D
IDLAB design #: IDL_13_047
circuit design: LJR, MZA, KAN, GSV, LM
PCB design: MZA, LJR

sheet #: 7 of 11
sheet description: ASIC1_AMPS
date last modified: 2013-12-31

IMPORTANT SCROD pin mapping page



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier13
revision:	D
IDLAB design #:	IDL_13_047
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR
sheet #:	8 of 11
sheet description:	ASIC2
date last modified:	2013-12-31

6

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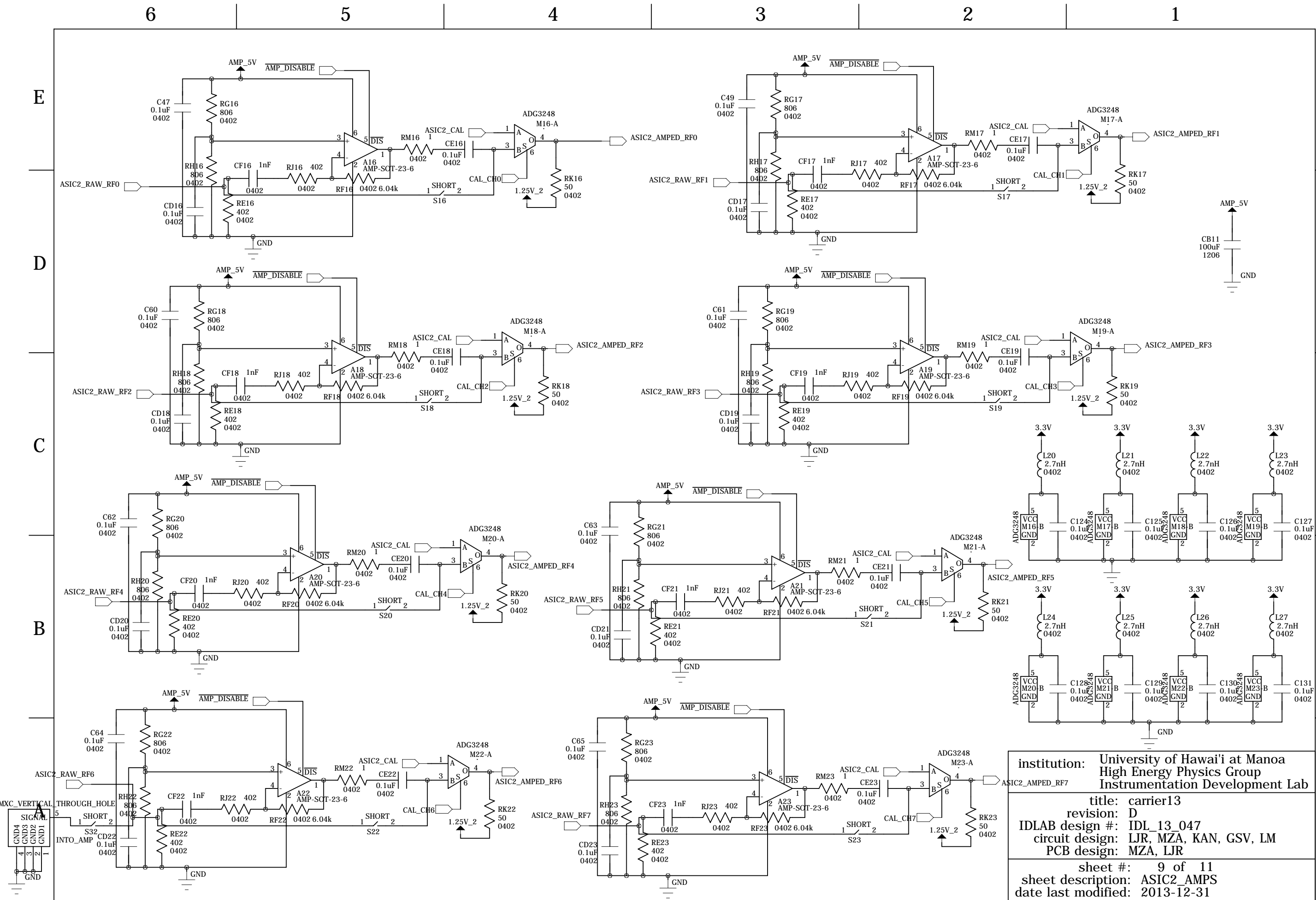
C

C

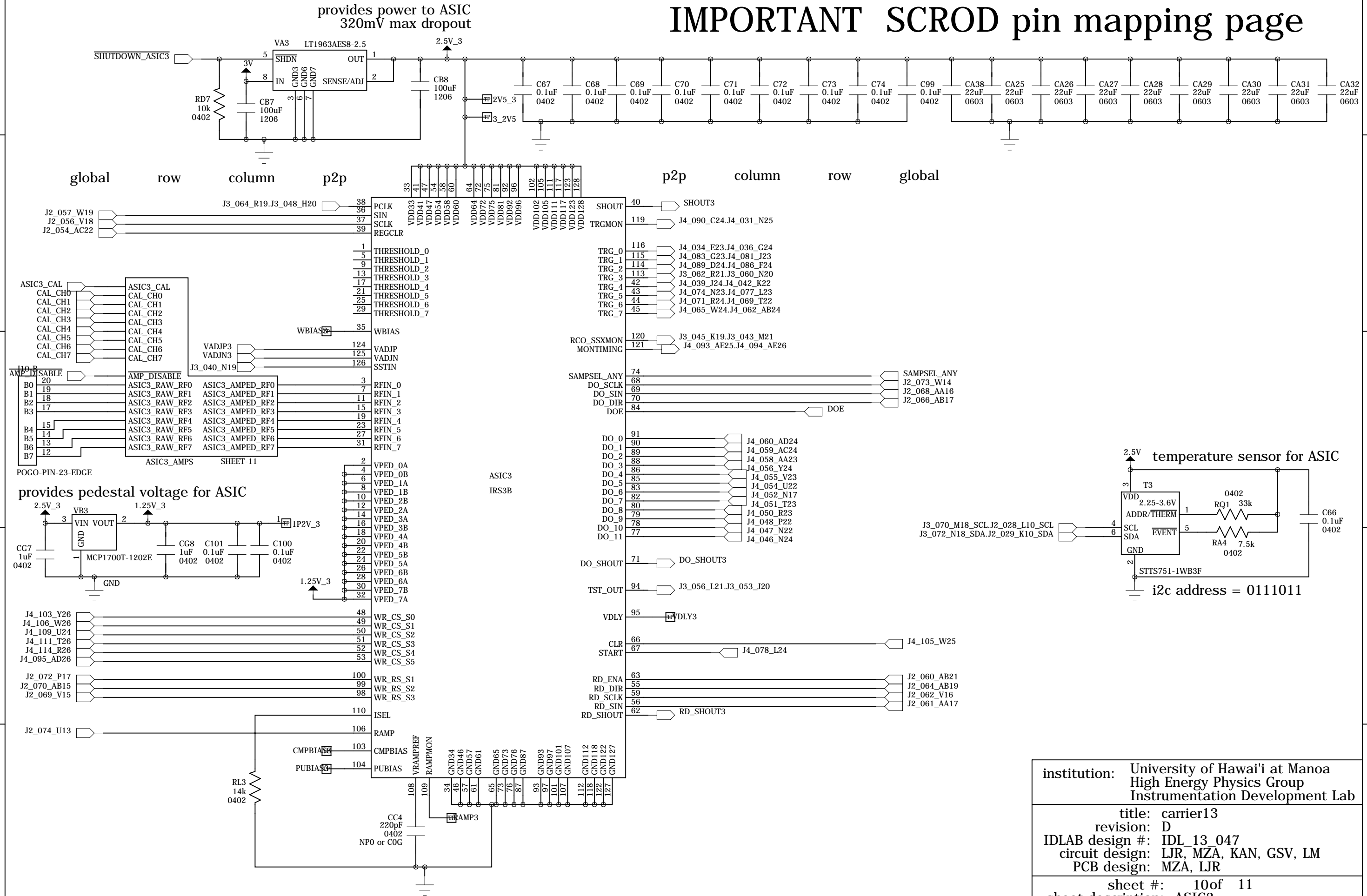
B

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IMPORTANT SCROD pin mapping page



institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

```

title: carrier13
revision: D
IDLAB design #: IDL_13_047
circuit design: LJR, MZA, KAN, GSV, LM
PCB design: MZA, LJR

```

sheet #: 10 of 11
sheet description: ASIC3
date last modified: 2013-12-31

6

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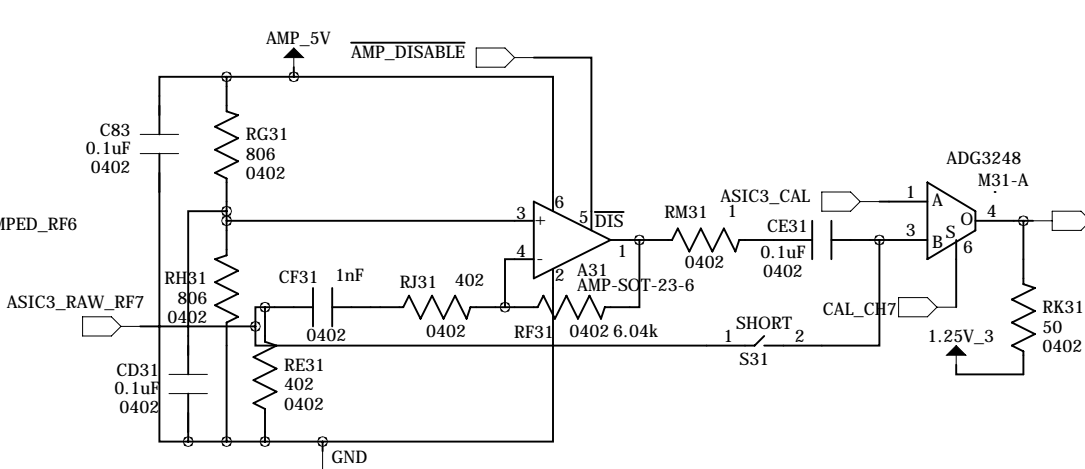
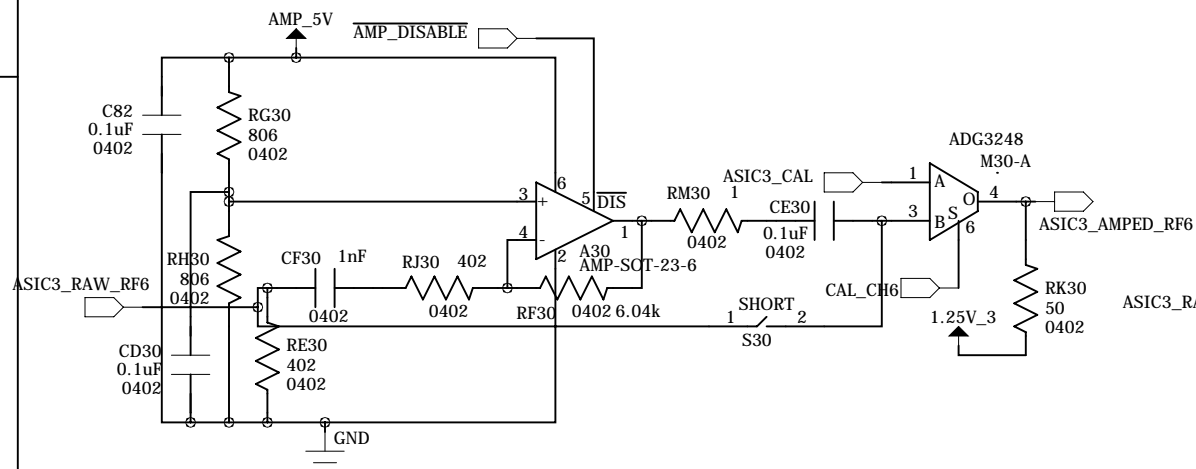
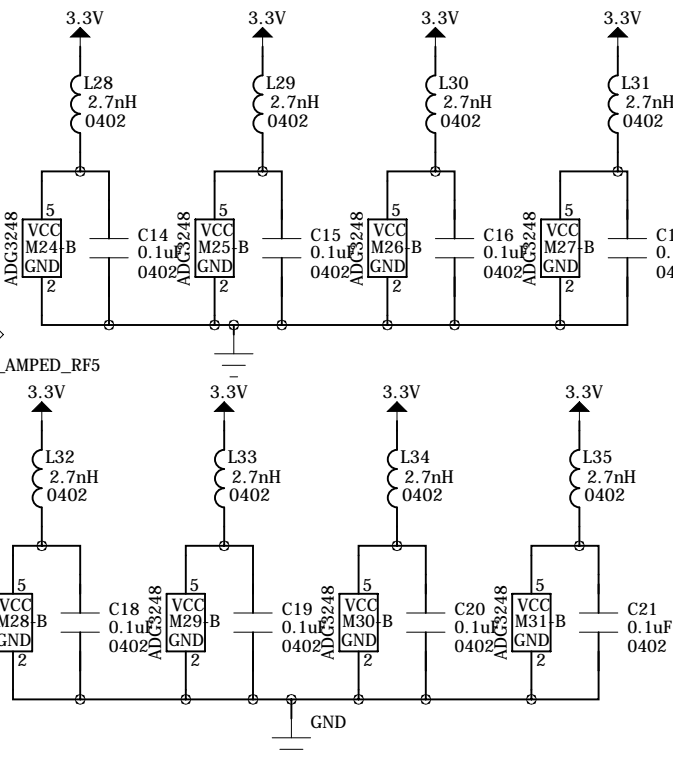
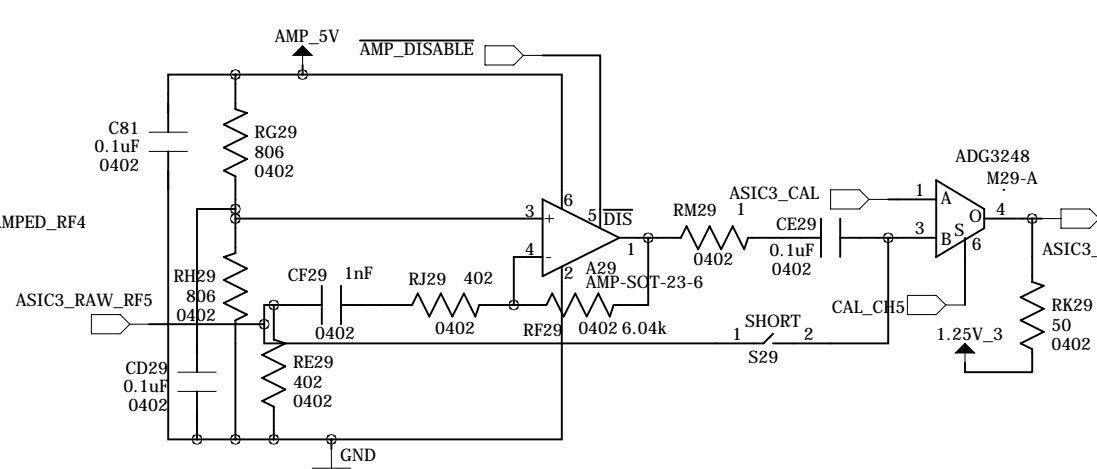
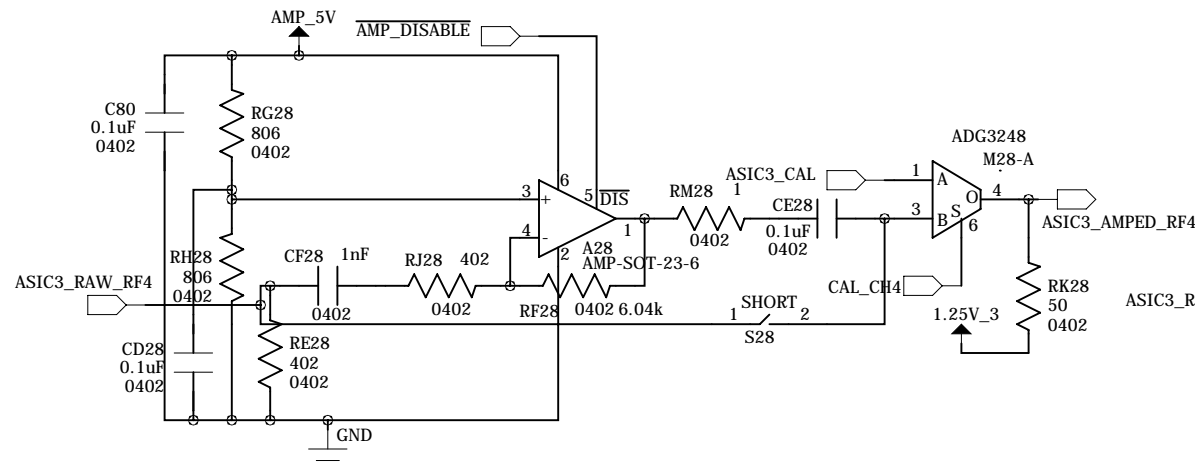
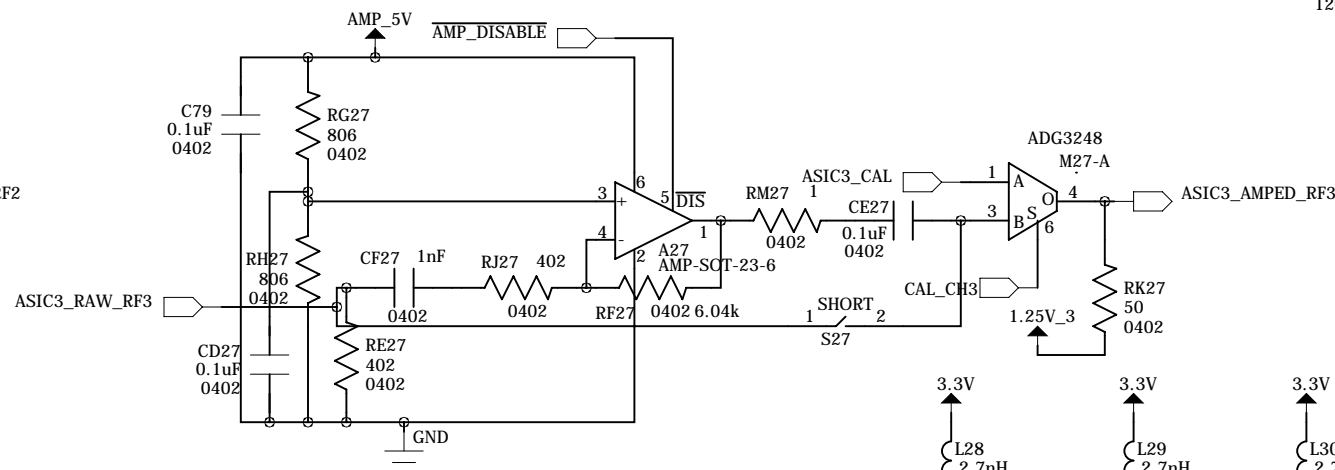
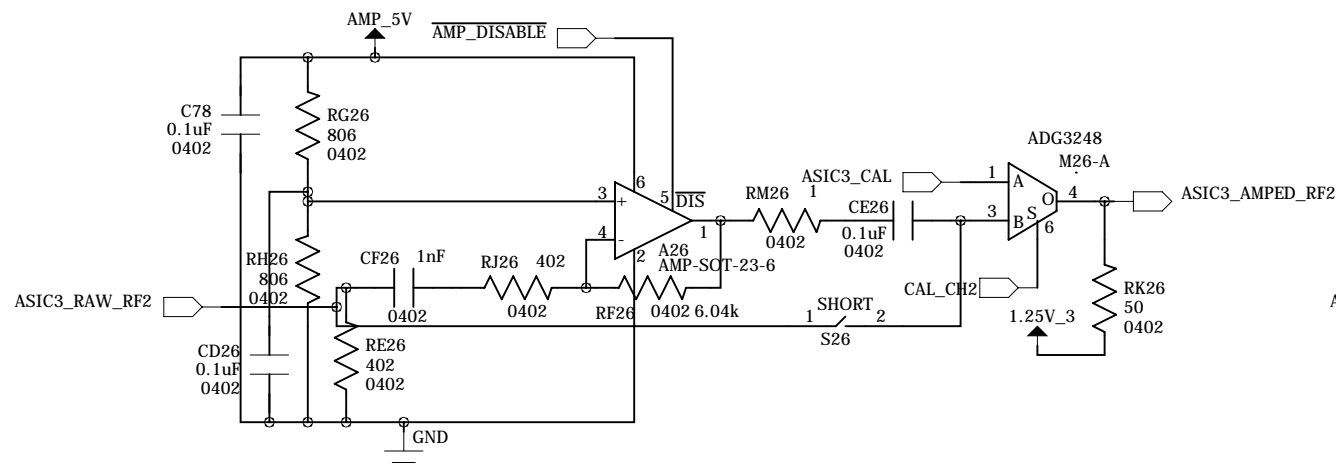
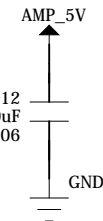
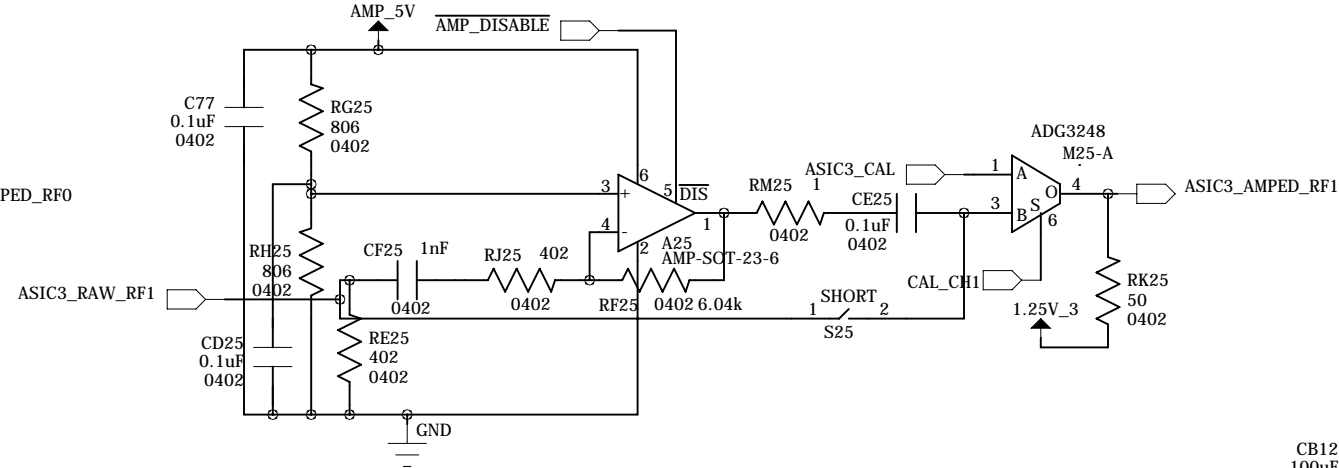
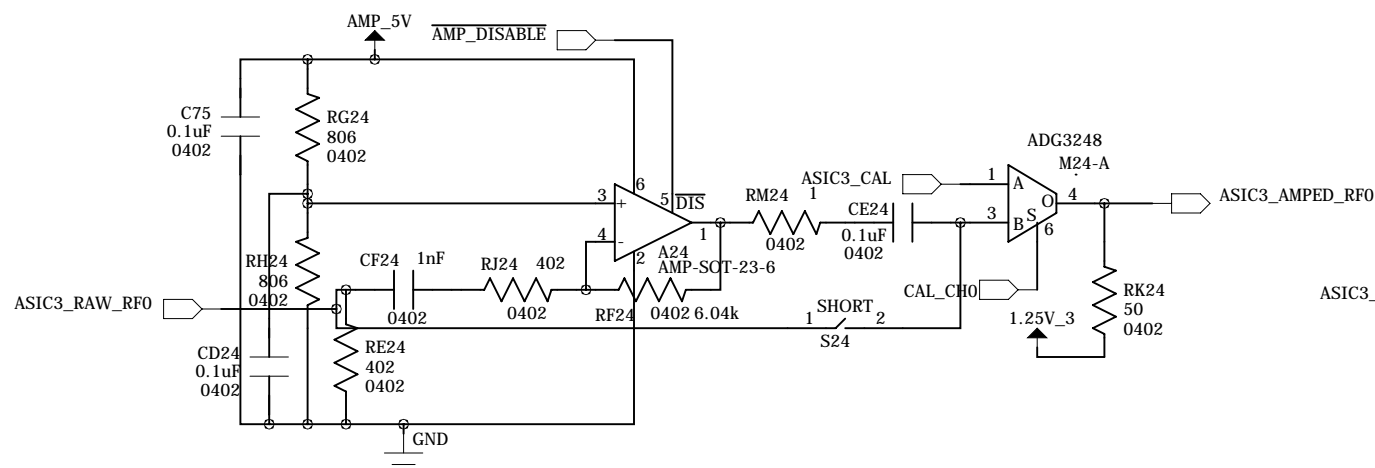
E

D

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A



institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

title: carrier13
revision: D
IDLAB design #: IDL_13_047
circuit design: LJR, MZA, KAN, GSV, LM
PCB design: MZA, LJR

sheet #: 11 of 11
sheet description: ASIC3_AMPS
date last modified: 2013-12-31