notes for end-user:
   RAW1 should be set to 1.87 V measured at the board (which is ~8.1 V at the other end of a 24 m long 18 AWG cable)
   RAW2 should be set to 3.15 V measured at the board (which is ~7.6 V at the other end of a 24 m long 16 AWG cable)
   RAW3 should be set to 4.33 V measured at the board (which is ~8.1 V at the other end of a 24 m long 20 AWG cable)
the 2mm jumpers on SCROD revB are closed=
   to run the board in Belle-II mode, all jumpers should be removed/open; see other sheets for more info on benchtop use

progress / timeline:
   2013-11 (mechanical mockup):
      holes for vertical mini-USB connector are too small (fixed in January 2014)
      maybe switch to actual press-fit holes since they're otherwise very close to the thermal wall landing
      the JTAG connector outline is slightly wrong
      need mounting holes in FMC decal
   2014-01:
      defined FPGA schematic symbol and power pins
   2014-02:
      wired up LT3055 and LT3086 linear voltage regulators
   2014-03
      rotated FPGA and adjusted power pours accordingly (went to 10 layer board)
   2014-04:
      wired up USB transceiver to PS MIO pins
      LPDDR2 RAM
      added 330 Ohm; [ug470 page 24 says we could use a 330 Ohm resistor on DONE; do we need to (wording is unclear in datasheet)?]
      fixed connectivity problem (PS_ENABLED AND PL_ENABLED were unconnected)
      fixed error on FMC mosfet logic
      added extra stage of isolation between PS_AND_PL_POWERED and $\overline{\text{INIT}}$ so FPGA doesn't de-power other boards duing programming
      added connections to FMC_LPC to mimic the first set of MGT lanes to pseudo-carrier
      LT3055 needs a minimum of 2V in; swapped several RAW1's going into LT3055s for RAW2's
      wire up another MGT channel to the FMC board
      set voltage resistors were wrong in several places; fixed
      running start-up logic on 2.5V instead of RAW2
      added pfet+nfet to each LT3055/LT3086 to ensure supplies come on sequentially
      boot mode pull-up/downs (re-purposed a DIP switch for QSPI/JTAG mode; PS PLL disabled)
      used JTAG cable presence detect to change JTAG mode (followed ug593 page 16)
      do we need termination resistors to calibrate DCI on VRP/VRN on banks 33, 34, 35? ug471 page 47 says no for LVDS
      not sure how to handle sequencing of PS_POR and PS_CLOCK in JTAG mode, so added DNI resistors to select, and wired one to a PL IO
      added mounting holes to FMC decal
      added logic so that all three supplies must be at least 0.5 V before anything on the board will power on
      added LED for DONE pin, and each stage of the supply sequencing to indicate which are not working
      added DIP switch to enable LEDs
      made connections from HR banks to FMC connector
      changed to press-fit holes for SFP+, and made board cutouts smaller
      added muxtree for CAL and connected it to board-to-board connector
      '348 was not enabled; fixed
      PL_IS_POWERED was not pulled up; fixed
      made LVDS TDO a 1 by default instead of a 0
      removed p-fet for Vref on FMC connector (comes from 2V5_VCCO)
      removed JTAG demultiplexers; shorted JTAG header pins to LVDS-to-single-ended outputs; JTAG cable header pin 13 disables LVDS-to-single-ended outputs (high Z)
      FMC board now in JTAG chain, when FMC_PRESENT is low
      added bypass resistor to omit FPGA on SCROD from chain (for testing carriers standalone)
      changed DIP switches to 2mm jumper headers (so we can enable various functions in situ without soldering; additional J2-A connected to PS and J2-B connected to PL)
      switched GTX regulators to LT3086es (current draw will be more than 500mA) drawing from RAW1 (this saves >5W); changed RAW1 to 1.7V (so we can run 1.2V regulators on it)
      added some logic to ensure the 2V5 and 3V3 regulators are power=good before allowing the rest of the regulators to sequence
      removed LED for 2V5/3V3 = not up, as it relied on them being up...
   2014-05:
      removed unwanted parallel output terminator for TTL_TRIG_OUT; rewired it to be a series source termination
      added cdclvd1208 2:8 lvds fanout buffer for incoming clock/board clock to 5 FPGAs' MGT clock inputs; rewired MGT clock fanout correspondingly
      swapped LA31 and LA01_CC from FMC so LA01_CC goes into a MRCC
      swapped GTX duals to shorten trace lengths
      swapped 0402 (1/16W) termination resistors for 1206 (1/2W)
      made cal fanout tree
      carrier0_present was pulled up twice (fixed), as was FMC_PRESENT
      relized someone might sell a part that is a non-inverting buffer with open-drain (TI sells a dual in a SC-70-6 package); this saves components and board area
      q28 and q29 form a nice power-to-ground short if the gate voltage is between 0.6V and 1.9V...; replaced with the "spare" digital buffer
      determined dielectric stackup, trace thicknesses and spacing for differential pairs and single-ended signals on top and inner routing layers
      realized discrete digital buffer can't drive 50 Ohms, switched to a pair of transistors and inverted signal name
      had many sch to pcb "database connection problems" that had to be fixed...
      wired extra clock fanout outputs to MRCC inputs on FPGA
      added part numbers to all components to ease creation of BoM
      fit all components on board (preliminary placement); xilinx recommendations for decoupling caps changed considerably...
      rearranged IO placement to ease board routing
      expanded breadboard size to fill available space
      re-grouped connections on board-to-board connectors to ease routing on carrier revE
      nudged things around a bit in layout; fixed MSOP-16 footprint, as it did not match a part in hand
   2014-06:
      rewired some things to help with layout
      added 2 sets of GTX connections to boardstack connectors; added GTX clock from boardstack connectors; rewired some things to help with layout
      gave up trying to appease autorouter and manually routed the GTX pairs and the FMC connector manually
      manually routed clock fanout traces so all carriers should get a nearly in-phase clock; rewired some things to aid layout
   2014-07:
      change CG78 & CG79 from 100nF to 100pF (now called CM1 and CM2)
      add 4V regulator for cal amps, as well as connection to board-to-board connector
      added test point for PS_CLOCK in case we have to drive it externally
      matched trace lengths for LPDDR2 byte banks; lengthened clock traces so all signals arrive before clock
      changed pad size from 0.6mm to 0.45mm as recommended by ug865 page 80; stopped using soldermask defined pads
      took unused 127 MHz output and divided it with flip-flips to drive PS_CLOCK
      swapped power for one of the dual digital buffers to come from 2V5_MIO
      added 2.5V to keying to help save pullup resistor space on carrier boards
      added pullup to temperature sensor output
      finished routing board
      back-annotated a few part numbers that were wrong in the BoM
   2014-08:
      changed lmh6659 to buf602 due to higher bandwidth measurement @ 4V

layer stackup:
   1.4 mils copper (top; components and routing)
3.15 mils
   1.4 mils copper (ground plane)
8 mils
   1.4 mils copper (routing)
8 mils
   1.4 mils copper (ground plane)
3.15 mils
   1.4 mils copper (power plane)
3.15 mils
   1.4 mils copper (power plane)
3.15 mils
   1.4 mils copper (power plane)
3.15 mils
   1.4 mils copper (power plane)
3.15 mils
   1.4 mils copper (ground plane)
8 mils
   1.4 mils copper (routing)
8 mils
   1.4 mils copper (ground plane)
3.15 mils
   1.4 mils copper (bottom; components and routing)

C =	0.47	uF
CA =	4.7	uF
CB =	47	uF
CC =	10	nF
CD =	100	uF ???
CF =	680	uF polarized
CG =	0.1	uF
CH =	10	uF 0603
CJ =	270	pF
CK =	12	pF
CL =	22	uF 0603
CM =	100	pF

R =	10k	
RA =	15.4k	
RB =	100	
RC =	200k	
RD =	60.4k	
RE =	121	
RF =	40.2k	
RG =	121k	
RH =	12k	
RJ =	16k	
RK =	7.150k	
RL =	1k	
RM =	196k	
RN =	61.9k	
RP =	280k	
RQ =	340k	
RR =	13.7k	
RS =	4.7k	
RT =	50	
RU =	7.5k	
RV =	1	
RW =	8.06k	
RY =	40	
RZ =	240	
RAA =	330	
RAB =	57.6k	
RAC =	20k	
RAD =	57.6	
RAE =	374	
RAF =	50	(1/2W 1206)
~~RAG =~~	~~75~~	
RAH =	174	
RAJ =	69.8	

notes for designer:
   ug585 page 618 says the 7z045 needs 106,571,232 bits of configuration memory for the PL
   unsure CDC pins can be left floating in LT3086 (seems okay in LTspice)
   PWRBAD pin on LT3055 seems to not be held low while in shutdown...
   there is no info on how much power the MGT/GTX use per quad (need post-implemenation spreadsheet)

outstanding questions:
   is the "filter" for the fiber transceiver power acting as a useful filter? (replaced the inductor with a 1 Ohm resistor)
   need to look into termination for the JTAG signals (ug470 page 60 says TCK must be terminated)
   to keep the device reliable for 10 years, we might need a heatsink (ug865 page 65) to couple the die temperature to the board better than the FFG900 package does by itself
   need to check footprints

things for SCROD revB2:
   add signals down boardstack to indicate power-up status
   maybe add a way to disable the cal signal from propagating?
   maybe add a temperature sensor near the thermal wall
   the 200k could be replaced with the (already used) 196k

institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

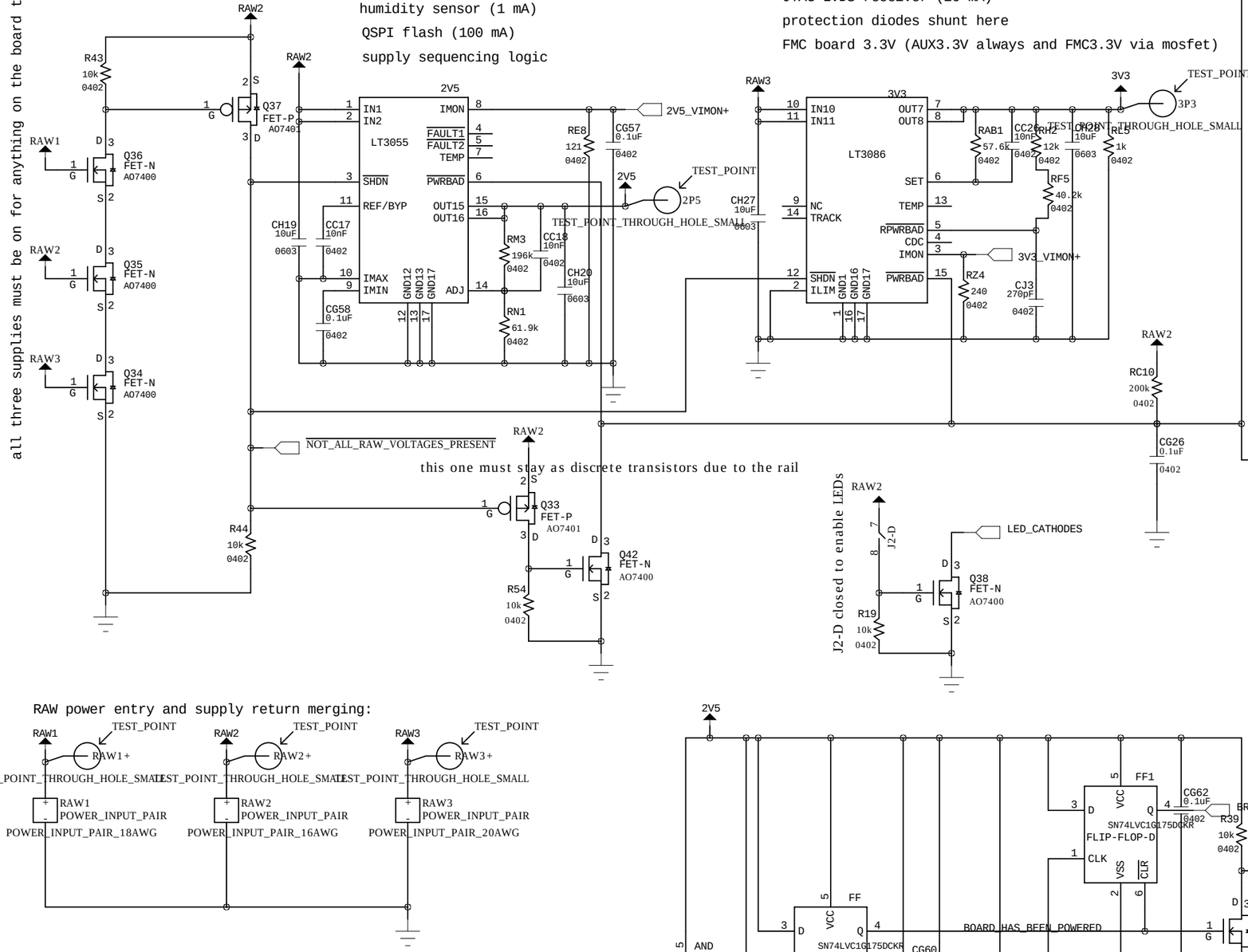
title: SCROD
revision: B
IDLAB design #: IDL_14_002
circuit design: MZA, JLB, KAN, KRO, GV, BK, LW
PCB design: MZA

sheet #: 1 of 11
sheet description: NOTES
date last modified: 2014-08-01

all three supplies must be on for anything on the board to be powered

this 2.5V regulator supplies:
oscillator (70 mA)
various pull-ups (1 mA)
humidity sensor (1 mA)
QSPI flash (100 mA)
supply sequencing logic

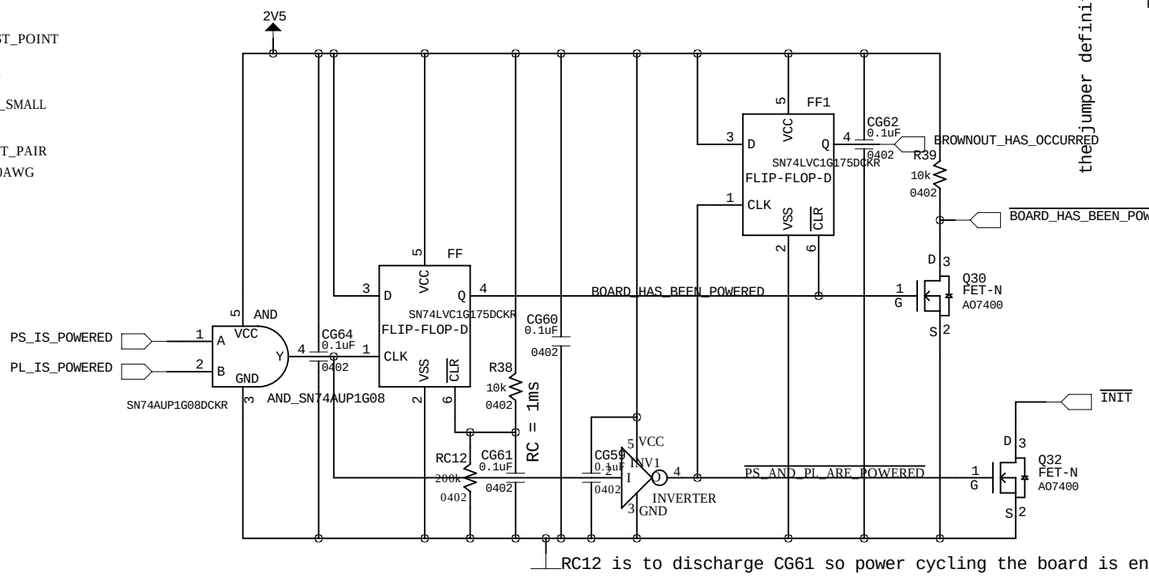
this 3.3V regulator supplies:
USB (12 mA)
QSPI flash (100 mA)
both fiber transceivers (470 mA)
JTAG LVDS receiver (20 mA)
protection diodes shunt here
FMC board 3.3V (AUX3.3V always and FMC3.3V via mosfet)



J1-A DISABLE_PS	J1-B WAIT_FOR_PL	PL_IS_POWERED	PS_SHOULD_POWER_UP
up	x	x	0
down	up	0	0
down	up	1	1
down	down	x	1

J1-D DISABLE_PL	J1-C IGNORE_PS	PS_IS_POWERED	PL_SHOULD_POWER_UP
up	x	x	0
down	up	x	1
down	down	0	0
down	down	1	1

RAW power entry and supply return merging:



PS_IS_POWERED	PL_IS_POWERED	PS_AND_PL_ARE_POWERED	INIT
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

BOARD_HAS_BEEN_POWERED
1 for at least first 1 ms after 2V5 supply is stable
0 after the first time PS_AND_PL_ARE_POWERED is pulsed

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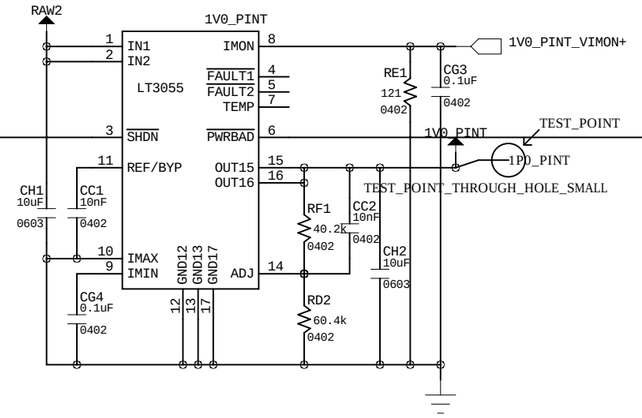
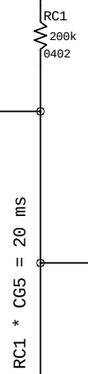
PCB design:	MZA
sheet #:	2 of 11
sheet description:	POWER_ENTRY_AND_SEQUENCING
date last modified:	2014-08-01

PS_SHOULD_POWER_UP

PINT = 1V; 122 mA quiescent + 70 mA @ power-on = 192 mA peak

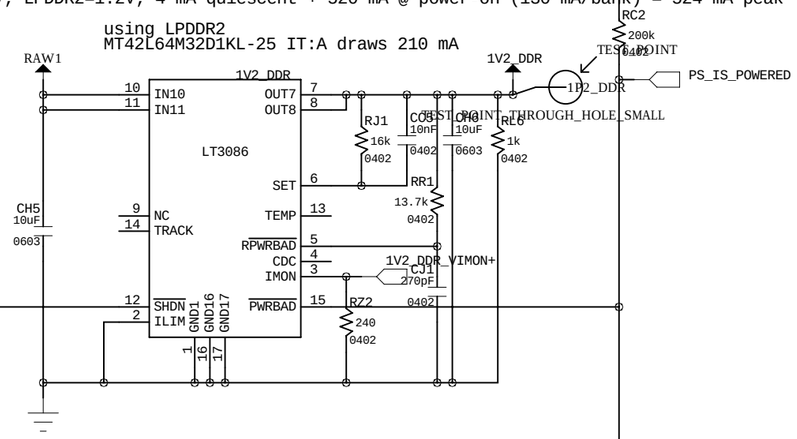


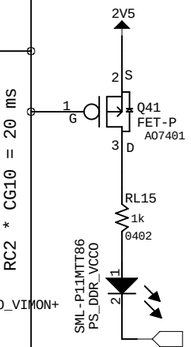
RC1 * CG5 = 20 ms

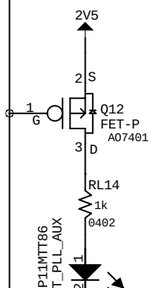


DDR2=1.8V; DDR3=1.5V; LPDDR2=1.2V; 4 mA quiescent + 520 mA @ power-on (130 mA/bank) = 524 mA peak

using LPDDR2
MT42L64M32D1KL-25 IT:A draws 210 mA

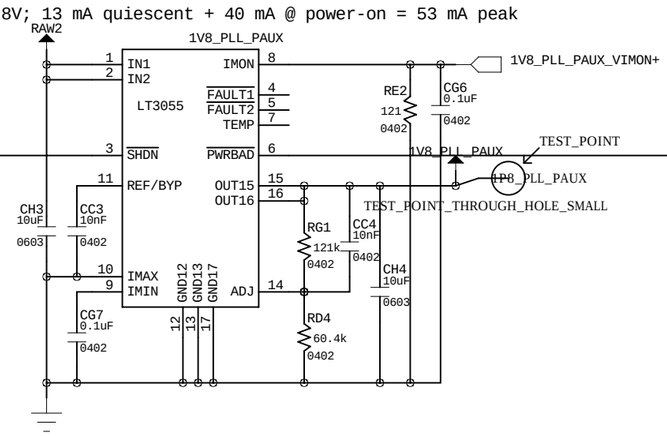




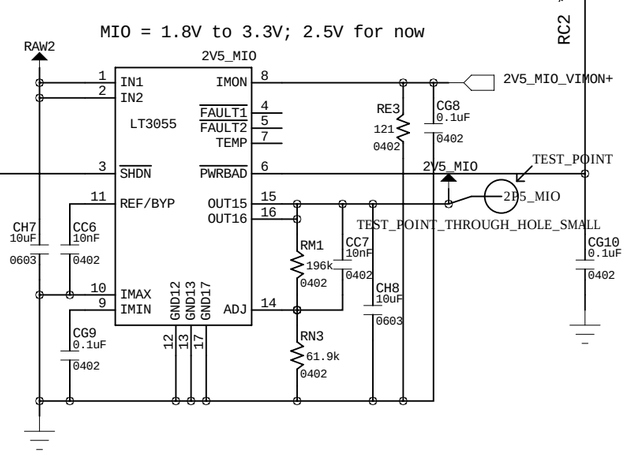


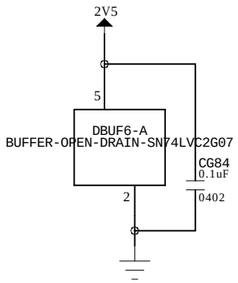
RC2 * CG10 = 20 ms

PAUX = 1.8V; 13 mA quiescent + 40 mA @ power-on = 53 mA peak



MIO = 1.8V to 3.3V; 2.5V for now





institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	B
IDLAB design #:	IDL_14_002
circuit design:	MZA, JLB, KAN, KRO, GV, BK, LW
PCB design:	MZA
sheet #:	3 of 11
sheet description:	PS_VOLTAGE_REGULATORS
date last modified:	2014-08-01

total 8 stages of 20 ms RC filter for both PS and PL sequencing; LTspice simulation shows about 200 ms between power being applied and the PS_AND_PL_ARE_POWERED signal going high

BRAM = 1V; 23 mA quiescent + 90 mA @ power-on = 113 mA peak

INT = 1V; 611 mA quiescent + 1400 mA @ power-on = 2011 mA peak

AUX = 1.8V; 131 mA quiescent + 60 mA @ power-on = 191 mA peak

AUXIO = 1.8V; 2 mA quiescent + 400 mA @ power-on = 402 mA peak

VCCO = 1.2V to 3.3V; 40 mA quiescent + 900 mA @ power-on = 940 mA peak
(for all HR and HP banks together)

can tie MCTVCCAUX to VCCAUX because QPLLs are unused (only true in non-zynq 7-series)
ug585 page 614 has details on selecting RAM (LPDDR2 seems best)

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PCB design:	MZA
sheet #:	4 of 11
sheet description:	PL_VOLTAGE_REGULATORS
date last modified:	2014-08-01

notes on cap counts are from cap count from ug933 (sept '13), but the recommendations changed by the december '13 version

cap count from ug933 z-7045 ffg900 (pages 13-14)

voltages from ds191 page 3

MGT cap count from ug476 page 307

zynq 045 quiescent currents from ds191 page 7

90 mA power-on current (on top of quiescent)
23 mA quiescent
(2) 100uF @ Vcc_bram
(1) 47uF @ Vcc_bram
(6) 4.7uF @ Vcc_bram
(12) 0.47uF @ Vcc_bram
Vcc_bram = 1V

CD1 100uF 1210
CA1 4.7uF 0402
CA4 4.7uF 0402
C1 0.47uF 0402
C2 0.47uF 0402
C3 0.47uF 0402
C4 0.47uF 0402

1V0_BRAM

(1) 100uF @ Vcc_o (each bank)
Vcc_o = 1.2V to 1.8V (HP)
Vcc_o = 1.2V to 3.3V (HR)

90 mA power-on current per bank (on top of quiescent)
4 mA quiescent (each VCCO)
1.2 to 1.8 or 1.2 to 3.3 for each VCCO

2V5_VCCO	1V8_VCCO	1V8_VCCO	1V8_VCCO	1V8_VCCO	2V5_VCCO	2V5_VCCO	2V5_VCCO	2V5_VCCO	2V5_VCCO	1V8_AUXIO	1V8_AUX	1V0_INT	
CD3 100uF 1210 HR	CD10 100uF 1210 HP	CD11 100uF 1210 HP	CD12 100uF 1210 HP	CD13 100uF 1210 HR	CD14 100uF 1210 HR	CD15 100uF 1210 HR	CD16 100uF 1210 HR	CB5 47uF 1812		CB4 47uF 1812	CB1 47uF 1812	CA5 4.7uF 0402	CF1 680uF E
													CF2 680uF E
Y19 AC20	L16 H15 E14 D17 B13 A16	K9 J12 G8 F11 D7 C10 A6	L6 J2 H5 F1 E4 B3	V25 U28 T21 R24 P27 N30	Y29 AK29 AG28 AD27 AC30 AA26	W22 AK19 AJ22 AH25 AF21 AE24 AB23	AJ12 AH15 AG18 AE14 AD17 AB13 AA16	Y15 Y13		V11 T11 P11	Y10 W10 U10 R10 N10 M11	Y17 W16 W14 W12 V15 V13 U16 U12 T13 R16 R12 P13 N14 N12 M15 M13	

(1) 47uF @ Vcc_o (bank 0)
requires CFGBVS=high

2 mA quiescent
(1) 47uF @ Vcc_auxio
Vcc_auxio = 1.8V

40 mA power-on current per bank (on top of quies.)

131 mA quiescent
Vcc_aux = 1.8V
(2) 47uF @ Vcc_aux

100 mA power-on current (on top of quiescent)

611 mA quiescent
(2) 680uF @ Vcc_int
Vcc_int = 1V

1400 mA power-on current (on top of quiescent)

VCCBRAM_W20 VCCBRAM_W18 VCCBRAM_V19 VCCBRAM_V17
VCCO_9_Y19 VCCO_9_AC20
VCCO_35_L16 VCCO_35_H15 VCCO_35_E14 VCCO_35_D17 VCCO_35_B13 VCCO_35_A16
VCCO_34_K9 VCCO_34_J12 VCCO_34_G8 VCCO_34_F11 VCCO_34_D7 VCCO_34_C10 VCCO_34_A6
VCCO_33_L6 VCCO_33_J2 VCCO_33_H5 VCCO_33_F1 VCCO_33_E4 VCCO_33_B3
VCCO_13_V25 VCCO_13_U28 VCCO_13_T21 VCCO_13_R24 VCCO_13_P27 VCCO_13_N30
VCCO_12_Y29 VCCO_12_AK29 VCCO_12_AG28 VCCO_12_AD27 VCCO_12_AC30 VCCO_12_AA26
VCCO_11_W22 VCCO_11_AK19 VCCO_11_AJ22 VCCO_11_AH25 VCCO_11_AF21 VCCO_11_AE24 VCCO_11_AB23
VCCO_10_AJ12 VCCO_10_AH15 VCCO_10_AG18 VCCO_10_AE14 VCCO_10_AD17 VCCO_10_AB13 VCCO_10_AA16
VCCO_0_Y15 VCCO_0_Y13
VCCAUX_IO60_V11 VCCAUX_IO60_T11 VCCAUX_IO60_P11
VCCAUX_Y11 VCCAUX_W10 VCCAUX_U10 VCCAUX_R10 VCCAUX_N10 VCCAUX_M11
VCCINT_Y17 VCCINT_W16 VCCINT_W14 VCCINT_W12 VCCINT_V15 VCCINT_V13 VCCINT_U16 VCCINT_U12 VCCINT_T13 VCCINT_R16 VCCINT_R12 VCCINT_P13 VCCINT_N14 VCCINT_N12 VCCINT_M15 VCCINT_M13

SOC-A ZYNQ-XC7Z045-FFG900

GND_A1 GND_A11 GND_A21 GND_AA1 GND_AA10 GND_AA11 GND_AA21 GND_AA5 GND_AB11 GND_AB18 GND_AB28 GND_AB3 GND_AB7 GND_AC1 GND_AC11 GND_AC15 GND_AC25 GND_AC5 GND_AC9 GND_AD11 GND_AD12 GND_AD22 GND_AD3 GND_AD7 GND_AE1 GND_AE11 GND_AE19 GND_AE29 GND_AE5 GND_AE9 GND_AF11 GND_AF16 GND_AF26 GND_AF3 GND_AF7 GND_AG1 GND_AG11 GND_AG13 GND_AG23 GND_AG5 GND_AG9 GND_AH11 GND_AH20 GND_AH3 GND_AH30 GND_AH7 GND_AJ1 GND_AJ11 GND_AJ17 GND_AJ27 GND_AJ5 GND_AJ9 GND_AK11 GND_AK14 GND_AK24 GND_AK3 GND_AK7 GND_B18 GND_B28 GND_B8 GND_C15 GND_C25 GND_C5 GND_D12 GND_D2 GND_D22 GND_E19 GND_E29 GND_E9 GND_F16 GND_F26 GND_F6 GND_G13 GND_G23 GND_G3 GND_H10 GND_H20 GND_H30 GND_J17 GND_J27 GND_J7 GND_K14 GND_K24 GND_K4 GND_L11 GND_L21 GND_M1 GND_M14 GND_M18 GND_M2 GND_M28 GND_M3 GND_M4 GND_M5 GND_M6 GND_M7 GND_M8 GND_M9 GND_N1 GND_N11 GND_N13 GND_N15 GND_N17 GND_N19 GND_N25 GND_N5 GND_N9 GND_P12 GND_P16 GND_P18 GND_P20 GND_P22 GND_P3 GND_P7 GND_R1 GND_R11 GND_R13 GND_R17 GND_R19 GND_R29 GND_R5 GND_T10 GND_T12 GND_T16 GND_T18 GND_T20 GND_T26 GND_T3 GND_T8 GND_U1 GND_U11 GND_U13 GND_U17 GND_U19 GND_U23 GND_U5 GND_V12 GND_V14 GND_V16 GND_V18 GND_V20 GND_V3 GND_V30 GND_V8 GND_W1 GND_W11 GND_W13 GND_W15 GND_W17 GND_W19 GND_W27 GND_W5 GND_Y14 GND_Y16 GND_Y18 GND_Y24 GND_Y3 GND_Y7

programmable logic (PL) power

MGTAVCC = 1V; 489 mA for "4 channels @ 3.125 Gb/s" (which is overkill)
MGTAVTT = 1.2V; 428 mA for "4 channels @ 3.125 Gb/s" (which is overkill)
unused quad supply lines can remain floating (ug476 page 308)

multi-gigabit transceivers (MGT) power

1V0_GTX 1V2_GTX 1V8_AUXIO

(1) 4.7uF @ Vcc_mgta
Vcc_mgta = 1V
CA29 4.7uF 0402

(1) 4.7uF @ Vtt_mgta
Vtt_mgta = 1.2V
CA23 4.7uF 0402
CA22 4.7uF 0402

(1) 4.7uF @ Vcc_mgtaux
Vcc_mgtaux = 1.8V

MGTAVCC_Y8 MGTAVCC_W6 MGTAVCC_U6 MGTAVCC_R6 MGTAVCC_P8 MGTAVCC_N6 MGTAVCC_AJ10 MGTAVCC_AH8 MGTAVCC_AG10 MGTAVCC_AF8 MGTAVCC_AE6 MGTAVCC_AE10 MGTAVCC_AD8 MGTAVCC_AC6 MGTAVCC_AC10 MGTAVCC_AB8 MGTAVCC_AA6
MGTAVTT_Y4 MGTAVTT_W2 MGTAVTT_V4 MGTAVTT_U2 MGTAVTT_T4 MGTAVTT_R2 MGTAVTT_P4 MGTAVTT_N2 MGTAVTT_AK8 MGTAVTT_AK4 MGTAVTT_AJ6 MGTAVTT_AJ2 MGTAVTT_AH4 MGTAVTT_AG6 MGTAVTT_AG2 MGTAVTT_AF4 MGTAVTT_AE2 MGTAVTT_AD4 MGTAVTT_AC2 MGTAVTT_AB4 MGTAVTT_AA2
MGTVCCAUX_V7 MGTVCCAUX_T7

SOC-B ZYNQ-XC7Z045-FFG900

processing system (PS) power

1V8_PLL_PAUX

13 mA quiescent
(1) 100uF @ Vcc_paux
(2) 4.7uF @ Vcc_paux
(3) 0.47uF @ Vcc_paux
Vcc_paux = 1.8V

C18 0.47uF 0402
C19 0.47uF 0402
CA12 4.7uF 0402
CH29 10uF 0603
CD5 100uF 1210

40 mA power-on current (on top of quiescent)

(1) 100uF @ Vcc_mio1
(2) 4.7uF @ Vcc_mio1
(3) 0.47uF @ Vcc_mio1
Vcc_o_mio = 1.8V to 3.3V

(1) 100uF @ Vcc_mio0
(1) 4.7uF @ Vcc_mio0
(2) 0.47uF @ Vcc_mio0
Vcc_o_mio = 1.8V to 3.3V

2V5_MIO 2V5_MIO

C31 0.47uF 0402
CA18 4.7uF 0402
CD9 100uF 1210

C29 0.47uF 0402
CA17 4.7uF 0402
CD8 100uF 1210

1V0_PINT

CD4 100uF 1210

(1) 10uF @ Vcc_pll
(1) 0.47uF @ Vcc_pll
Vcc_pll = 1.8V

1V8_PLL_PAUX

C33 0.47uF 0402
CB6 47uF 1812

DDR_VREF1
DDR_VREF0

1V2_DDR

CD7 100uF 1210

(2) 100uF @ Vcc_ddr
(3) 4.7uF @ Vcc_ddr
(7) 0.47uF @ Vcc_ddr
Vcco_ddr = 1.2V to 1.8V

VCCPINT_U18 VCCPINT_T19 VCCPINT_T17 VCCPINT_R18 VCCPINT_P17 VCCPINT_N16
VCCO_M1_501_K19 VCCO_M1_501_J22 VCCO_M1_501_G18 VCCO_M1_501_C20
VCCO_M0_500_F21 VCCO_M0_500_E24 VCCO_M0_500_B23
VCCPAUX_U20 VCCPAUX_R20 VCCPAUX_P19 VCCPAUX_N20
VCCPLL_N18
DDR_VREF1_502 DDR_VREF0_502
VCCO_DDR502_M23 VCCO_DDR502_L26 VCCO_DDR502_K29 VCCO_DDR502_H25 VCCO_DDR502_G28 VCCO_DDR502_D27 VCCO_DDR502_C30 VCCO_DDR502_A26

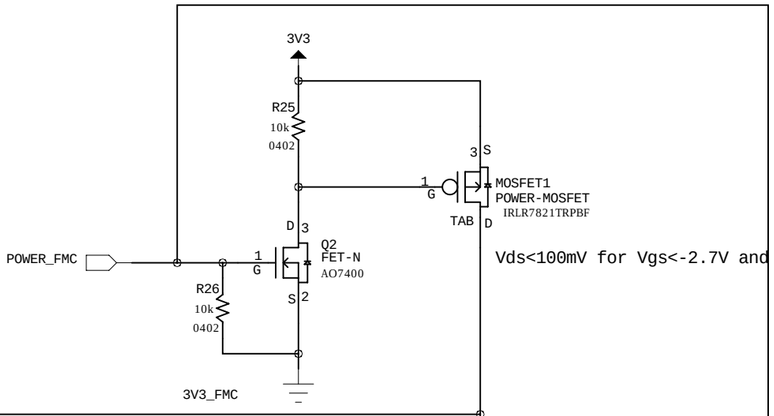
SOC-C ZYNQ-XC7Z045-FFG900

122 mA quiescent
(1) 100uF @ Vcc_pint
(3) 4.7uF @ Vcc_pint
(5) 0.47uF @ Vcc_pint
Vcc_pint = 1V

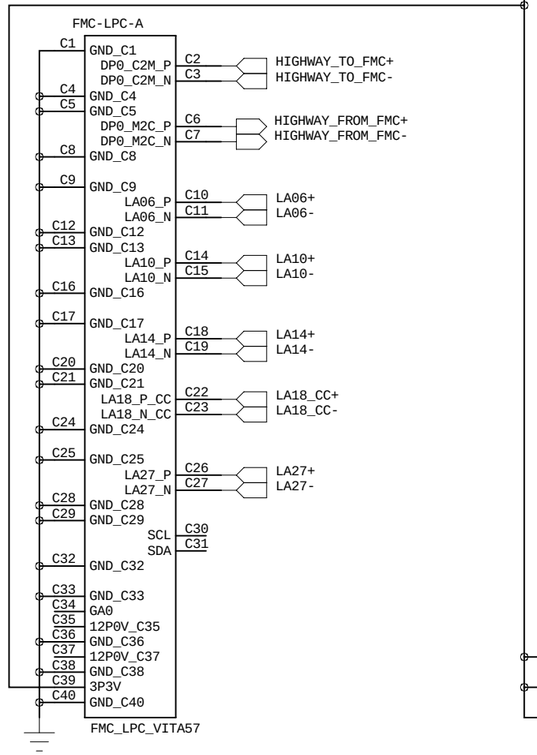
70 mA power-on current (on top of quiescent)

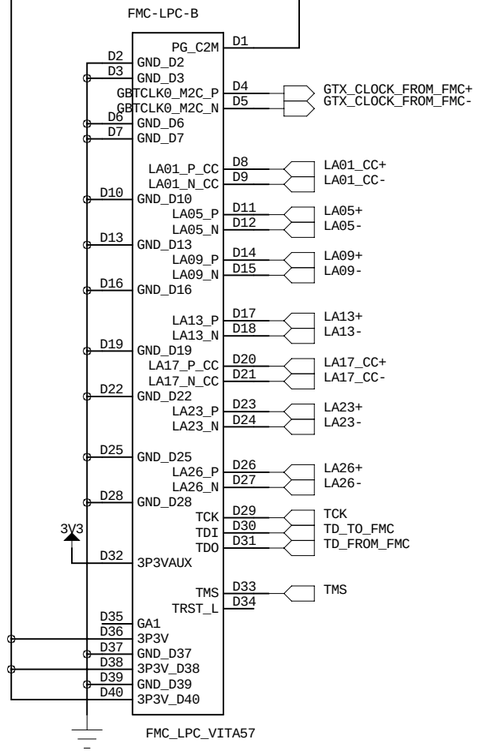
130 mA power-on current per bank (on top of quiescent)

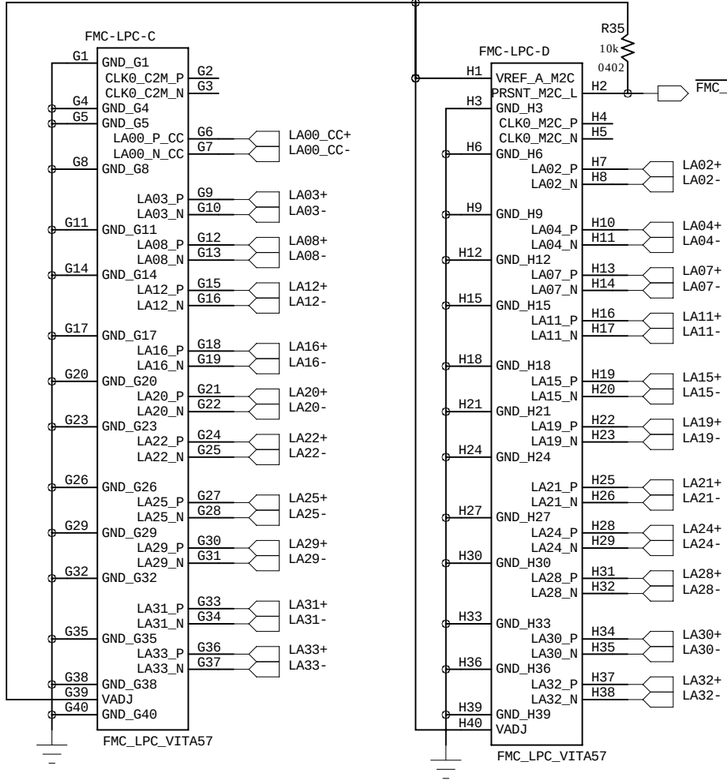
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	B
IDLAB design #:	IDL_14_002
circuit design:	MZA, JLB, KAN, KRO, GV, BK, LW
PCB design:	MZA
sheet #:	5 of 11
sheet description:	FPGA_POWER
date last modified:	2014-08-01

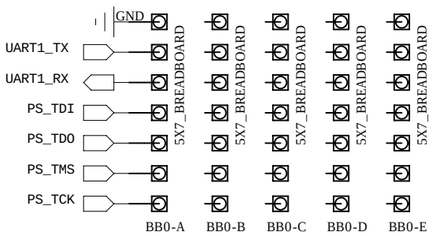


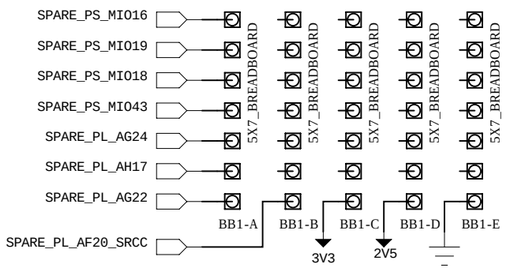
Vds<100mV for Vgs<-2.7V and Id<-2.1A



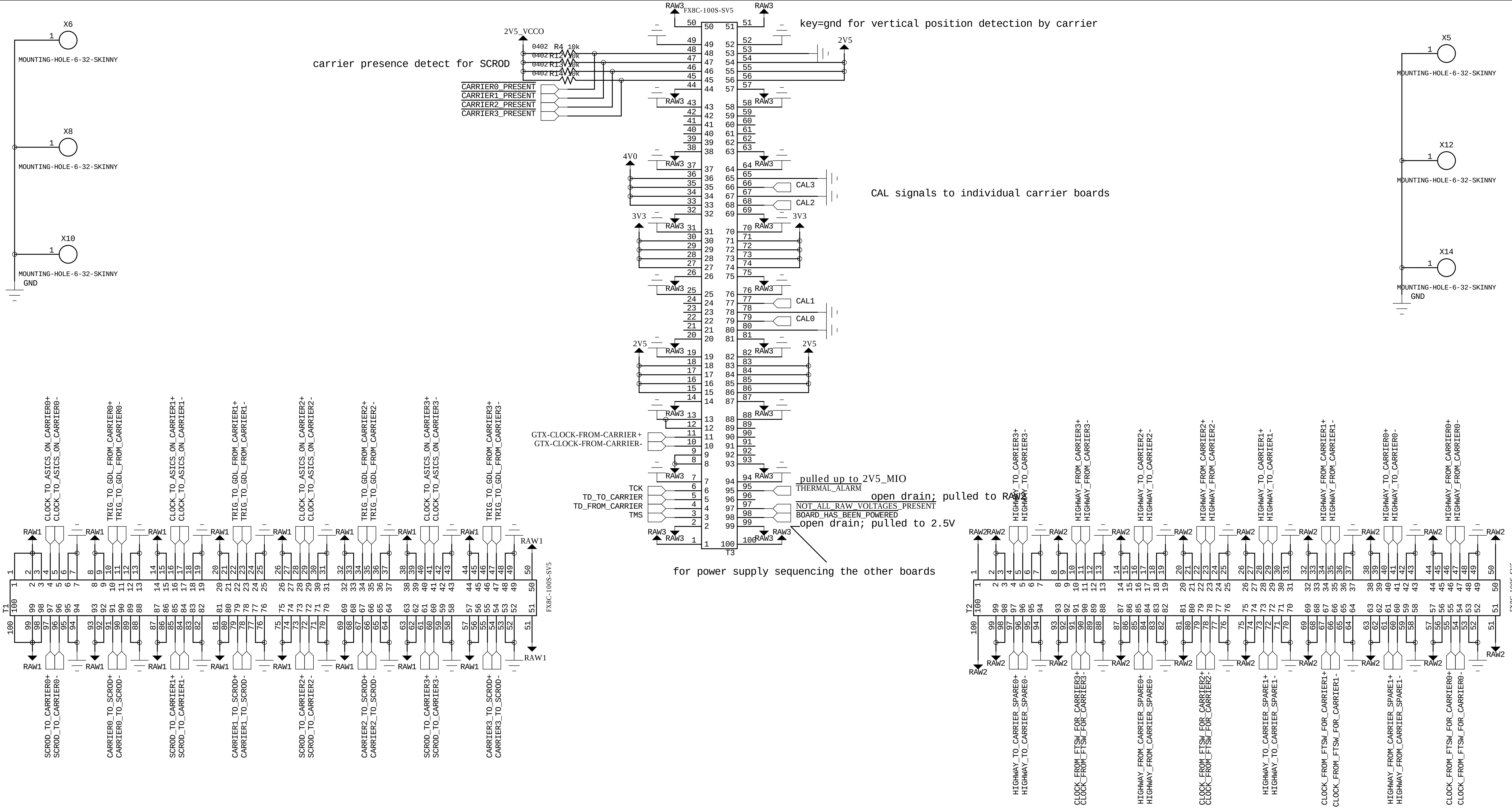




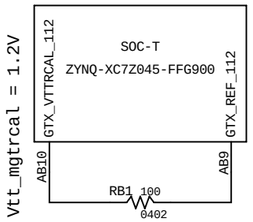




institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	B
IDLAB design #:	IDL_14_002
circuit design:	MZA, JLB, KAN, KRO, GV, BK, LW
PCB design:	MZA
sheet #:	6 of 11
sheet description:	FMC_LPC_CONNECTOR_BREADBOARD
date last modified:	2014-08-01


key=gnd for vertical position detection by carrier
carrier presence detect for SCROD
CARRIER0_PRESENT
CARRIER1_PRESENT
CARRIER2_PRESENT
CARRIER3_PRESENT
CAL signals to individual carrier boards
CAL3
CAL2
CAL1
CAL0
GTX-CLOCK-FROM-CARRIER+
GTX-CLOCK-FROM-CARRIER-
TCK
TD_TO_CARRIER
TD_FROM_CARRIER
TMS
pulled up to 2V5_MIO
THERMAL_ALARM
open drain; pulled to RAW2
NOT_ALL_RAW_VOLTAGES_PRESENT
BOARD_HAS_BEEN_POWERED
open drain; pulled to 2.5V
for power supply sequencing the other boards
FX8C-100S-SV5
MOUNTING-HOLE-6-32-SKINNY
GND
2V5_VCCO
4V0
3V3
2V5
RAW1
RAW2
RAW3
T1
T2
T3
X5
X6
X8
X10
X12
X14
CLOCK_TO_ASICS_ON_CARRIER0+
CLOCK_TO_ASICS_ON_CARRIER0-
TRIG_TO_GDL_FROM_CARRIER0+
TRIG_TO_GDL_FROM_CARRIER0-
SCROD_TO_CARRIER0+
SCROD_TO_CARRIER0-
CARRIER0_TO_SCROD+
CARRIER0_TO_SCROD-
HIGHWAY_TO_CARRIER0+
HIGHWAY_TO_CARRIER0-
HIGHWAY_FROM_CARRIER0+
HIGHWAY_FROM_CARRIER0-
HIGHWAY_TO_CARRIER_SPARE0+
HIGHWAY_TO_CARRIER_SPARE0-
HIGHWAY_FROM_CARRIER_SPARE0+
HIGHWAY_FROM_CARRIER_SPARE0-
CLOCK_FROM_FTSW_FOR_CARRIER0+
CLOCK_FROM_FTSW_FOR_CARRIER0-

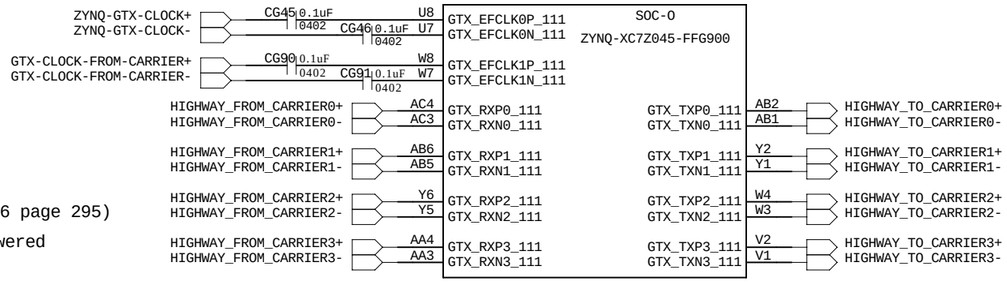
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	B
IDLAB design #:	IDL_14_002
circuit design:	MZA, JLB, KAN, KRO, GV, BK, LW
PCB design:	MZA
sheet #:	7 of 11
sheet description:	BOARD_TO_BOARD_CONNECTORS
date last modified:	2014-08-01



these two traces must be equal length (ug476 page 295)

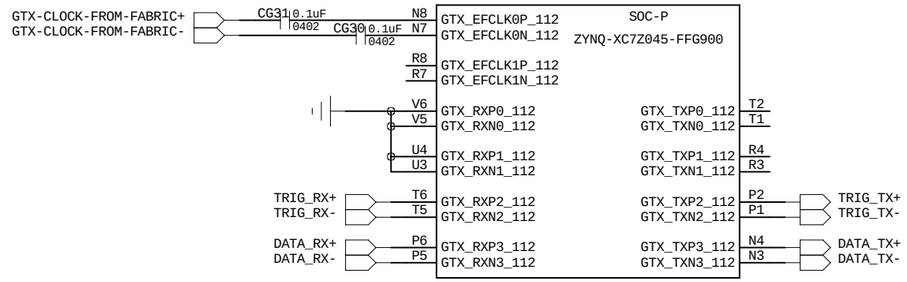
ug476 page 294 says quad/bank 112 must be powered

gigabit connections between SCROD and each carrier board



gigabit connections to backend HSLB and FMC daughtercard

GTX clock must be AC coupled through 100nF caps (ug476 page 307)



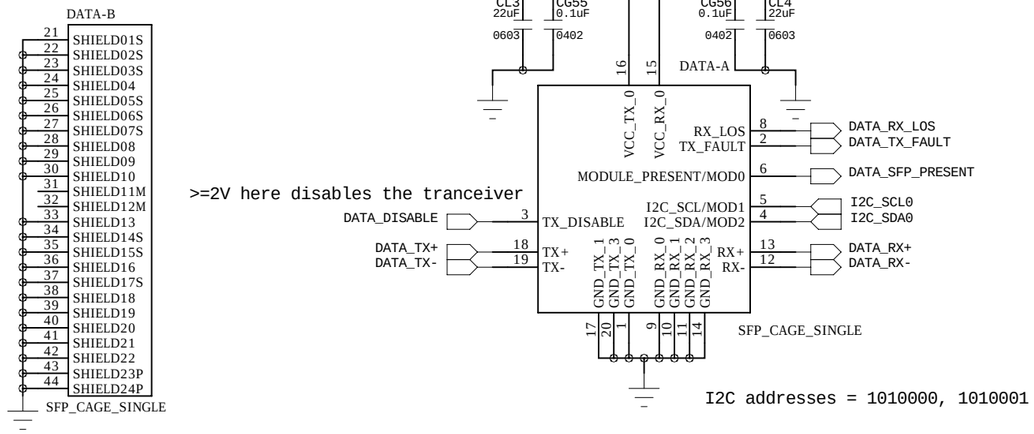
note: GTX clocks from 110 can be used on the 111; clocks from 112 can be used on the 111; but 110 clocks can't be used on the 112 and vice versa

GTX clocks via fabric are not recommended due to noise on VccINT and VccAUX
http://www.xilinx.com/support/answers/53500.htm

each AFBR-57D7APZ uses 235mA

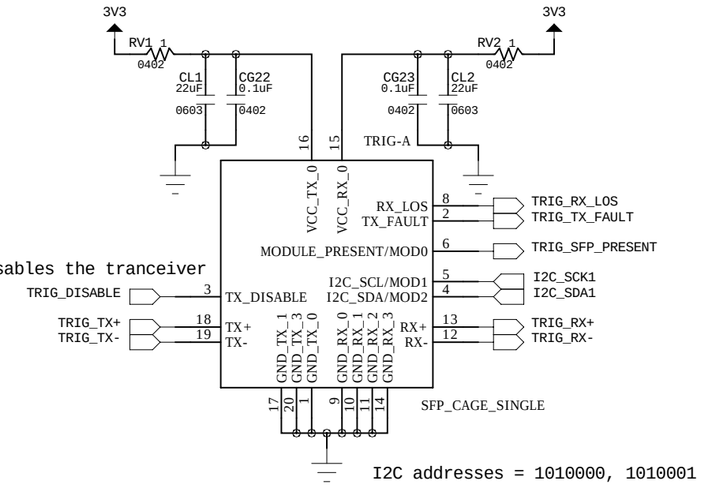
trig_present and data_present need PULLUP enabled in FPGA

data_tx_fault and trig_tx_fault need PULLUP enabled in FPGA



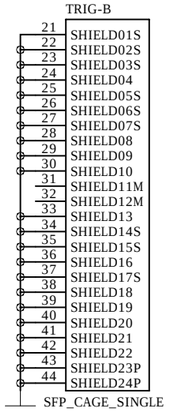
>=2V here disables the tranceiver

I2C addresses = 1010000, 1010001

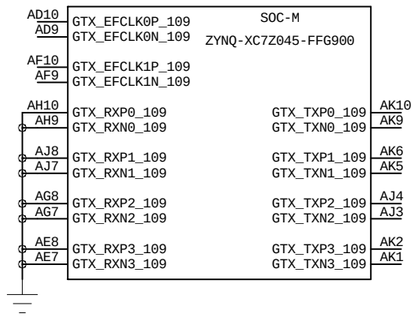


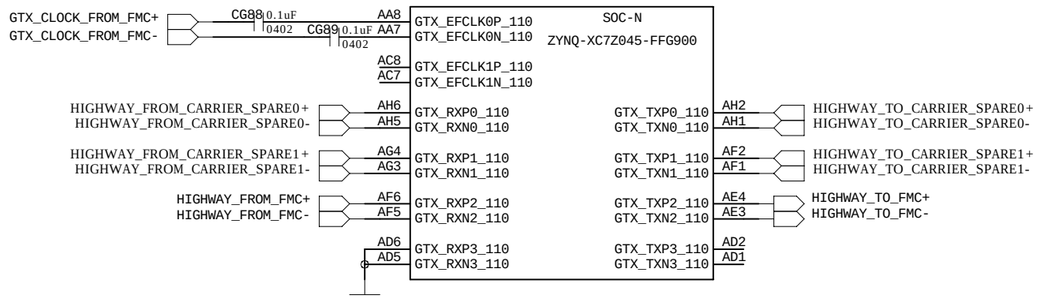
>=2V here disables the tranceiver

I2C addresses = 1010000, 1010001



ug476 page 304 says we should leave unused gtx clock inputs floating





institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	B
IDLAB design #:	IDL_14_002
circuit design:	MZA, JLB, KAN, KRO, GV, BK, LW
PCB design:	MZA
sheet #:	8 of 11
sheet description:	FIBER_OPTIC_TRANSCEIVERS
date last modified:	2014-08-01

CFGBVS determines JTAG voltage (ug470 page 22)
configuration (bank 0) voltage is 2.5V

all 0.1uF 0402

might hard solder this connection

L=LVDS

H=Header

M=Multiplexer

F=FPGA

JTAG_SEL must be LVDS when 14 pin header not connected
ds593 page 16 suggests this hookup

sneaky place for the 17th analog input...

Vcc_adc = 1.8V @ 25 mA
ug480 page 13; short vrefp to gnd to use internal reference

2V terminated into 50 Ohms = 80 mW

5V terminated into two 10k = 5 mW each

5 V terminated into 50 Ohms = 500 mW

2V terminated into 50 Ohms = 80 mW

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	B
IDLAB design #:	IDL_14_002
circuit design:	MZA, JLB, KAN, KRO, GV, BK, LW
PCB design:	MZA
sheet #:	9 of 11
sheet description:	JTAG_MISCELLANEOUS
date last modified:	2014-08-01

VIO and VCC must come up at the same time for these parts
ug585 page 342 says only up to 128Mbit devices are supported, although a 256Mbit part would fit on the board...

data fiber transceiver also on this i2c chain

I2C address = 1001010

I2C address = 1010100

I2C address = 1000000

trig fiber transceiver also on this i2c chain

ug585 page 647 says this will clear the PL configuration

12mA@3.3V, 30mA@1.8V, 6mA@IOV

ug933 page 62 says LPDDR2 does not require termination

ug585 page 256/257 : bank, ras, cas, we, reset signals not used in LPDDR2?

VDD1 = 1.8V; all else are 1.2V

VDD1 needs 20 mA

VDD2 needs 210 mA peak

VDDCA + VDDQ need 28 mA combined

ug585 page 273 says the zynq can generate the vrefs for the LPDDR2 RAM
resistive dividers are for when that doesn't work
ug585 pages 271 and 614 say LPDDR2 ram does not need a termination resistor

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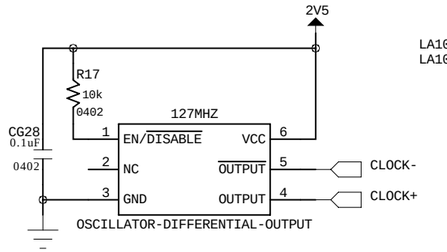
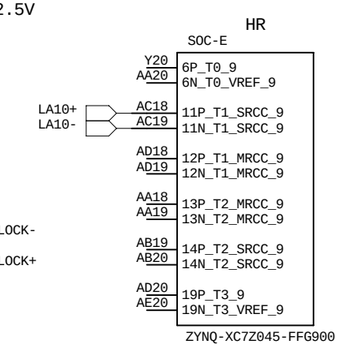
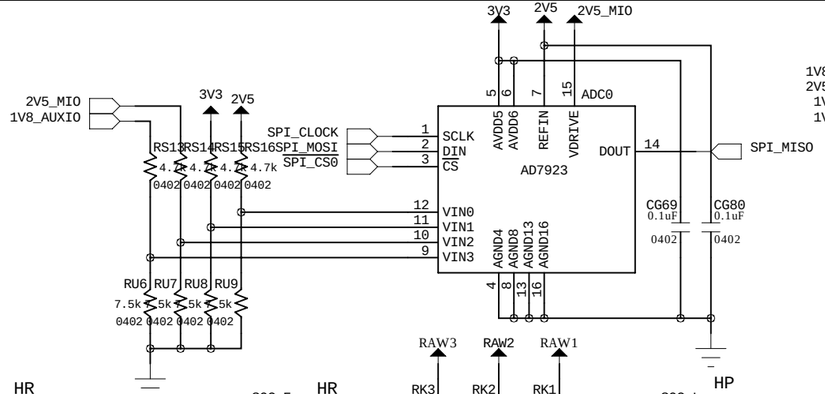
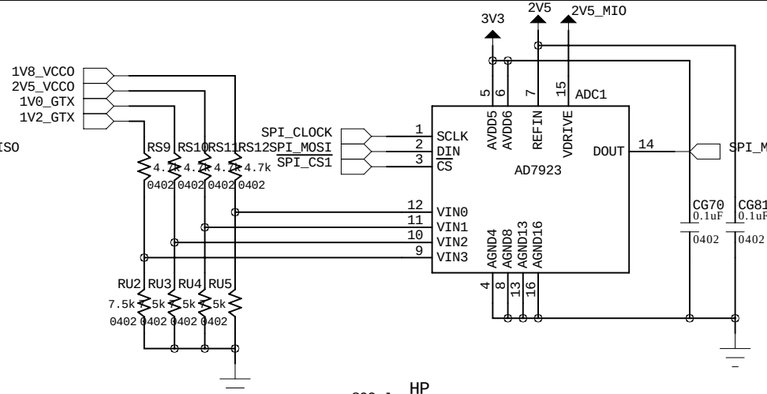
title:	SCROD
revision:	B
IDLAB design #:	IDL_14_002
circuit design:	MZA, JLB, KAN, KRO, GV, BK, LW
PCB design:	MZA
sheet #:	10 of 11
sheet description:	PS_CONNECTIONS_ARM_IIC_RAM_FLASH
date last modified:	2014-08-01

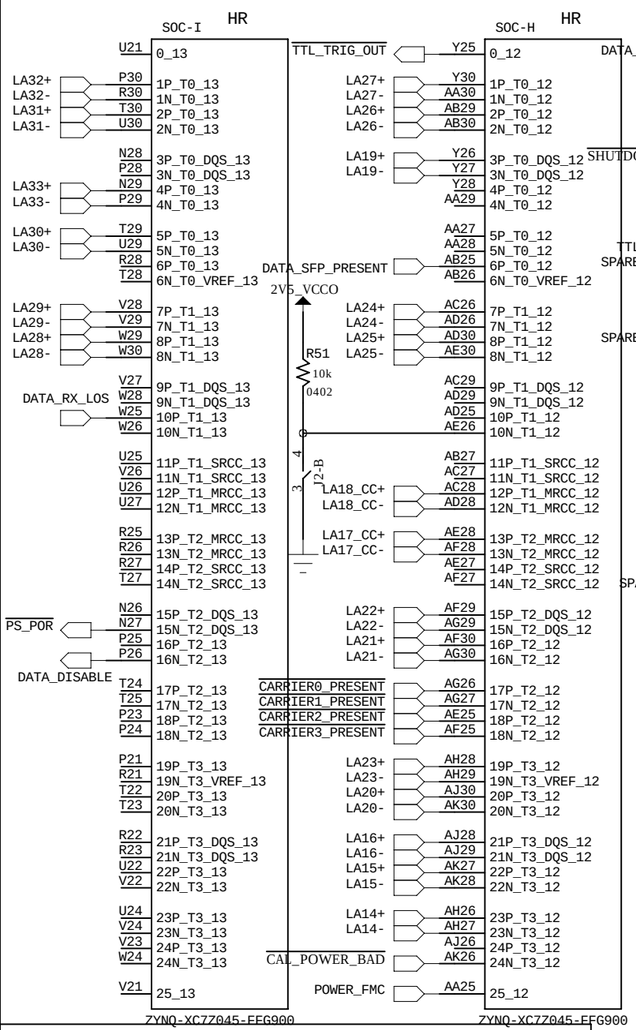
banks 13,33,34,35 are 1.8V; the rest are 2.5V











institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	B
IDLAB design #:	IDL_14_002
circuit design:	MZA, JLB, KAN, KRO, GV, BK, LW
PCB design:	MZA
sheet #:	11 of 11
sheet description:	PL_CONNECTIONS_FPGA_ANALOG_INPUT
date last modified:	2014-08-01

ug480 page 21 says Vccint, Vccaux, Vccbram, Vccpint, Vccpaux, Vccddr are monitored internally