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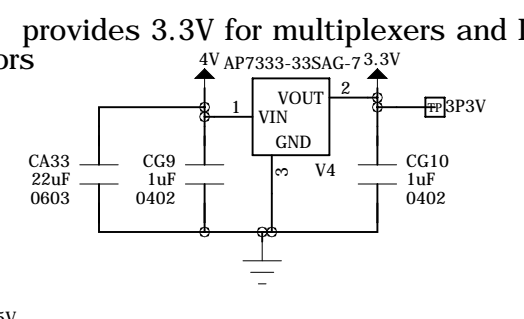
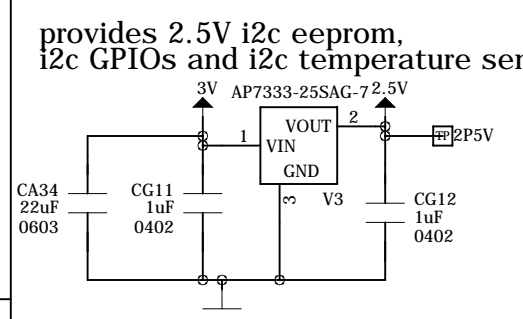
E

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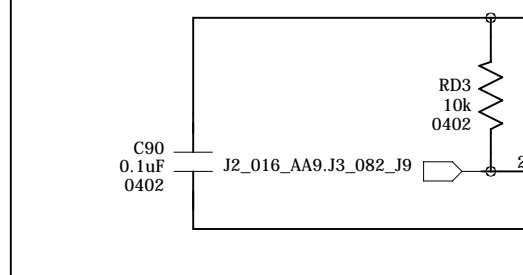
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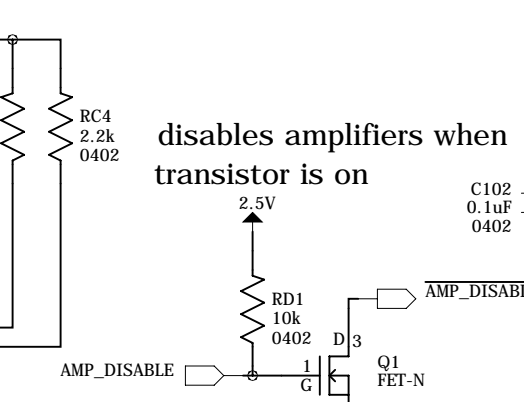
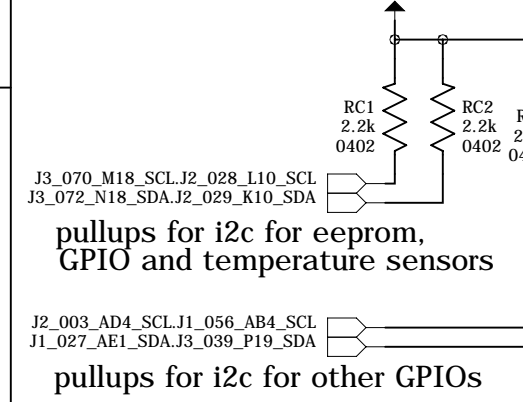
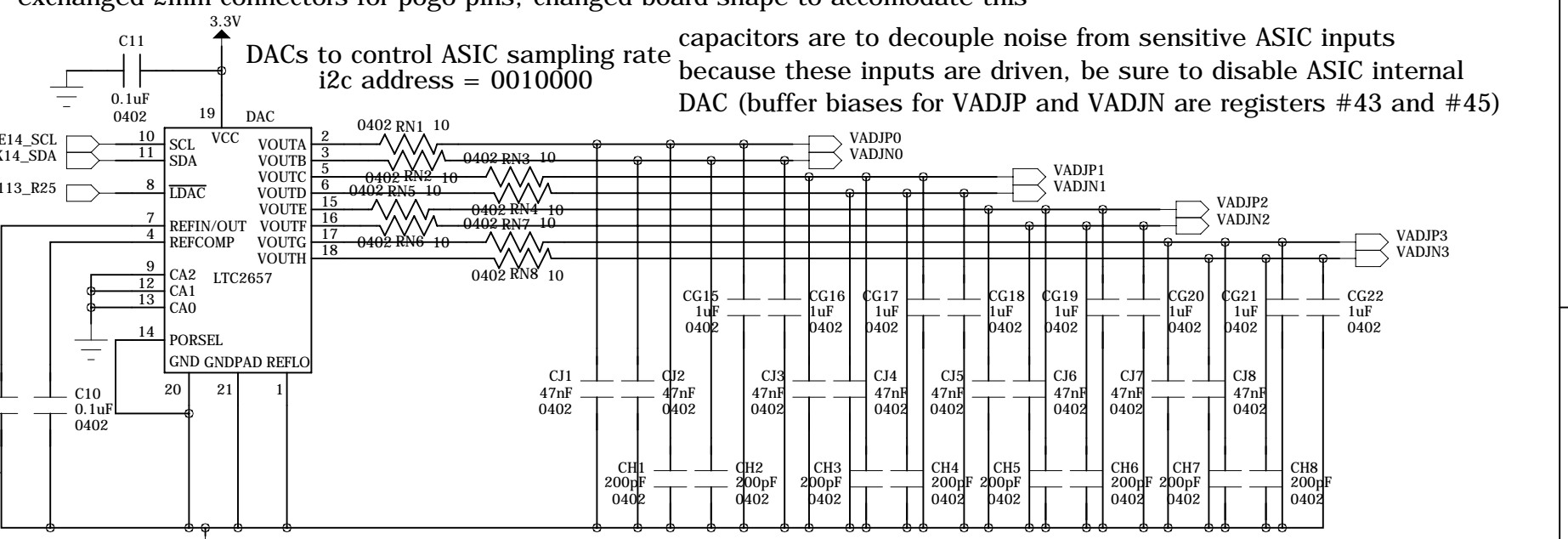
2013-11 notes / changes since revB:
added 10 Ohm series resistors between external DAC and ASIC pins
changed capacitance for external DACs to be 1uF+47nF+200pF
connected 3V and 5V nets to bottom connectors (so only one power connector should be necessary per stack)
exchanged SMA connectors for MMCX
exchanged ltc2637 for ltc2657
used lt1963a with a shutdown and wired shutdowns to be active on power-up (controllable via I2C)
changed to LMH6629 amplifier
the RJ resistors are 50 Ohms; the RF resistors are 20k, yeilding a supposed voltage gain of 400 (compared to 15=6k/400)
the CE resistors are 1nF instead of 100nF

2013-11-15 notes / changes since revC:
added LT1529 5V regulator (need to provide ~6V to board now; repurposed FPGA's J16 as a shutdown pin for this)
exchanged 2mm connectors for pogo pins; changed board shape to accomodate this

capacitors are to decouple noise from sensitive ASIC inputs
because these inputs are driven, be sure to disable ASIC internal DAC (buffer biases for VADJP and VADJN are registers #43 and #45)

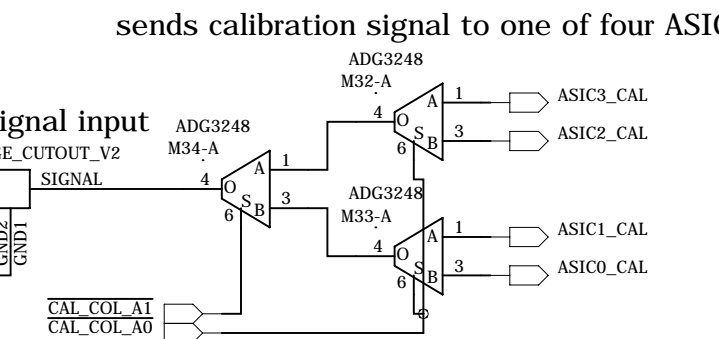
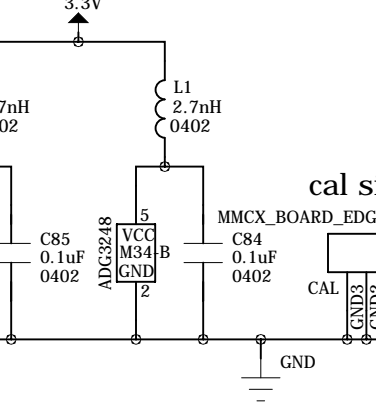
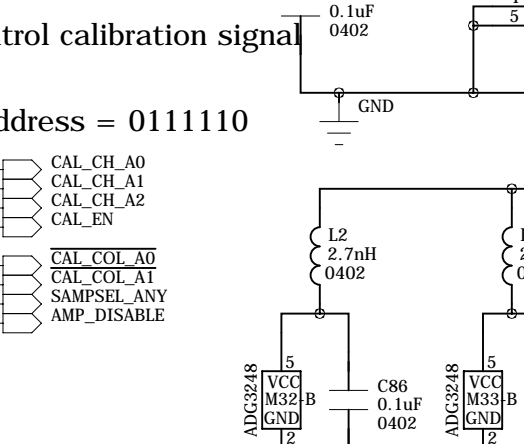
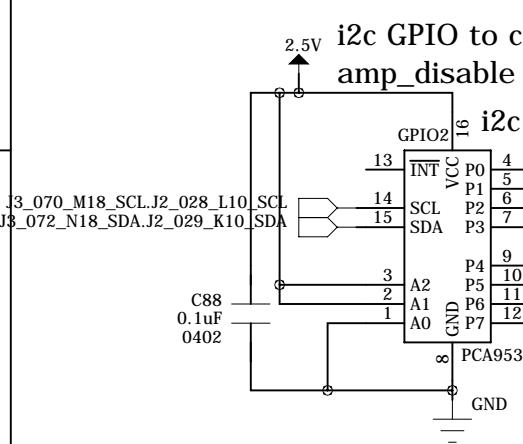
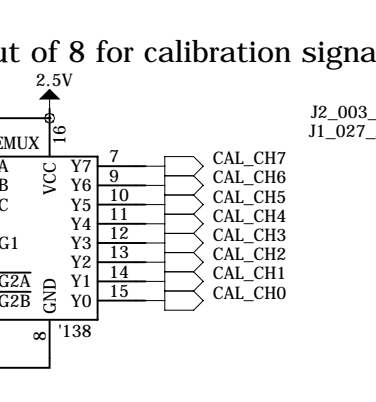
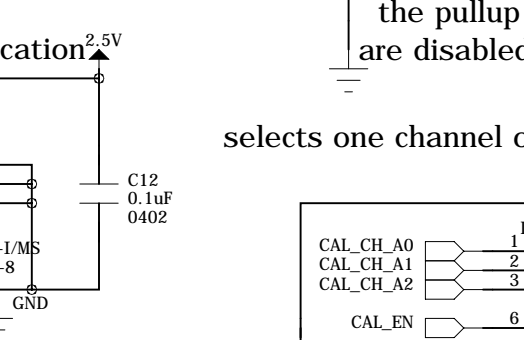
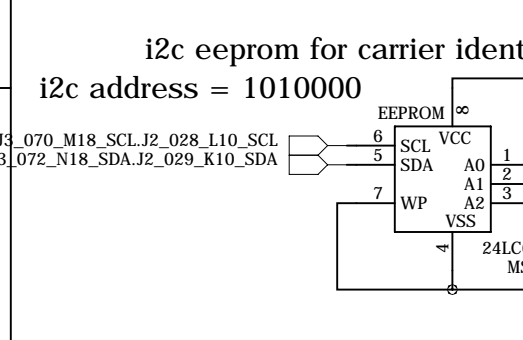


disables DOE by default
ensures all four DOE (active high) signals are not driven during FPGA high-impedance mode

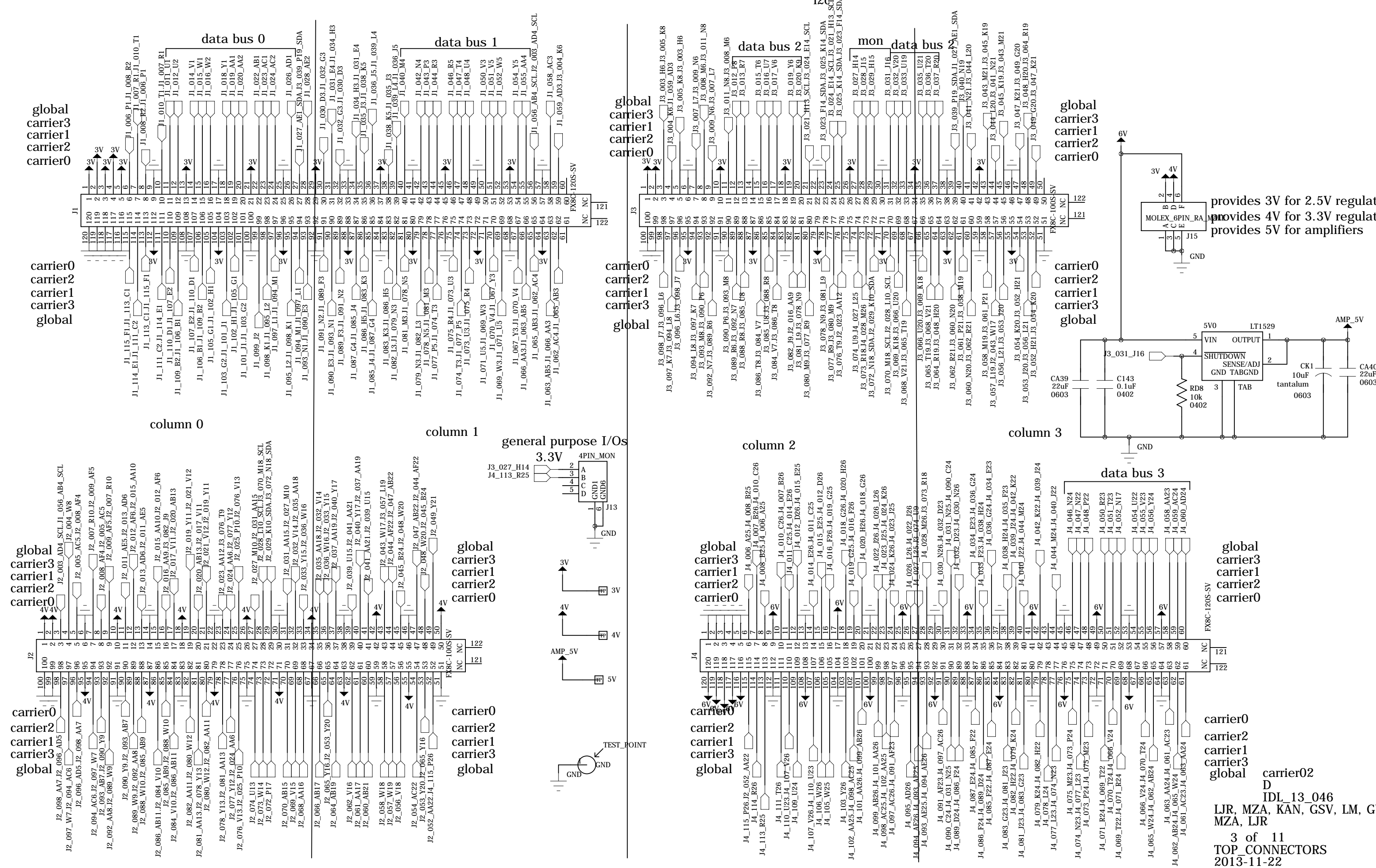


disables amplifiers when transistor is on

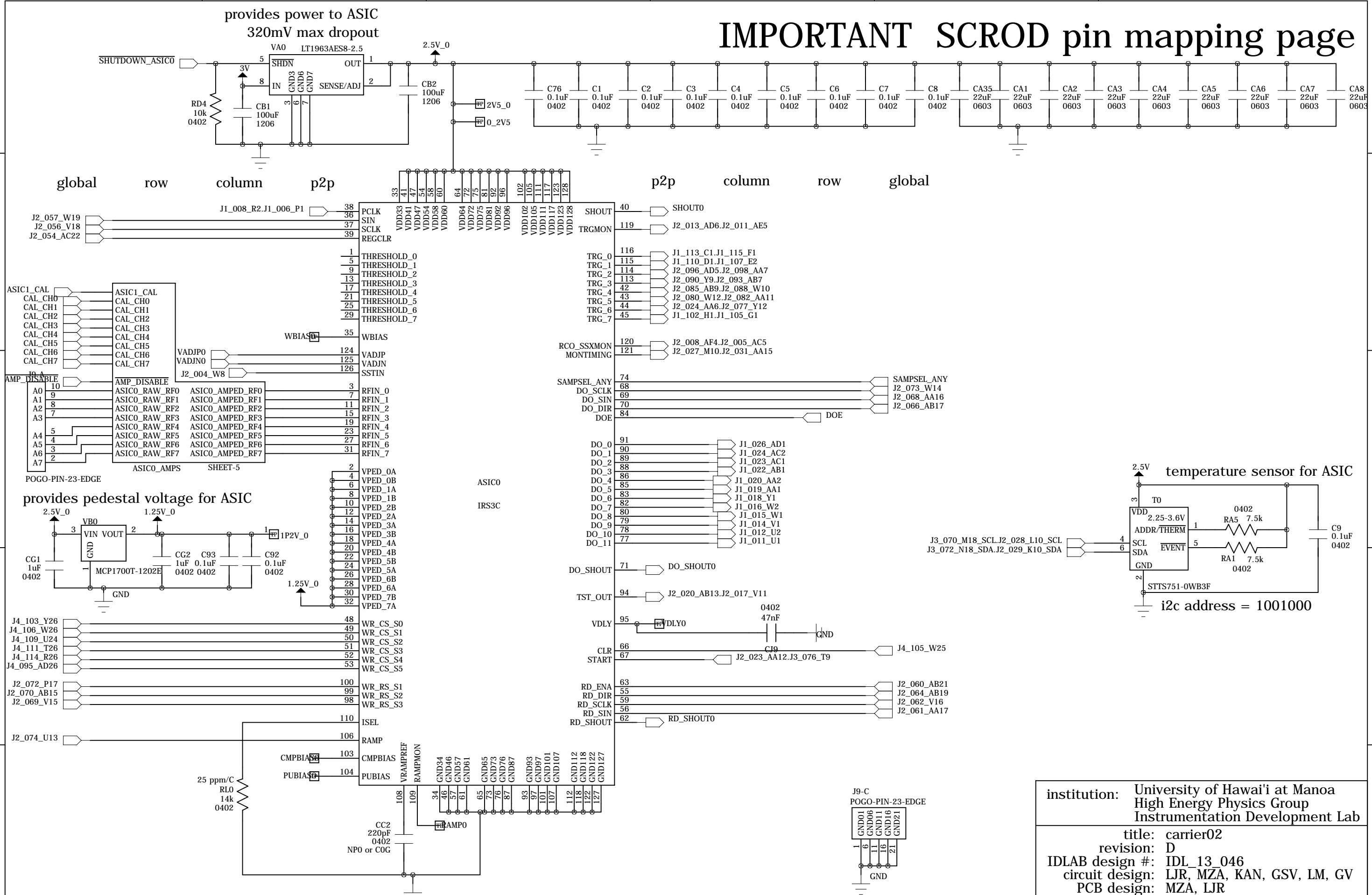
the pullup is so the amps are disabled by default



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	D
IDLAB design #:	IDL_13_046
circuit design:	LJR, MZA, KAN, GSV, LM, GV
PCB design:	MZA, LJR
sheet #:	1 of 11
sheet description:	POWER_CAL_I2C_FET_DAC_GPIO_EPROM
date last modified:	2013-11-22



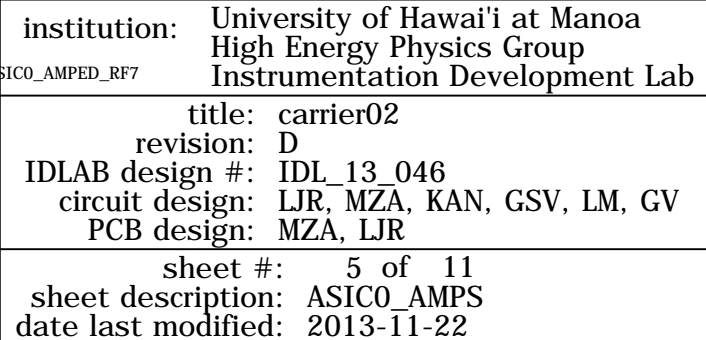
IMPORTANT SCROD pin mapping page



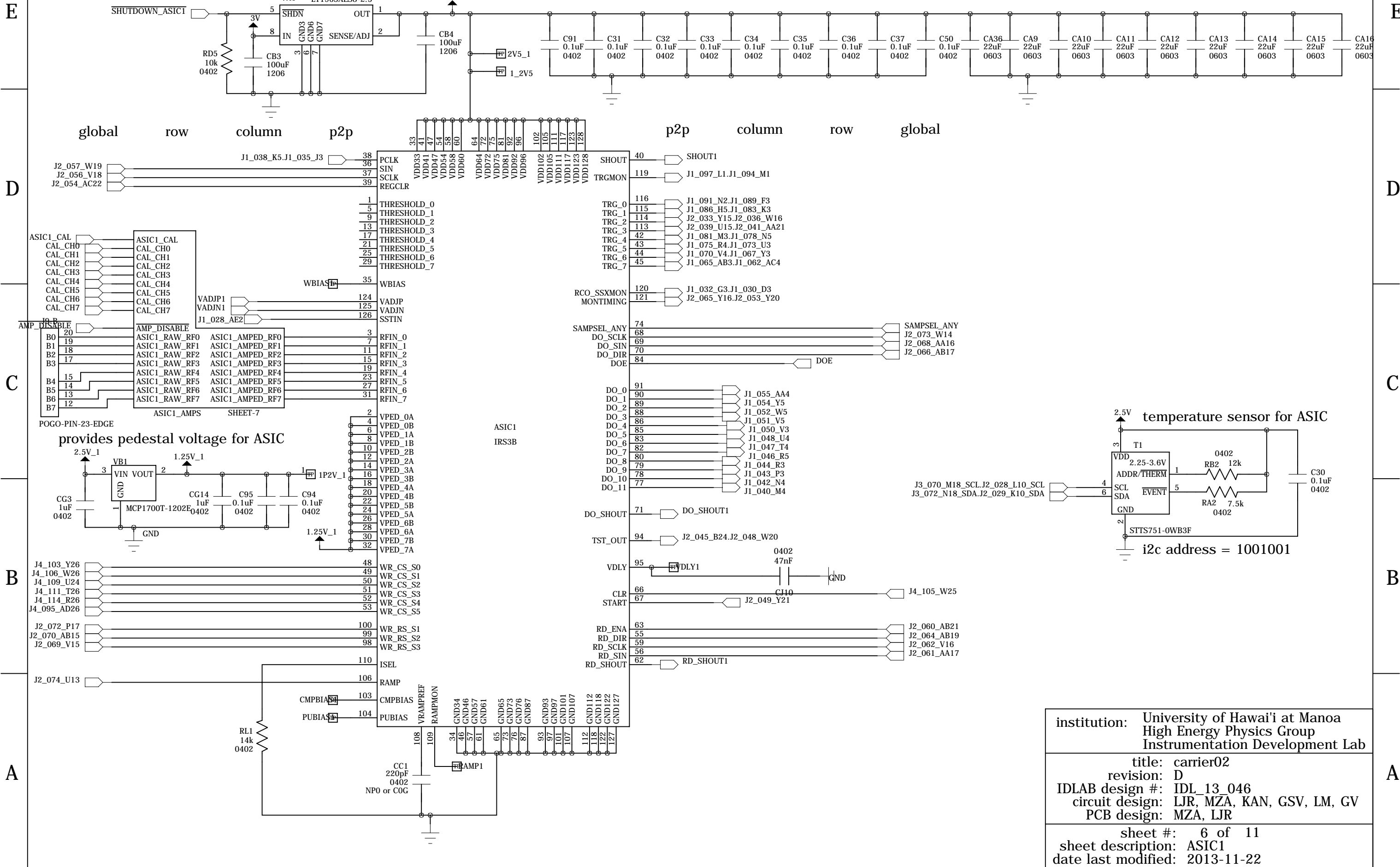
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
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title:	carrier02
revision:	D
IDLAB design #:	IDL_13_046
circuit design:	LJR, MZA, KAN, GSV, LM, GV
PCB design:	MZA, LJR

sheet #:	4 of 11
sheet description:	ASIC0
date last modified:	2013-11-22



IMPORTANT SCROD pin mapping page



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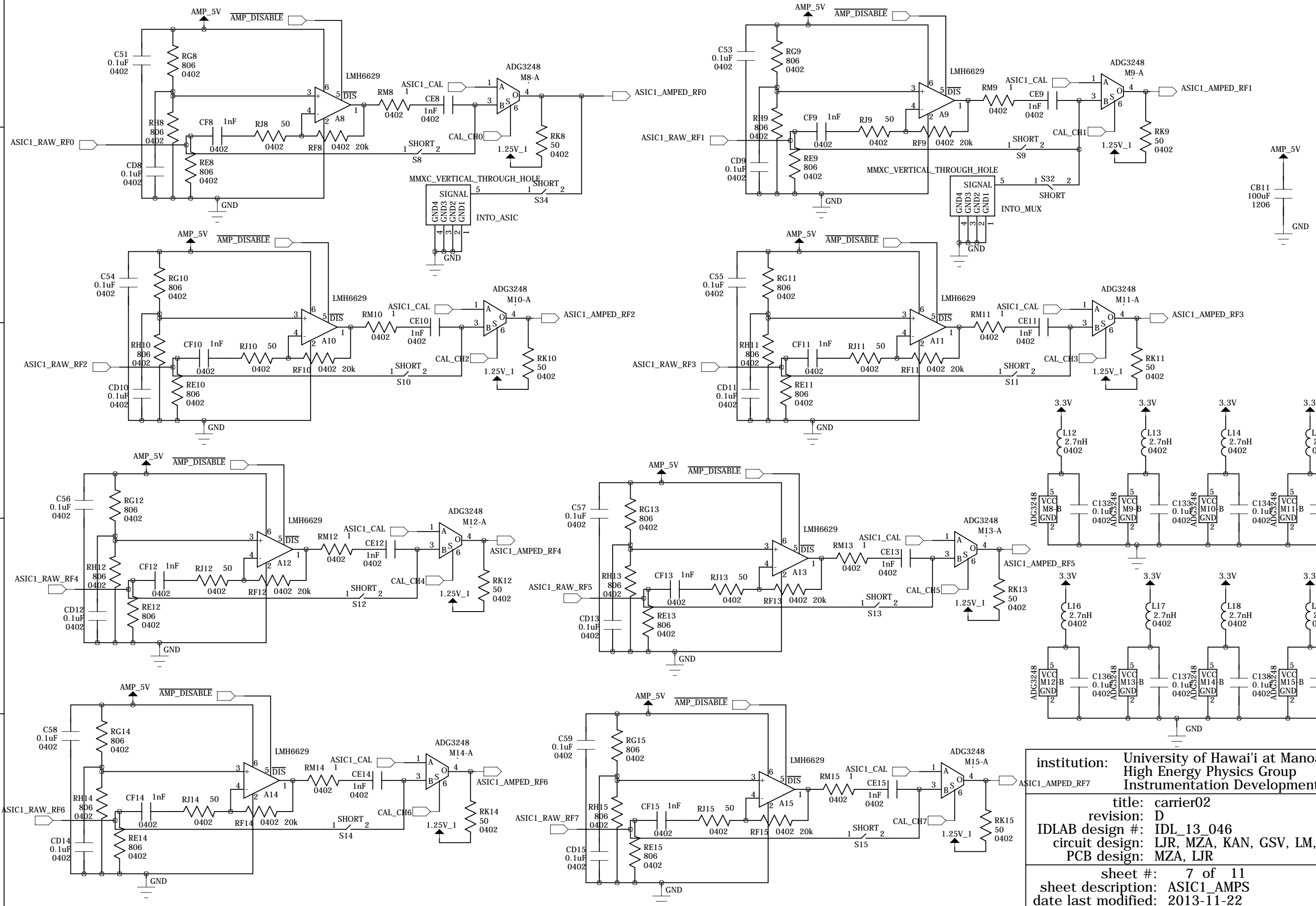
E

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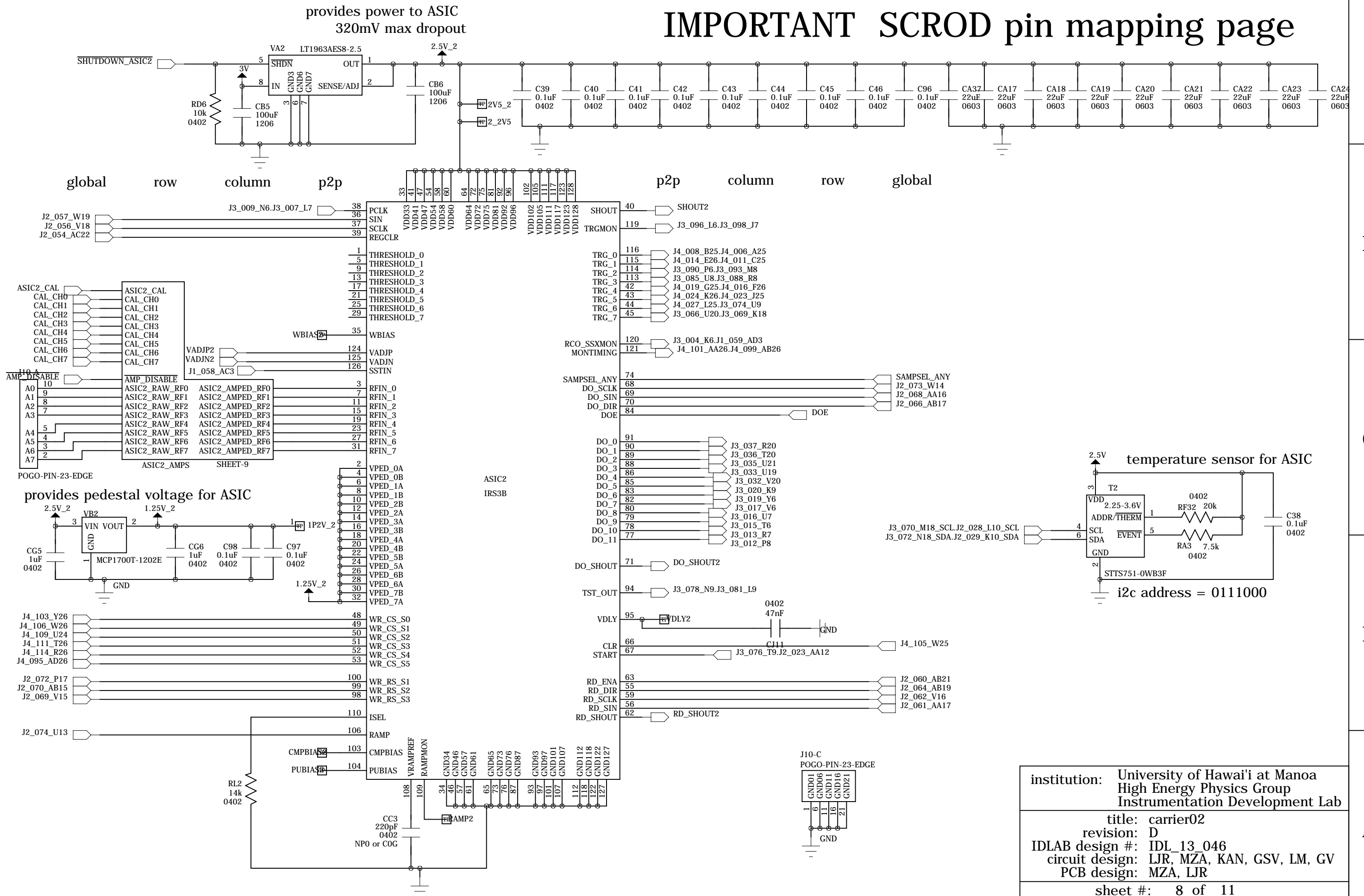
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IMPORTANT SCROD pin mapping page



institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

title:	carrier02
revision:	D
IDLAB design #:	IDL_13_046
circuit design:	LJR, MZA, KAN, GSV, LM, GV
PCB design:	MZA, LJR

sheet #: 8 of 11
sheet description: ASIC2
date last modified: 2013-11-22

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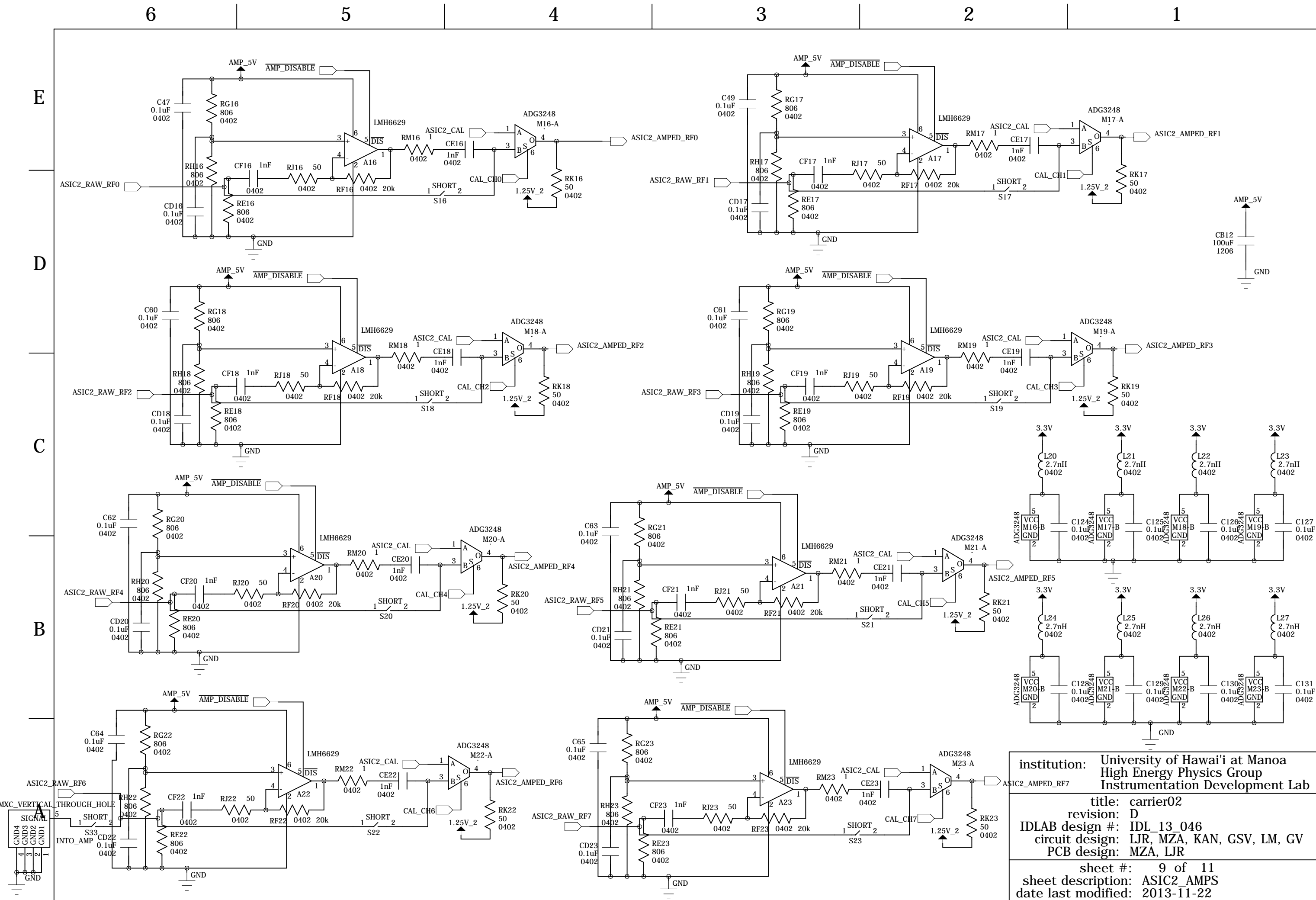
C

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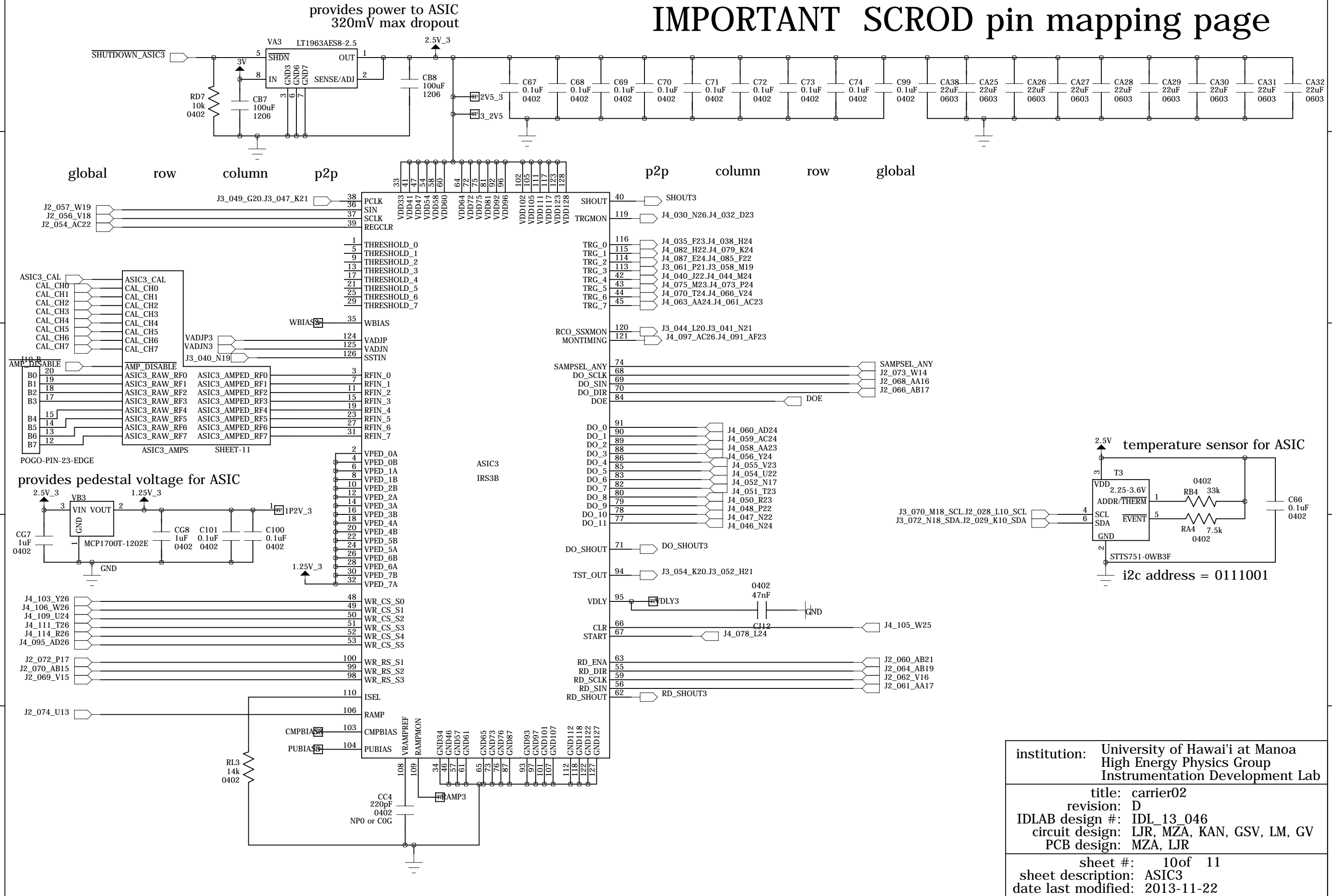
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IMPORTANT SCROD pin mapping page



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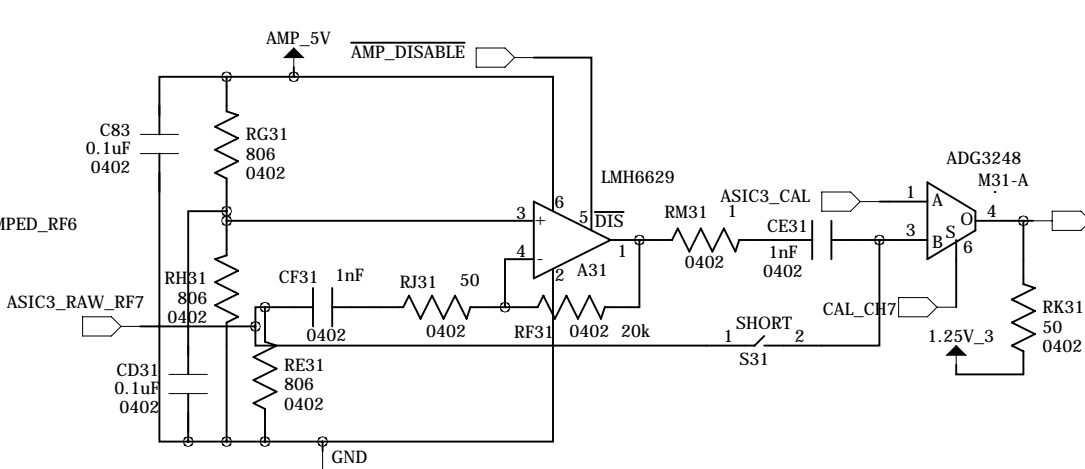
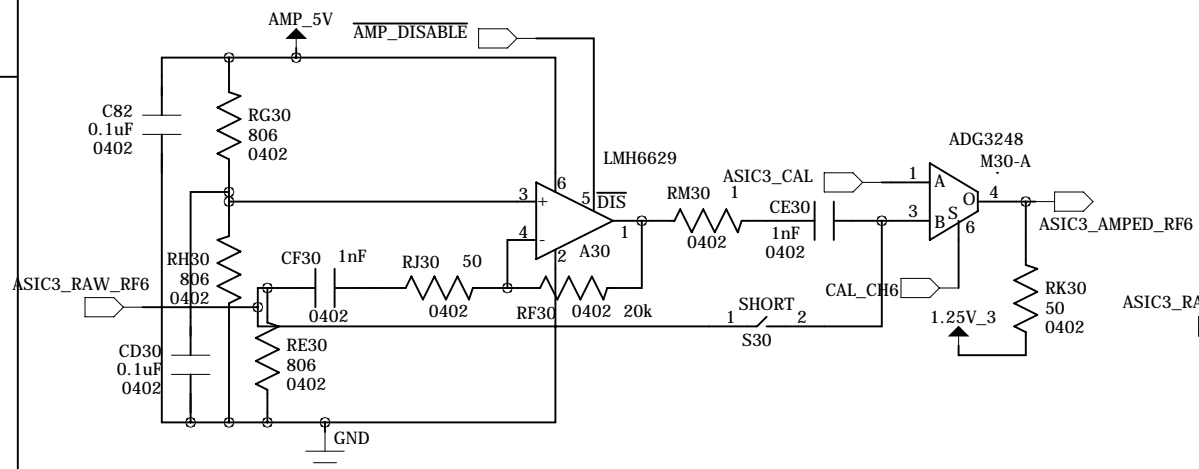
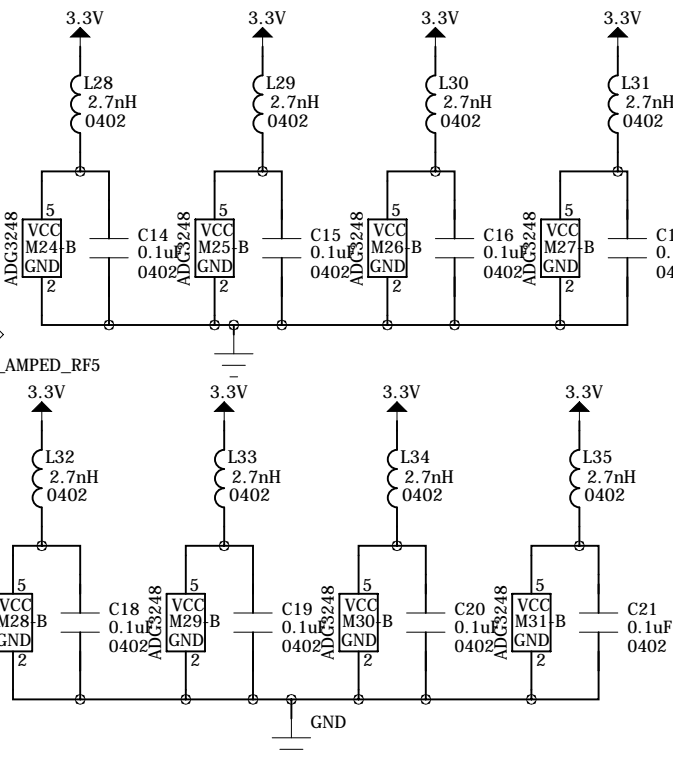
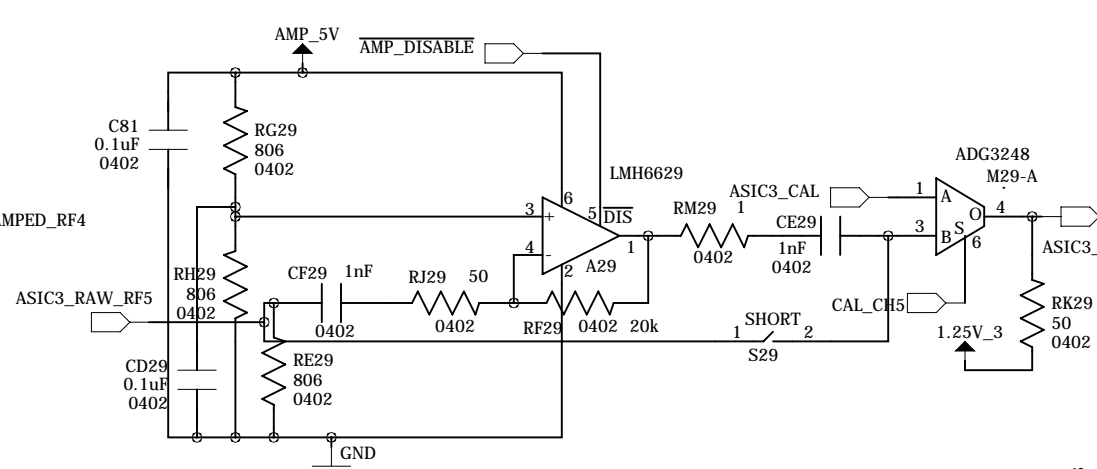
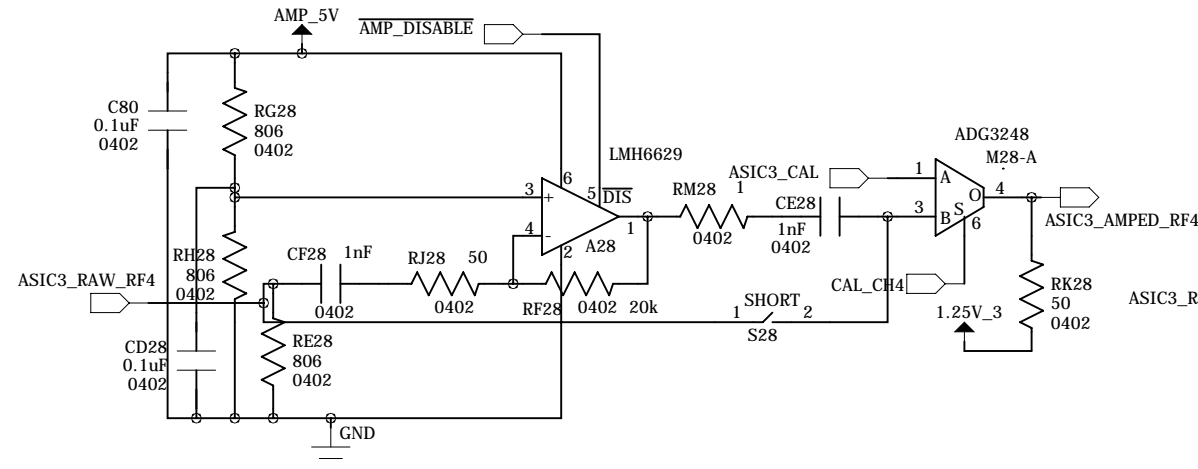
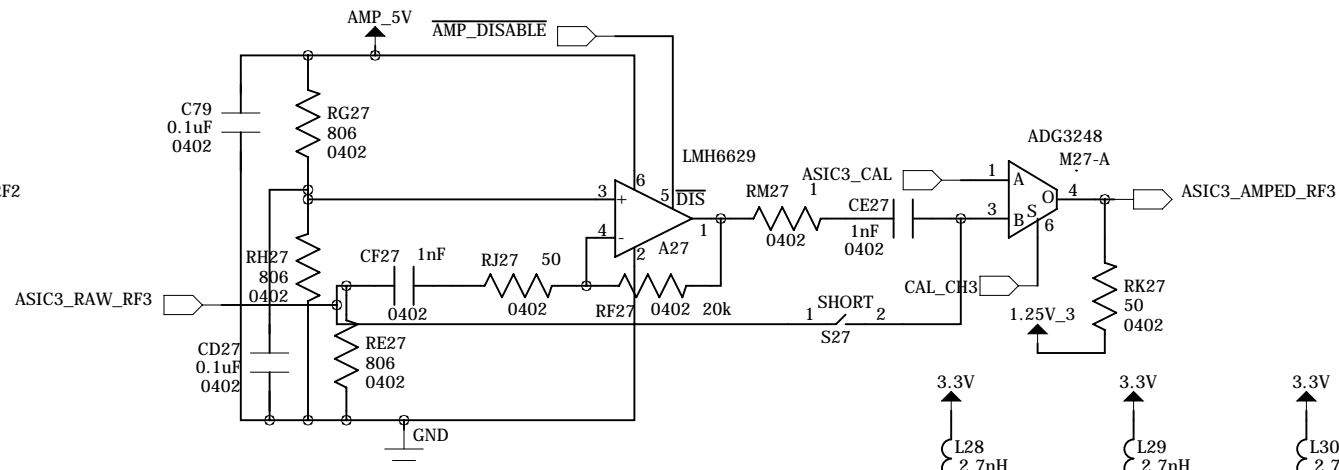
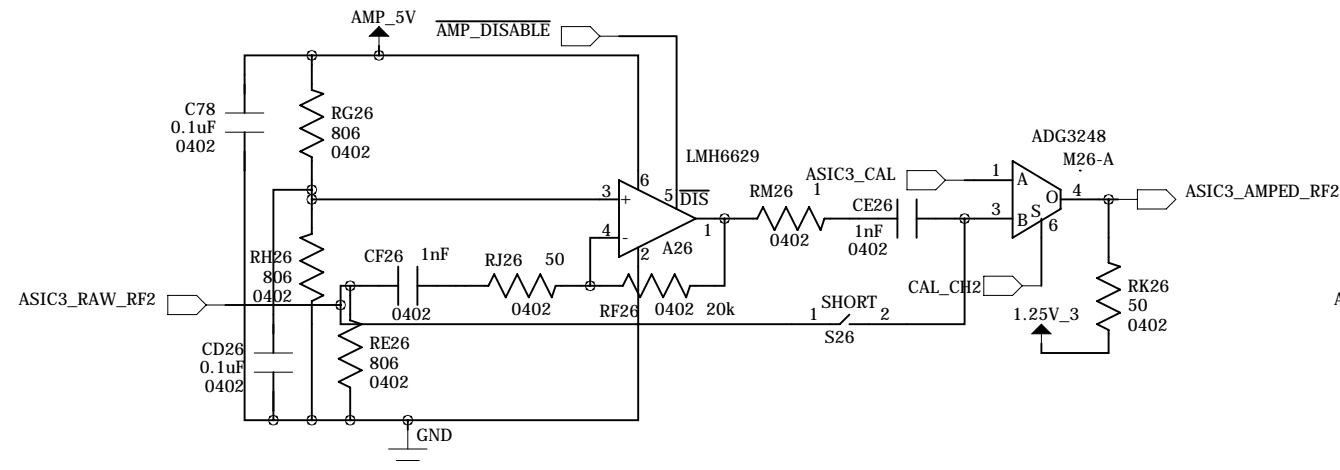
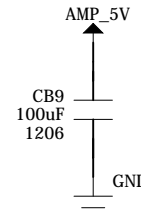
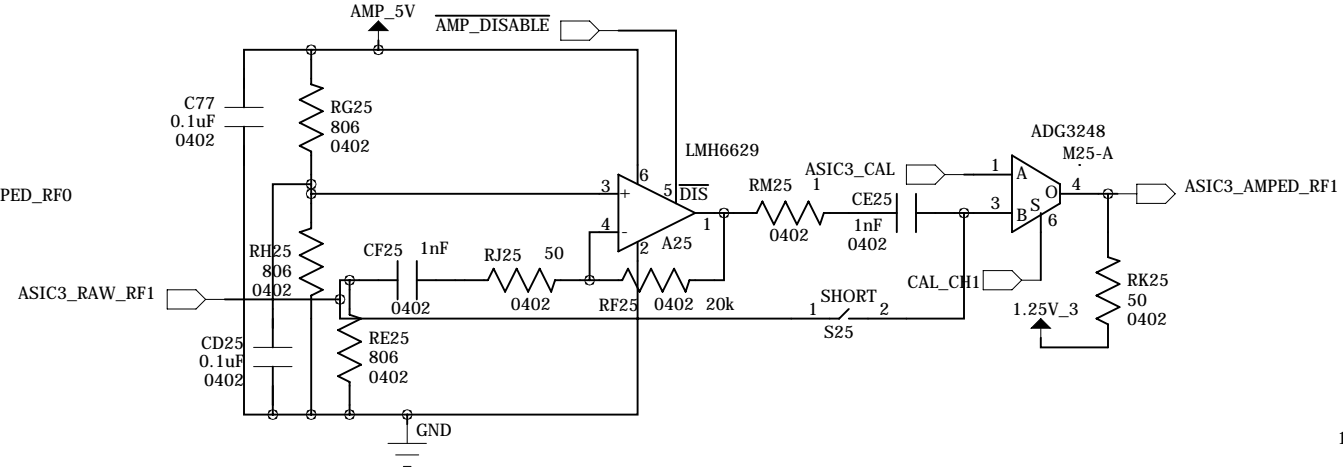
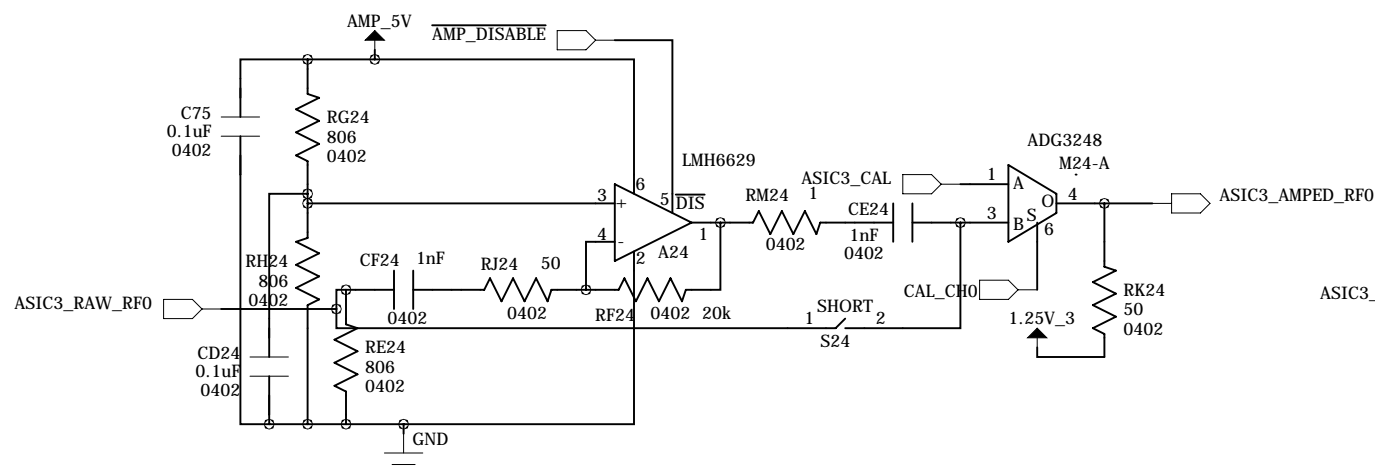
C

B

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institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

title: carrier02
revision: D
IDLAB design #: IDL_13_046
circuit design: LJR, MZA, KAN, GSV, LM, GV
PCB design: MZA, LJR

sheet #: 11 of 11
sheet description: ASIC3_AMPS
date last modified: 2013-11-22